Silicon Cortex (SCX)

Report

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Silicon Cortex (SCX)

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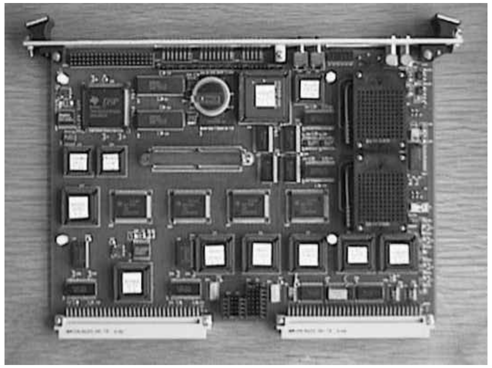
1. What is Silicon Cortex?

Silicon Cortex (SCX) is a prototype infrastructure for performing multi-chip neuromorphic computation.

It is a system which can connect special analog very large scale integration (aVLSI) *silicon* chips using conventional, digital computer hardware. The aVLSI chips have many individual 'silicon neurons' or 'neuromorphs' on them, each of which uses the physical properties of transistors to mimic the physical behaviour of neurons (for example those that occur in *cortex*).



An SCX-1 circuit board.

2. What is it for?

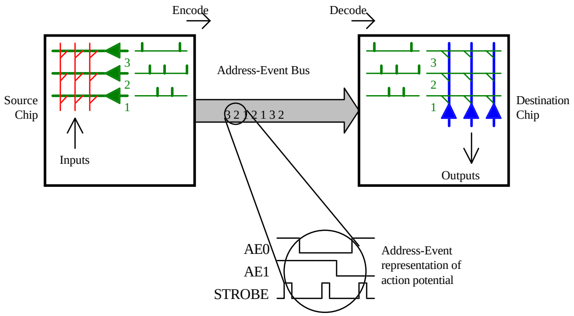
The SCX project is intended to
- be the prototype of systems which modellers can use to model large networks of neurons;
- act as a test-bed for multi-chip neuromorphic systems that will later be used on mobile robots etc.;
- explore technical issues that arise in connecting multiple neuromorphic chips together.

3. How do models constructed using the SCX system differ from those constructed using other systems?

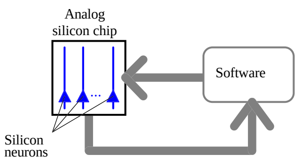
- Conventional digital computers *simulate* the actions of neurons taking perhaps up to 1 minute to simulate 1 second of activity of a single neuron, whereas the aVLSI chips used in the SCX system exploit the physics of their transistors to *emulate* the activities of any number of neurons in *real time*, or in other words, at the same speed as real biological neurons.
- The SCX system uses a biologically inspired, pulse-based method of communicating between neurons called Address-Event Representation.

4. Address-Event representation

Address-Event (AE) representation uses the occurrence of an address on an asynchronous digital bus to represent the occurrence of an action potential in a neuromorph on a chip. AEs from many thousands of neuromorphs could be multiplexed together on one bus, thus solving the problem of how to connect such large numbers of neuromorphs within the constraints imposed by the chip packaging and circuit board technologies.

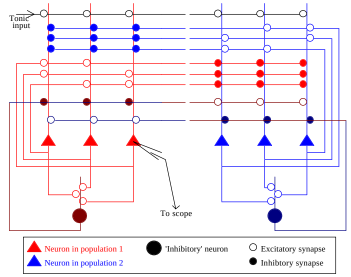


Address-Events are routed between chips under complete software control, thus preserving the reconfigurability of the neural networks implemented on the SCX system, a reconfigurability that is often absent in other, more specialised neural network hardware.



5. An example neuronal network

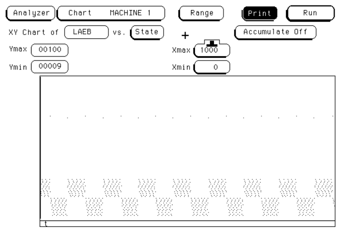
As a proof of concept, we have implemented a simple, recurrently connected circuit of integrate-and-fire silicon neurons, configured as shown in the diagram below (except each population contains 12 rather than 3 neurons).



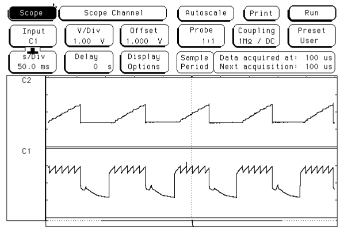
NB. Our technology allows us omit interneurons between 'inhibitory' neurons and excitatory synapses and *vice versa*, and in this example we have chosen to omit them, thus appearing to violate Dale's principal. However, we could equally well choose to accord with this principal by inserting the necessary interneurons.

6. Results

With suitably adjusted connection strengths, the network settles into a stable oscillatory firing pattern. The neurons in one 'excitatory' population fire for a period whilst neurons in the other population are silent, then the pattern of activity swaps over between the two populations. When one population is firing, each output contributes to the inhibition that prevents neurons in the other population from firing, and also produces an EPSC in the associated 'inhibitory' neuron. After integrating a certain number of such inputs, this neuron will reach its threshold and fire. When it does so, it produces a large inhibitory effect on the neurons in the population that was firing, thus bringing their activity to a halt. Neurons in the previously silent population thus no longer receive inhibitory input and can now begin to fire, and continue to do so until their associated 'inhibitory' neuron fires. The cycle then repeats (see below).



A raster plot of address-event activity over the course of several oscillatory cycles of the network described above. The vertical axis represents the address of the neuron in the network. Each plotted point represents the occurrence of an address-event, and hence the firing of a neuron. The horizontal axis represents the firing order (not strictly time). The lower twelve traces represent the activity of the neurons in one of the 'excitatory' populations. The next twelve traces represent the activity of the neurons in the other 'excitatory' population. The two traces further up represent the activity of the two 'inhibitory' neurons.



The lower trace (C1) shows the 'membrane potential' of one of the 'excitatory' neurons over time, and the upper trace (C2) that of the associated 'inhibitory' neuron.

7. Conclusion

We have demonstrated the basic functionality of our multi-chip neuromorphic computation infrastructure and are now going on to explore its use in multiple applications, including some that take sensory input from a neuromorphic silicon retina.

Acknowledgements:
The SCX-1 printed circuit board was designed and produced by Stephen R. Deiss of Applied Neurodynamics, 345 Via Montanosa, Encinitas CA 92024, USA.
The aVLSI chips were designed by the late Dr. Misha Mahowald, and fabricated via the MOSIS service.
Some of the diagrams used in this poster are to appear in: Deiss, S. R., Douglas, R. J. & Whatley, A. M., "A Pulse-Coded Communications Infrastructure for Neuromorphic Systems", ch. 6, in Maass, W., & Bishop, C. M., editors, Pulsed Neural Networks, MIT Press, in press.
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