Evaluation of topologies and optimal design of a hybrid distribution transformer

Evaluation of Topologies and Optimal Design of a Hybrid Distribution Transformer

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Abstract

Due to the increasing integration of distributed generators, the grid underlies conceptual challenges. To ensure an efficient and reliable operation, more controllable assets are expected in the future grid. The transformer as one of the most important components possesses only limited control capabilities today. By combining a conventional transformer with a converter, a hybrid transformer with comprehensive controllability is obtained. In this paper suitable concepts are investigated and an optimum design is determined to compare its potential to conventional and solid state transformers.

Introduction

Today's energy grid is in operation for several decades now and has not undergone a paradigmatic change yet [1]. However, the operating conditions of the grid are changing. By substitution large scale power plants with distributed generators using renewable energy sources, instantaneous energy reserves based on inertia are reduced. Furthermore, new and dynamic types of loads like electric vehicles are emerging. Increasing fluctuations in the grid voltage are the result. To ensure an efficient, economic and sustainable operation of the power system, several approaches have been developed to control parameters like voltage, transmitted active and reactive power or harmonics. These systems range from tap changers over diverse FACTS devices to solid state transformers (SSTs) [2],[3]. Up until today, the adjustment of voltage with tap changers is the most common way to control grid parameters. Mechanical on load tap changers are still the standard solution despite drawbacks like arcing, high maintenance cost and slow operation. Electronically assisted or full-electronic tap changers were developed to overcome these problems but still do not have a noticeable market share. In the transmission grid, FACTS devices are used to control voltage or increase the transferable power e.g. to enable the integration of large wind farms or to transport power over very long distances [4]. Similar systems were also introduced for the usage in the distribution grid and are known as "custom power devices" [5]. SSTs offer the widest range of controllable parameters. However, recent investigations reveal that cost are increased by a factor of more than four while losses increase by a factor of roughly three compared to a line frequency transformer (LFT) [6]. This prevents the widespread application of the SST for AC/AC conversion in the near future whereas an application in DC grids is advantageous.

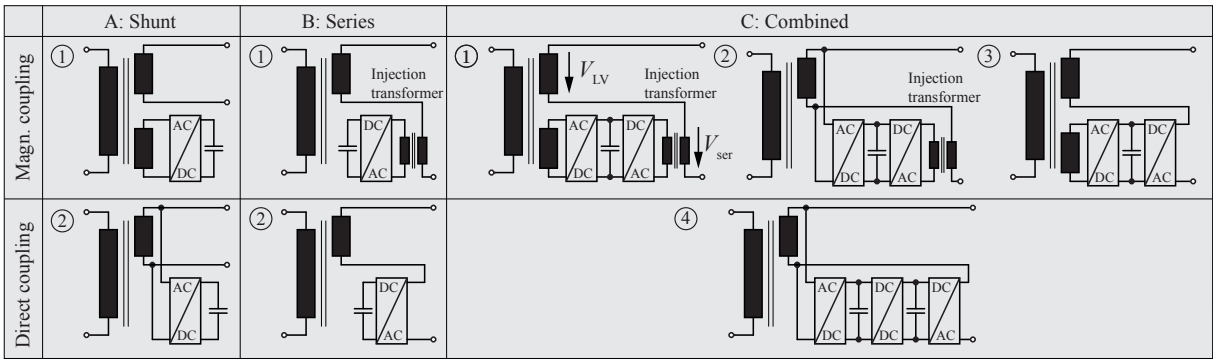

Figure 1: Possible configurations of HTs: Shunt connected converters for the injection of a reactive current (A), series connected converters for the addition of a reactive voltage (B) and a combination of series and shunt connected converters for active and reactive voltage and current injection (C).

A promising alternative concept is addressed in this paper. It combines a LFT with a power electronic converter to form a hybrid transformer (HT) [7]. The power electronic converter enables the control of different parameters and has to be rated only to a fraction of the transformed power. This allows to combine the high efficiency and low cost of a conventional transformer with the flexibility of a power electronic converter. In contrast to SSTs, power can still be transferred if the power electronic converter fails so that the reliability of the overall system is ensured.

The single-phase equivalent circuits of different configurations of HTs are depicted in Fig. 1. Depending on the configuration, the control of voltage, active and reactive power as well as active filtering and three phase load balancing are possible. Compared to FACTS and custom power devices, with the HT cost and volume are reduced due to the integration into one single smart asset.

The concept of a single-phase HT has been presented among others in [7] more than a decade ago. In [8] several alternative arrangements of transformers augmented with power electronic converters are discussed. The authors of [9] put emphasis on the application of a matrix ac-ac converter and proof its ability to control the voltage amplitude in a 50 V three-phase laboratory setup. In [10] voltage and power factor control of a single-phase prototype employing a voltage source inverter (VSI) have been verified experimentally. A comparison of converter topologies for a three-phase HT consisting of several parallel and series connected modules is carried out in [11]. Despite the stated publications, HTs are still far away from a competitive alternative to transformers equipped with tap changers. Many aspects like filter design and a comprehensive determination of efficiency and volume including all relevant system components have not been investigated yet. Even though in theory different configurations and converter topologies for HTs are possible, the practical applicability is limited by available semiconductor devices and complexity.
Therefore, this paper starts with a brief discussion of different configurations, possible grid voltage levels and topologies for the HT in **Section 1**. An optimisation procedure used to determine pareto optimal designs in terms of efficiency and power density is detailed in **Section 2**. A focus is put on the design of the differential mode filter. With the procedure an optimal design and its performance characteristics are presented in **Section 3** and compared to the LFT and the SST in **Section 4** taking volume, cost, losses and controllability into account.

1 Comparison of Hybrid Transformer Concepts

In the following, different configurations for HTs are presented and compared. Favorable voltage levels for the HT in the grid are compared and possible converter topologies are identified by taking the limits of available semiconductor devices into account.

1.1 Basic Configurations of Hybrid Transformers

There are two ways of influencing voltage and current of a LFT with a converter. On the one hand, a current can be injected on the high voltage (HV) or low voltage (LV) side by using a shunt connected converter as shown in Fig. 1 configurations A. On the other hand, a voltage can be added to the HV or LV side voltage with a series connected converter (configurations B). By combining both shunt and series connected converter, basic configuration C is obtained. For the converters, only VSIs are considered. Required filter elements are considered as part of the converter and are thus not shown separately. The converter and the main transformer can be connected directly or with the use of a magnetin injection transformer or an auxiliary winding. With the three basic configurations different functionalities can be realized. In configuration A a reactive current can be injected, power factor can be controlled and active filtering of harmonics is possible. Basic configuration B enables the control of the load voltage by adding a reactive voltage component. Since no active power can be applied by the converters with the concepts A and B, a change in voltage and current results in a change of the power factor. This drawback is eliminated in basic configuration C where almost arbitrary voltage and current vectors can be generated so that the focus is put on this alternative in this paper. The shunt and the series converter are connected back-to-back to the same dc-link. Since the voltage added in series is only a fraction of that of the LV grid an adaption of the converter input and output voltages is necessary to obtain a reasonable utilization of the semiconductor blocking voltage. This can be done with the help of an additional transformer (C ②), a tertiary winding (C ③) or both (C ①). Another possibility is to use a bidirectional dc-dc converter (C ④).

1.2 Suitable Voltage Levels for HTs

In this paper, a controllable voltage range of $\pm$ 10% is assumed for the HT. Due to the high voltage and power ratings of transformers in the transmission grid, complex and costly converters are necessary to control the voltage to a reasonable extend. A system being economically competitive to a tap changer is therefore expected to operate within the distribution grid. Fig. 2 shows voltage levels as well as transformer ratings and winding arrangements

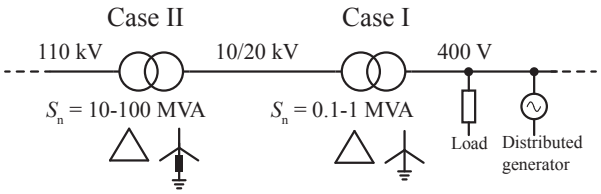

Figure 2: Typical voltage levels, transformer ratings and winding arrangements in European distribution grids.

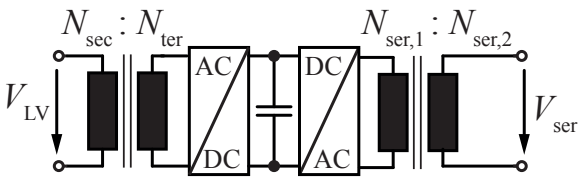

Figure 3: Schematic representation of configuration C ①.

for a typical European distribution grid [1]. Two possible cases of application for the HT with distinctive benefits can be identified.
Case I: The HT can be used at the interconnection of the 20 kV and 400 V grid. By controlling the voltage locally, an increased integration of small scale renewable energy sources is possible [12], [13]. A series voltage of $V_{ser} = 23\,V_{RMS}$ has to be generated.
Case II: The application of the HT at the interconnection between the 110 kV and $10/22$ kV grid requires a series voltage of up to $V_{ser} = 1270\,V_{RMS}$. Control of active and reactive power flow can be utilized to improve loading of lines in a meshed system [14].

1.3 Suitable Converter Topologies

The simplified representation of configuration C ① given in Fig. 3 is considered to derive the transformer turns ratios used to describe different realisations of configurations C ①, C ② and C ③. The following relation represents the adaption of the series voltage V_{ser} and the LV grid voltage V_{LV} for the required voltage control range of $\pm$ 10%:

$$\frac{V_{ser}}{V_{LV}} = r_{sh} \cdot r_{ser} = 10\% \quad \text{with} \quad r_{sh} = \frac{N_{ter}}{N_{sec}} \quad \text{and} \quad r_{ser} = \frac{N_{ser,2}}{N_{ser,1}}$$

In the low and medium voltage distribution grid, the neutral point is usually grounded directly or through a petersen coil, see Fig. 2 and thus needs to be connected to the converter. If no injection transformer is used as in C ③, the neutral point must be connected to the midpoint of the split dc-link. In this case, the peak value of the series voltage $\hat{V}_{ser}$ is lower than $\frac{V_{dc}}{2}$ so that for the dc-link voltage $V_{dc} \geq \sqrt{8} \cdot V_{ser}$ applies. The minimum semiconductor blocking voltage $V_{block,min}$ can be calculated by taking the required maximum converter voltage adjustment of 10% of the line-neutral voltage $V_{l\text{-}n}$ and the number of converter levels N into account. For $N > 2$ a NPC or flying capacitor converter is assumed. With increasing N the required semiconductor voltage and current ratings reduce. Due to the series connection of the converter and the load, the converter current I_{conv} is equal to the LV side current and can be calculated from the power rating of the transformer S_{trafo}:

$$V_{block,min} = \sqrt{8} \cdot \frac{10\% \cdot V_{l\text{-}n}}{N-1}; \qquad \hat{I}_{conv} = r_{ser} \hat{I}_{sec} = \frac{2}{15} \cdot \frac{S_{trafo}}{(N-1) \cdot V_{block,min}}$$

If a series injection transformer is used, the secondary side of this transformer should have a star connection with its star point connected to neutral. The necessary dc-link voltage can be lower in this case if for example space vector modulation is used: $V_{dc} > \sqrt{6} \cdot V_{ser}$. Again, for a N-level topology, the minimum ratings can be determined:

$$V_{block,min} = \sqrt{6} \cdot \frac{10\% \cdot V_{l\text{-}n}}{(N-1) \cdot r_{ser}}; \qquad \hat{I}_{conv} = \frac{\sqrt{3}}{15} \cdot \frac{S_{trafo}}{(N-1) \cdot V_{block,min}}$$

The semiconductors are assumed to operate at a fraction of $k = \frac{V_{block,\,min}}{V_{block}} = 0.6$ of their voltage rating. For case I, Fig. 4 shows the necessary current capability of the converter as a function of the blocking voltage V_{block} with the power rating of the main transformer as a parameter. Furthermore, the resulting blocking voltages for different values of turns ratios of the series injection transformer r_{ser} and for a configuration without this transformer are shown as vertical lines. Each intersection represents a possible realisation of the converter. Due to the higher voltage level, emphasis is put on a realisation with multilevel converters and without series injection transformer in case II. An auxiliary winding with a turns ratio between the LV and auxiliary winding of $r_{sh} = 0.1$ is required nevertheless so that configuration C ③ has to be chosen. Semiconductor ratings for a N-level topology are depicted as crosses in Fig. 5. Realizations for the highest power levels for both cases I and II are listed in Tab. I. By omitting the series injection transformer, volume and cost can be minimized. Increased semiconductor and filter requirements as well as complexity associated with high voltage multilevel converters entail high system cost. Thus, the practical application of Case II appears improbable unless HV SiC devices are applicable so that HTs for

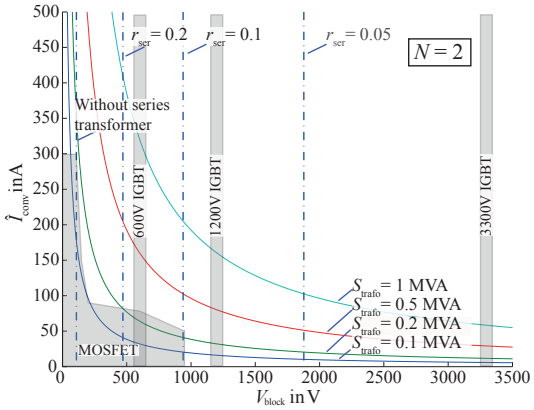

Figure 4: Required semiconductor ratings for 10/20 kV-400 V HTs for different power ratings of the main transformer and two-level converters $N = 2$. Each intersection with a vertical line represents a possible realisation with the respective series injection transformer.

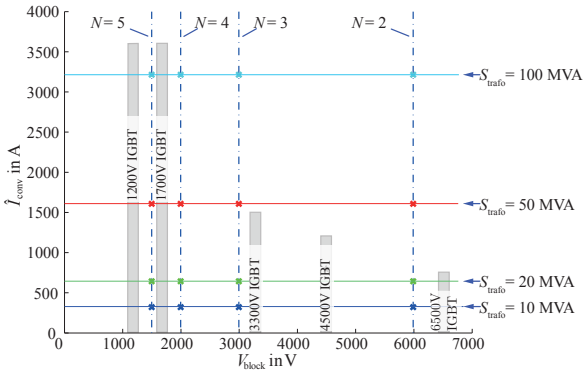

Figure 5: Required semiconductor ratings for 110 kV-10/20 kV HTs for different power ratings of the main transformer. Each cross indicates a possible realisation with the use of a N-level topology without a series injection transformer.

Table I: Realizations of a 1 MVA HT (case I) and a 100 MVA HT (case II) with ratios r_{ser}, r_{sh}, number of converter levels N, possible semiconductor and number of parallel switches/moduls/phase-legs P.

	Conf.	r_{ser}	r_{sh}	N	Switches	P
Case I	C ①	0.2	0.5	2	IGBT, 600 V, 600 A	1
	C ②	0.1	-	2	IGBT, 1.2 kV, 300 A	1
	C ③	-	0.1	2	MOSFET, 120 V, 150 A	12
	C ③	-	0.1	3	MOSFET, 100 V, 300 A	6
Case II	C ①	1.7	0.06	2	IGBT, 3.3 kV, 1.5 kA	5
	C ③	-	0.1	2	IGBT, 6.5 kV, 750 A	5
	C ③	-	0.1	3	IGBT, 3.3 kV, 1.2 kA	3
	C ③	-	0.1	5	IGBT, 1.7 kV, 3.5 kA	1

Table II: Specifications of the 40 kVA converter for a 400 kVA, 20 kV-400 V HT. The switching frequency and the filter elements are the result of the optimization procedure presented in Section 2.

Parameter	Value
Topology	Conf. C ③, two-level back-to-back VSIs
Controllability	±10% of nominal V (LV side), P and Q
S_{conv}, V_{ser}	40 kVA, 23 V
Switches	120 V MOSFETs, IPP041N12N3 (Inf.), 12 parallel
f_{sw}	16 kHz
V_{dc}, C_{dc}, L_N	70 V, 5 mF EPCOS B32526, 100 µH
$L_{F,A}$, $L_{F,B}$	6.7 µH, 3.8 µH, custom METGLAS cores
$C_{F,A}$, $C_{F,B}$	1 mF, 1.9 mF, EPCOS B32524

Case I are investigated in the following. The focus is on a two-level VSI with back-to-back connected converters based on MOSFETs (Tab. I, line 3). The topology is depicted in fig:Topology. The upper part of Tab. II summarizes the specifications for the converter. As shown in Fig. 2 the LV side of a distribution transformer needs to provide an accessible star point. In order to connect the three phases to a common dc-link, the star point has to be provided by the converter which is realized by an actively balanced split dc-link.

2 Converter Optimization Procedure

In this section the procedure to obtain an optimal system design is deduced for Case I with a HT in configuration C ③ (Fig. 1). However, it should be noted that a similar approach can also be used for HTs with different voltage levels and configurations. The aim of the optimization procedure shown in Fig. 8 is a pareto optimal design in terms of power density and efficiency. The semiconductor switching frequency is varied after the specifications and constant parameters are defined. For each switching frequency a filter is designed, the system is simulated, semiconductor losses are calculated, optimal filter inductors are determined and the volume of the cooling system is approximated. The different blocks of this procedure are presented briefly. Accounting for roughly half of the converter volume, the filter and its optimal design is detailed with special attention.

2.1 Simulation Model

In addition to the circuit depicted in Fig. 6, the simulation model contains a simplified three phase three winding transformer model. The transformer model is based on three single phase transformer models represented by their short circuit inductances which have been approximated from the geometric setup shown in Fig. 9. If the short circuit measurements of a three winding transformer with concentrically arranged windings are transferred into the simplified equivalent circuit of Fig. 11, a negative inductance on the side of the middle winding is calculated, i.e. $L_S < 0$. In order to avoid numerical instability of the simulation model, coupled inductors are used as proposed in [15]. For the split dc-link an active balancing circuit as depicted in Fig. 6 is designed according to [16].

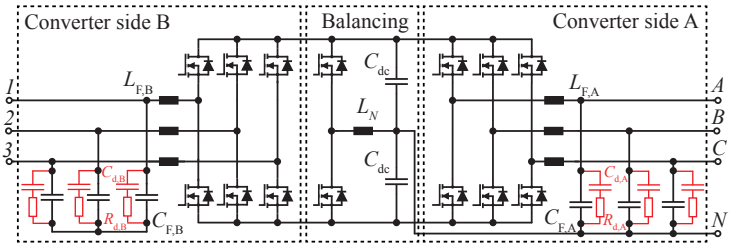

Figure 6: Three-phase, two-level back-to-back VSI with LC-filters and parallel $R_d - C_d$ damping branches considered for the 20 kV-400 V HT. Converter side A is connected in series to the low voltage transformer winding, converter side B is delta connected to the auxiliary transformer winding as shown in Fig. 7. The active balancing circuit provides a neutral point.

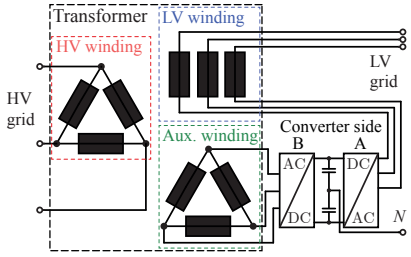

Figure 7: Three phase HT corresponding to configuration C ③ shown in Fig. 1.

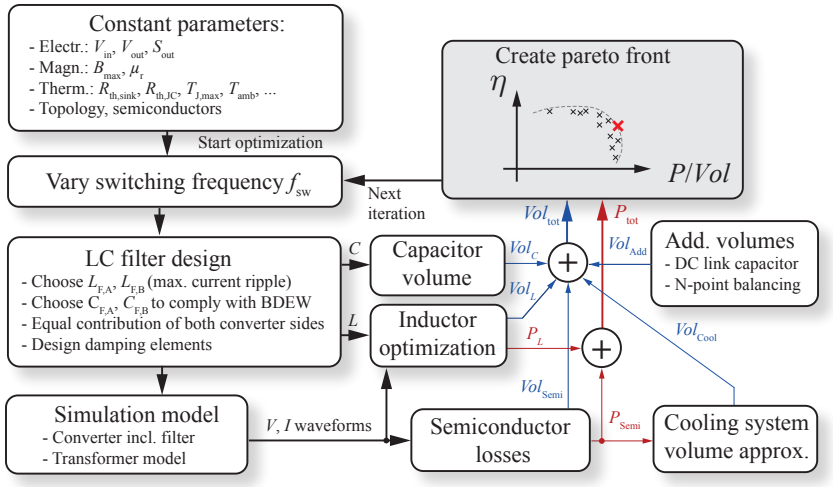

Figure 8: Optimization procedure applied to determine pareto optimal designs of the back-to-back converter in terms of efficiency and power density.

2.2 Inductor Optimization

Based on the inductance value and the simulated inductor current waveform the dimensions of the inductor are optimized for minimal volume by employing a genetic algorithm. Constraints ensure that the losses can be dissipated through an actively cooled surface and the core does not saturate. For each possible design core, skin, proximity and fringing losses are calculated.

2.3 Cooling System Volume Approximation

The heat sink is designed to ensure a junction temperature of the MOSFETs of $T_J = 100\,°C$ which has been determined to be a compromise between heat sink volume and semiconductor conduction losses. Forced convection cooling with a CSPI of $10\,W/(K \cdot l)$ is assumed, [17].

2.4 Semiconductor Losses

Conduction and switching losses of the MOSFETs are calculated from the simulated current waveforms and gate signals. By using the formulas stated in [18], a worst-case approximation of the losses is obtained derived from data sheet parameters to ensure a reliable operation under all operating conditions.

2.5 LC Filter Design

In order to ensure proper power quality and avoid disturbances caused by EMI, attention must be paid to the filter design. In this analysis LC filters with parallel $R_d - C_d$ damping branches are used on both sides of the converter, (Fig. 6). The damping elements R_d and C_d are calculated according to [19] with $n = \frac{C_d}{C_F} = 0.5$.
The harmonic limits for the grid current applied here are defined by the German association of energy and water industry BDEW in [20]. Defining stricter limits than IEEE 519/IEEE 1547, the BDEW standard is more suitable

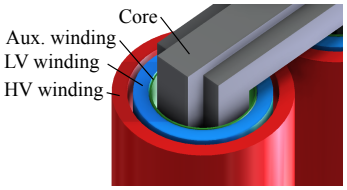

Figure 9: The windings are arranged by increasing voltage from the auxiliary to the HV winding.

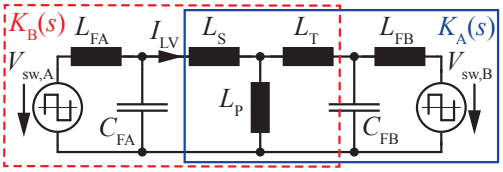

Figure 10: Single phase equivalent circuit of the HT (incl. LFT) valid for differential mode harmonics much greater than the LC filter resonance frequency.

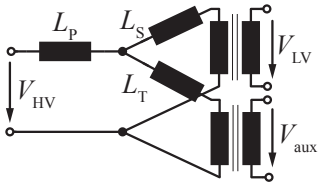

Figure 11: Simplified single phase equivalent circuit of the three winding transformer.

to ensure high grid power quality in the supposed scenario of increasing penetration of power electronic converters operating in the power grid. As proposed in [21] harmonic limits are extrapolated for frequencies between 9 kHz and 150 kHz. Although no standard covers this frequency range currently, an adaption can be expected. Harmonics at frequencies greater than 150 kHz have to comply with the CISPR11 standard. However, it has been verified by simulation that for the differential mode filter design the BDEW limits are more critical for the considered switching frequencies of up to 25 kHz. For typical distribution transformers, harmonics limits defined by BDEW are most difficult to comply with on the LV side since the limits are proportional to the short circuit power at the point of common coupling. Hence the filter design will focus on LV side current harmonics. For $f > 2\,\mathrm{kHz}$, the BDEW standard requires the harmonics to be calculated by evaluating a 200 Hz band:

$$I_{\nu,\mu} = \sqrt{\sum_{n=-19}^{20} I^2_{((\nu,\mu)\cdot 50+5\cdot \mathrm{n})\mathrm{Hz}}}. \tag{1}$$

As shown in Fig. 10, the HT can be represented by a single phase equivalent circuit valid for differential mode filter design. All voltages, currents and component values as well as the derived formulas are referred to the primary side. Since for the switching frequency $f_{sw} \gg \frac{1}{L_F C_F}$ applies, damping does not affect the propagation of harmonics for $f \geq f_{sw}$ and can be neglected. The indices A and B denote the two sides of the back-to-back converter. Since typical grid inductances and resistances are very small compared to the short circuit impedance of the LFT, the 20 kV and the 400 V grids are modeled by ideal voltage sources V_P and V_S, respectively. It is assumed that the LFT can be represented by its short circuit inductances L_P, L_S and L_T at the considered switching frequency harmonics. The voltage sources $V_{sw,A}$ and $V_{sw,B}$ represent the switched potentials of a half bridge on the converter sides A and B of the back-to-back converter. By substituting the voltage sources of the HV and LV grid with short circuits, additional damping due to the resistive and inductive characteristics of the grid is not included in the filter design. This conservative design ensures sufficient harmonic damping under all circumstances.

As both sides of the back-to-back converter are coupled by the transformer, harmonics produced by one converter side are also reflected to the other side. From the equivalent circuit, the contributions of both converter sides to the LV side current harmonics referred to the HV side $i_{LV} \leq |i_{LV,A}| + |i_{LV,B}|$ can be calculated, (2)-(3). For $\left|s^2 L_F C_F \gg 1\right|$, $\left|s^2 L_T C_F \gg 1\right|$ and $\left|s^2 L_P C_F \gg 1\right|$ approximations denoted with the tilde symbol can be given. The validity of these approximations has been checked for reasonable filter elements and transformer short circuit inductances.

$$i_{LV,A} = V_{sw,A}(s) \cdot \frac{1}{s^2 L_{F,A} C_{F,A} K_A + s L_{F,A} + K_A}; \qquad \tilde{i}_{LV,A} = V_{sw,A}(s) \cdot \frac{1}{s^2 L_{F,A} C_{F,A} \tilde{K}_A} \tag{2}$$

$$i_{LV,B} = V_{sw,B}(s) \cdot T_B \cdot \frac{1}{s^2 L_{F,B} C_{F,B} K_B + s L_{F,B} + K_B}; \qquad \tilde{i}_{LV,B} = V_{sw,B}(s) \cdot \tilde{T}_B \cdot \frac{1}{s^2 L_{F,B} C_{F,B} \tilde{K}_B} \tag{3}$$

Since superposition is used to calculate the current harmonics, the terms K_A and K_B correspond to those marked in Fig. 10 for $V_{conv,A} = 0$ and $V_{conv,B} = 0$, respectively. The factor T_B gives the fraction of the current harmonics produced by the auxiliary side converter which is transferred to the LV side.

$$K_A = s \frac{\left(s^2 L_{F,B} C_{F,B} + 1\right) \cdot \left(L_P L_S + L_P L_T + L_S L_T\right) + L_{F,B}\left(L_P + L_T\right)}{\left(s^2 L_{F,B} C_{F,B} + 1\right) \cdot \left(L_P + L_T\right) + L_{F,B}}; \qquad \tilde{K}_A = s\left(L_S + \frac{L_P L_T}{L_P + L_T}\right) \tag{4}$$

$$K_B = s \frac{\left(s^2 L_{F,A} C_{F,A} + 1\right) \cdot \left(L_P L_S + L_P L_T + L_S L_T\right) + L_{F,A}\left(L_P + L_T\right)}{\left(s^2 L_{F,A} C_{F,A} + 1\right) \cdot \left(L_P + L_T\right) + L_{F,A}}; \qquad \tilde{K}_B = s\left(L_T + \frac{L_P L_S}{L_P + L_S}\right) \tag{5}$$

$$T_B = \frac{L_P\left(s^2 L_{F,A} C_{F,A} + 1\right)}{\left(s^2 L_{F,A} C_{F,A} + 1\right)\left(L_P + L_S\right) + L_{F,A}}; \qquad \tilde{T}_B = \frac{L_P}{L_P + L_S} \tag{6}$$

In conventional LC filter design the maximum inductor current ripple and reactive power consumption of the capacitors defines the inductor and the capacitor values. For the considered converter, the reactive capacitor current

is comparatively small due to the low voltage level and can be compensated by the converter without a considerable increase of losses. Capacitance and inductance thus can be chosen with more degrees of freedom which allows an optimal selection of the elements. The filter design is based on the following procedure:

1. Calculate the necessary filter inductor to limit the maximum inductor current ripple to a given percentage $r_{L,\max}$. For two-level converters using sine-triangle or space vector modulation, the inductor values can be calculated dependent on the the switching frequency f_{sw}, the dc-link voltage V_{dc}, and the magnitude of the space vector V^*, [22]:

$$L_{\mathrm{F,sin-tri}} = \frac{V_{\mathrm{dc}}}{4 r_{L,\max} f_{\mathrm{sw}} I_n}; \qquad L_{\mathrm{F,SWM}} = \frac{V^*}{2\sqrt{3} r_{L,\max} f_{\mathrm{sw}} I_n}.$$

2. Calculate the capacitance of $C_{\mathrm{F,B}}$ as a function of $C_{\mathrm{F,A}}$ so that the contribution of both sides to the current harmonics on the LV side are equal. Using the approximations given in (2) to (6) an analytical formula can be derived:

$$|i_{LV,A}| \stackrel{!}{=} |i_{LV,B}| \Rightarrow C_{\mathrm{F,B}} = C_{\mathrm{F,A}} \cdot \frac{V_{\mathrm{sw,B}}(s) L_{\mathrm{F,A}}}{V_{\mathrm{sw,A}}(s) L_{\mathrm{F,B}}} \cdot \frac{L_{\mathrm{P}}}{L_{\mathrm{P}} + L_{\mathrm{T}}} \tag{7}$$

   whereas $V_{\mathrm{sw,A}}(s)$ and $V_{\mathrm{sw,B}}(s)$ are the harmonics of the half bridge voltages with reference to the neutral point on each converter side. For a given switching strategy, these voltage harmonics can be determined analytically or by simulation.

3. By inserting (7) into (2) and , $i_{LV,A}$ and $i_{LV,B}$ can be calculated or different filter capacitor values $C_{\mathrm{F,A}}$. The smallest capacitor value $C_{\mathrm{F,A}}$complying with the limits in a frequency range around the switching frequency is chosen.

4. Check, if switching frequency is far away from system resonances.

With this procedure a set of filter elements is determined for a given switching frequency and maximum current ripple. By performing the optimization procedure for different switching frequencies and current ripple values $r_{L,\max}$, the curves shown in Fig. 12 are obtained. It is obvious that a maximum ripple of 10% of the nominal current is a reasonable compromise to realise both low losses and low volume. For higher ripple current values, the semiconductor losses increase. Increasing heat sink and filter capacitor volume exceed the reduction of the inductor volume. For lower values of $r_{L,\max}$, the inductor volume and losses increase. A maximum inductor current ripple of 10% for both sides of the converter is consequently chosen for the filter design. The FFT of the simulated LV side current shows the effectiveness of the described differential mode filter design, see Fig. 13.

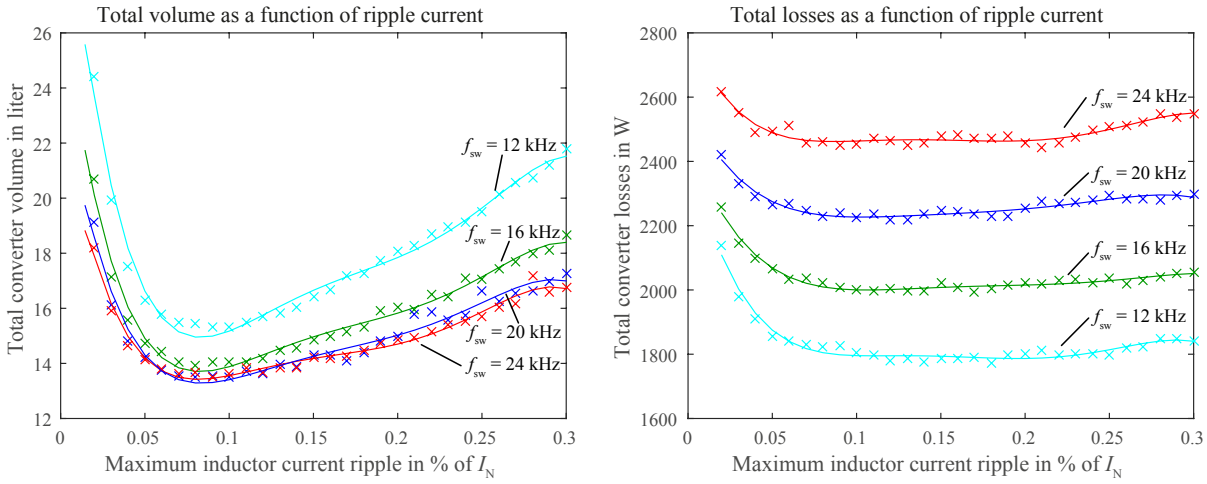

Figure 12: Total converter volume (left) and losses (right) as a function of the ripple current for different switching frequencies f_{sw}. Both volume and losses show a minimum at around 10% current ripple for all considered switching frequencies.

3 Optimal Design

With the procedure presented in the previous section, the pareto curve can be calculated for a 40 kVA back-to-back converter with the specifications given in Tab. II. As shown in Fig. 7, one side of the converter is delta connected

to the auxiliary winding of the transformer while for the other side each converter phase is series connected to the corresponding LV winding. For the series connected side, sine-triangle modulation in chosen since the neutral point has to be connected. For the delta connected side, space vector modulation is applied to take advantage of the 15% higher output voltage and hence reduced conduction losses for the same input power. To ensure reliable operation for all operating points, the design is performed for the scenario where the highest currents and hence losses occur. This is the case if the voltage of the HV grid is reduced by 10% and the HT is used to adjust the voltage of the LV grid to its nominal value. The pareto front for this scenario is shown in Fig. 14. Both efficiency and power density include the contribution of all relevant converter components assuming ideal packaging of the single components. For a real system, power density will be reduced by approximately 30%. Since genetic algorithms are involved in the inductor optimization, the simulated volumes and losses are scattered even if the same operating points are chosen. As expected, both efficiency and power density reduce for $f_{\mathrm{sw}} > 20\,\mathrm{kHz}$ since the switching losses increase and the heat sink required for ensuring a junction temperature of $T_{\mathrm{J}} = 100\,^{\circ}\mathrm{C}$ becomes voluminous. For the analyzed 400 kVA, 20 kV-400 V HT, a switching frequency of $f_{sw} = 16\,\mathrm{kHz}$ is chosen which results in an efficiency of 95% for the worst-case operation point and a power density of $3\,\mathrm{kW/l}$. If the operation at 70% of the rated power and at rated voltage in the HV grid is considered as an average operation point, the converter efficiency is 96% for the same design. The design parameters and the used components are given in the lower part of Tab. II. The 3D CAD rendering in figureXXX (to be included) shows a possible realisation of the converter system. The pie charts shown in Fig. 15 demonstrate how the different converter components contribute to the converter losses and volume.

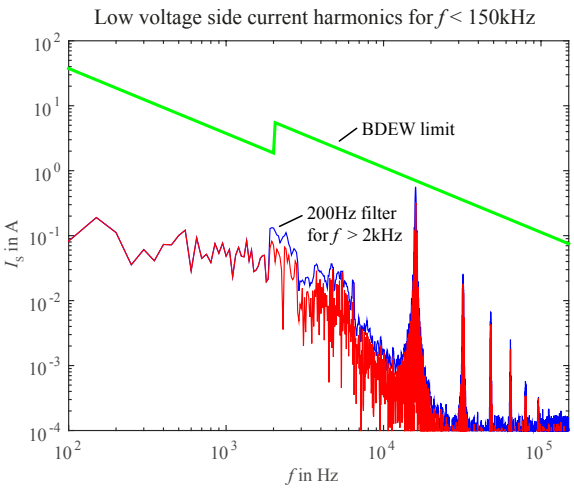

Figure 13: The proposed differential mode filter design ensures that the low voltage side current harmonics (red) comply with the BDEW limits (green). For $f > 2\,\mathrm{kHz}$ harmonics have to be evaluated in a 200 Hz band (blue), see (1).

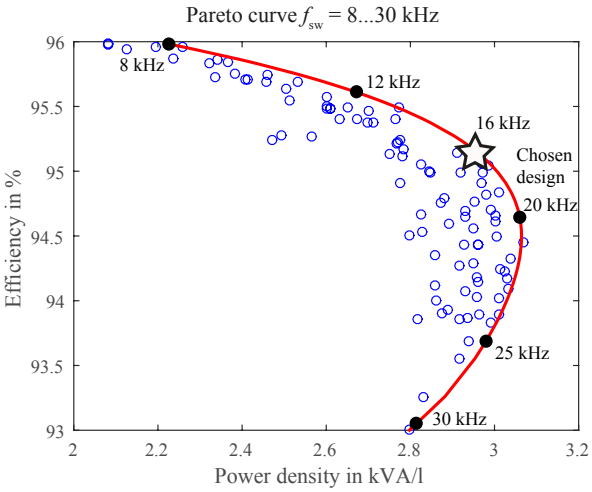

Figure 14: Total converter efficiency and power density including filters for a 40 kVA back-to-back converter used for the 400 kVA HT. The chosen design point is marked with a star at $f_{sw} = 16\,\mathrm{kHz}$.

4 Comparison of the HT with LFT and SST

In this section, the performance of the HT is compared to that of a LFT and a SST in terms of losses, volume, material cost and controllability. Since stationary applications in the distribution grid are considered, weight is not taken into account. For the LFT an oil immersed, 400 kVA 20 kV-400 V transformer is considered with an efficiency of $\eta_{\mathrm{trafo}} = 98.65\%$, a boxed volume including radiator of approximately 1000 l and material cost of 4200 USD. In [6] a comparison between a 1 MVA 10 kV-400 V SST and a LFT is performed. Since voltage and power ratings of the SST are in a similar range to that of the investigated HT, losses, volume, and cost are scaled linearly to that of a 400 kVA system. To estimate the converter cost for the HT the same relative cost of $52.7\,\mathrm{USD/kVA}$ that have been used for the SST in [6] are used. The boxed volume of the back-to-back converter is assumed to be 1.5 times higher than the sum of the components volumes. The material cost of a transformer equipped with a mechanical tap changer is estimated to be twice as much as that of an uncontrollable LFT. Tab. III summarizes the performance indices referred to the rated power for the LFT, LFT with tap changer, HT, and SST. Controllability is only compared in terms of voltage control for better comparability, although the control of further parameters and additional functionalities is possible with HTs and SSTs as described before. Even though the stated assumptions are rough, the potential of the HT becomes obvious from Fig. 16 which visualizes the performance of the three solutions. Except controllability, all quantities are referred to the values of the LFT.

Table III: Performance characteristics of the LFT, LFT with tap changer, HT, and SST. The numbers of the SST are taken from [6]. With the LFT with tap changer, voltage can only be controlled stepwise while a continuous control of voltage, active, and reactive power is possible with the HT and the SST.

	LFT	LFT + TC	HT	SST
Losses [W/kVA]	13.5	13.5	18.5	37.3
Volume [l/kVA]	2.8	3.1	2.85	2.7
Cost [USD/kVA]	10.5	21	15.8	52.7
V-Controllability	0%	10% (stepw.)	10%	100%

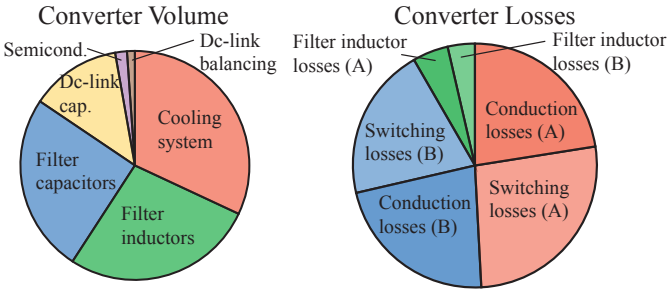

Figure 15: Contributions of the different converter components to the total converter volume (left) and losses (right) for the optimal design. A and B denote the two converter sides.

Reliability, efficiency and cost are the most important performance indices of a conventional distribution transformer. Taking only these parameters into account the LFT remains unrivalled. However, no parameter of the LFT can be controlled. Even with an additional tap changer, voltage adjustments are only possible in discrete steps. The SST offers full controllability at the expenses of more than four times higher cost and more than 2.5 times higher losses. The investigated HT possesses a control range of $\pm 10\%$ of the rated voltage or power which is considered to be sufficient for the distribution grid of the near future. In comparison to the SST, the efficiency of the converter of the HT is lower due the low voltage level causing high currents. Nevertheless, the losses of the total HT including the LFT are only increased by roughly one-third which results in a system efficiency of 98.16% for the worst case and 98.25% in average. Material cost are increased by 50% in comparison to the LFT. By disconnecting the converter from the LFT in case of a fault, the HT maintains the high reliability of the LFT. In contrast to that, for the SST power transmission is interrupted if a converter fault occurs which puts high reliability requirements on the semiconductors. As Fig. 16 shows, by employing a SST the volume cannot be reduced significantly and the HT increases volume only by 3%. In Fig. 17 the additional converter volume in comparison to the LFT and a possible attachment to the LFT is visualised.

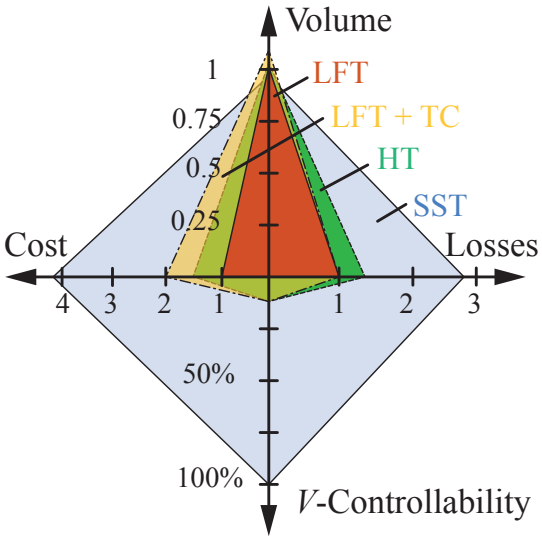

Figure 16: Comparison of total volume, full load losses, material cost and controllability for a 400 kVA 20 kV-400 V LFT (without tap changer), HT and SST.

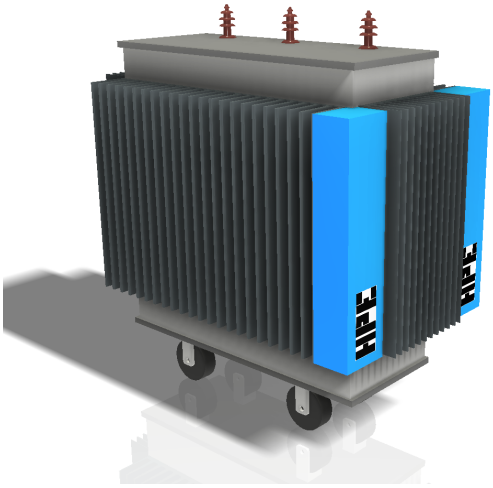

Figure 17: 3D rendering of the 400 kVA HT visualizing the 3% volume increase caused by the converter (blue boxes).

5 Conclusion

With HTs the controllability of conventional transformers is enhanced. Different configurations for HTs exist. However, active and reactive power and voltage control, active filtering and load balancing are only possible with two bidirectional converters connected back-to-back. Due to the high semiconductors and filter requirements, a practical application of HTs in the transmission and the HV distribution grid seems unlikely in near future. Thus, the potential of the HT is evaluated for a 400 kVA, 20 kV-400 V system using a two-level converter with MOSFET

modules. An optimization procedure is used to determine a pareto optimal converter design which features an average converter efficiency of 96% and a power density of 2 kVA/l including filters and enclosure. By adding the converter to a LFT to form a HT, the system efficiency is in average only degraded from 98.65% for the LFT to 98.25% for the HT while the volume increases by only 3%. A rough cost estimation revealed that the material cost of the HT will be approximately 50% higher compared to the LFT. In comparison to the tap changer transformer, the HT has slightly increased losses but increased control features at lower material cost so that the HT has the potential to become a reasonable alternative. For the application in the distribution grid the HT thus is a promising solution to enhance controllability of the transformer while increasing volume and losses only to a reasonable extend.

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