


# KISS PULPino - Updates on PULPino

## updates on PULPino

### Other Conference Item

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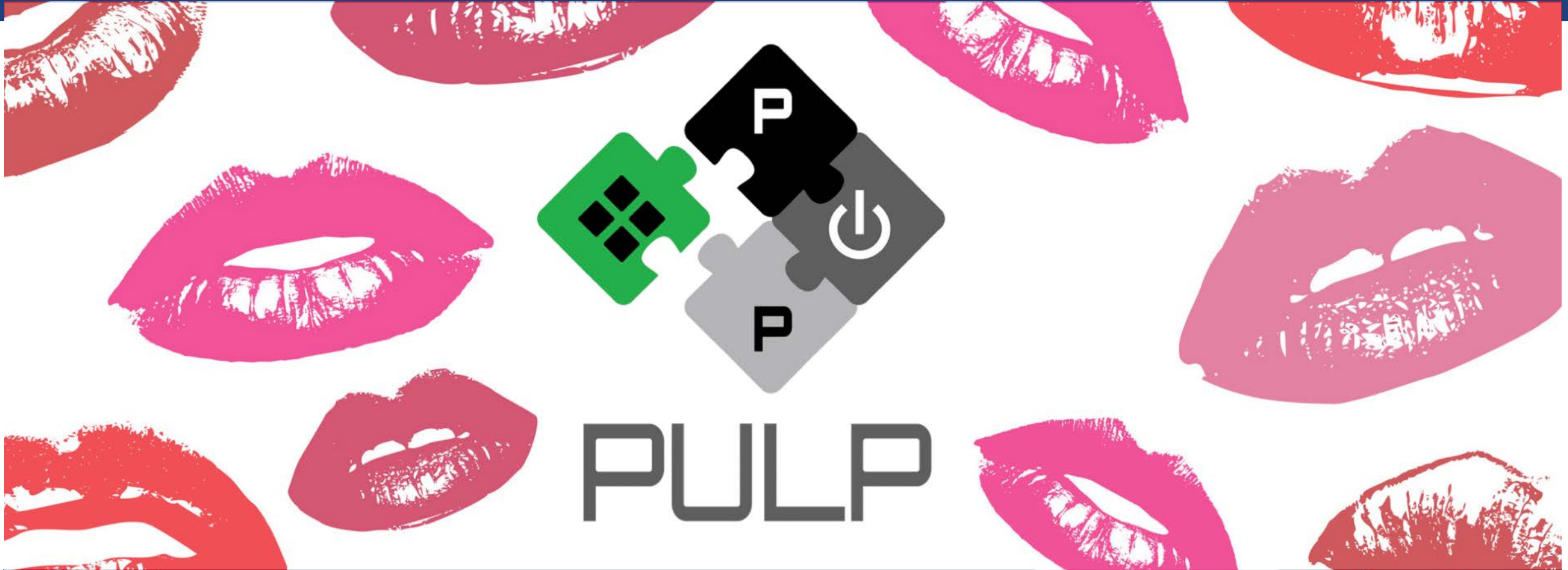
2016

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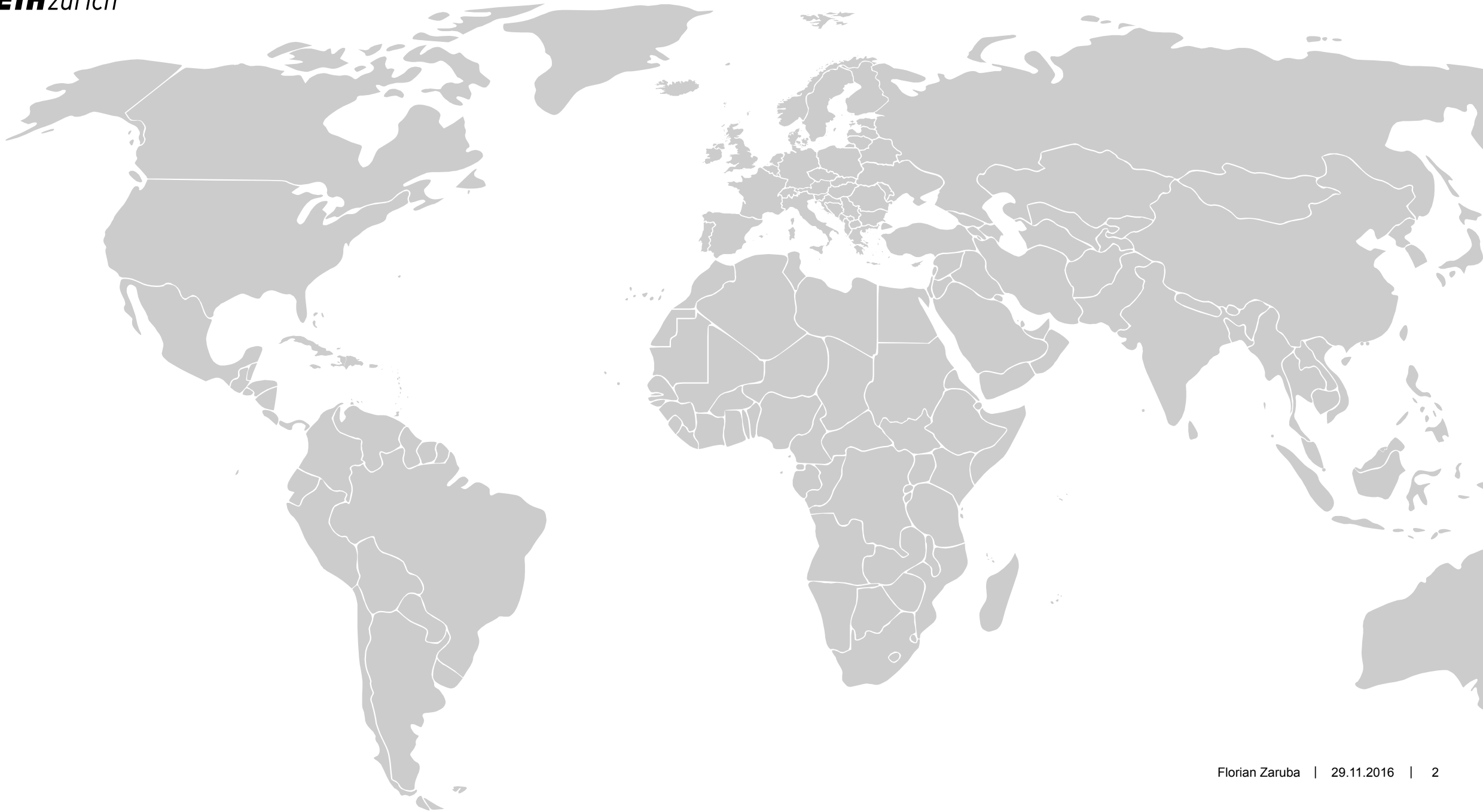
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# KISS PULPino

## Updates on PULPino

5<sup>th</sup> RISC-V Workshop, Mountain View (California), Florian Zaruba







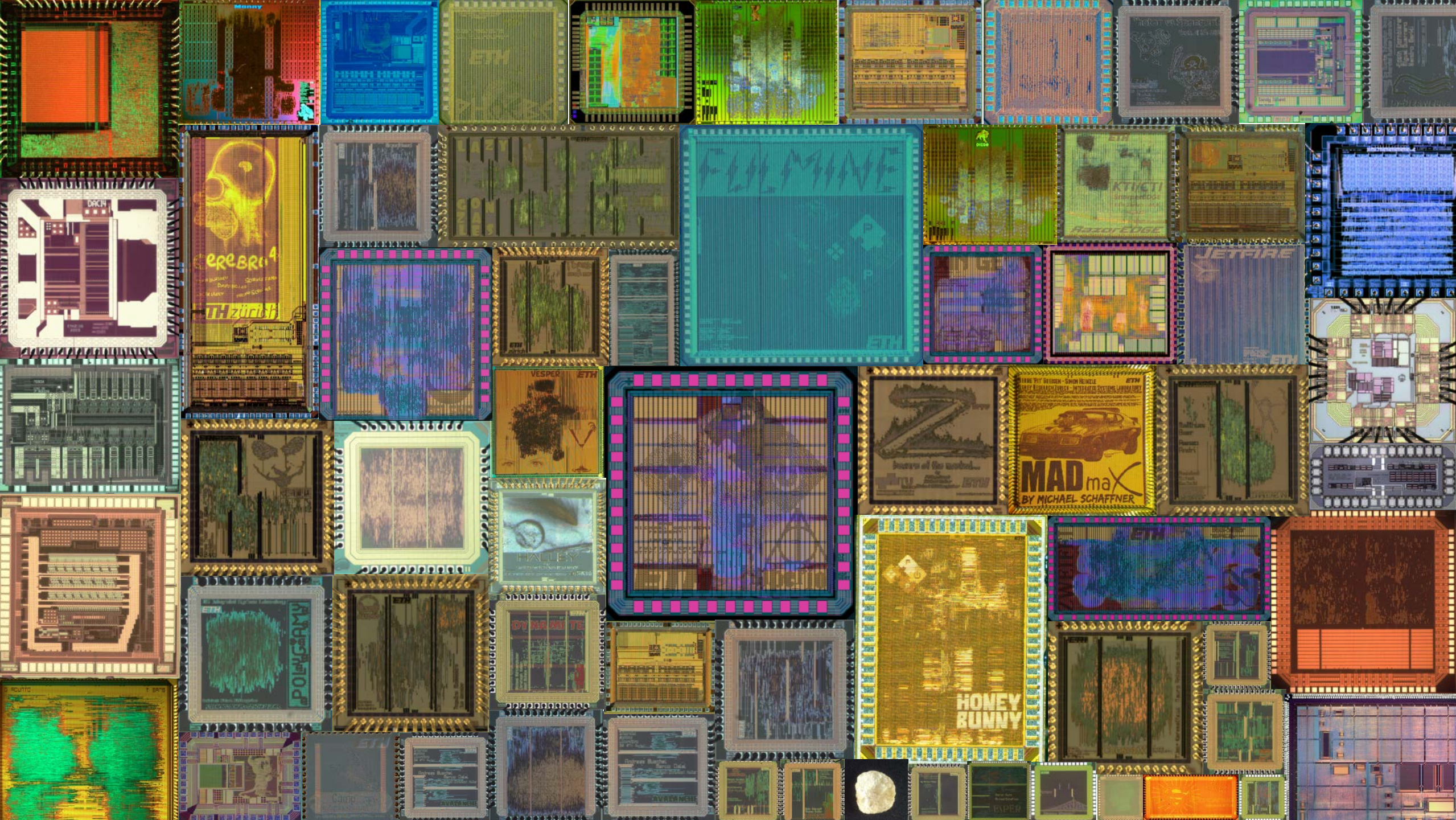






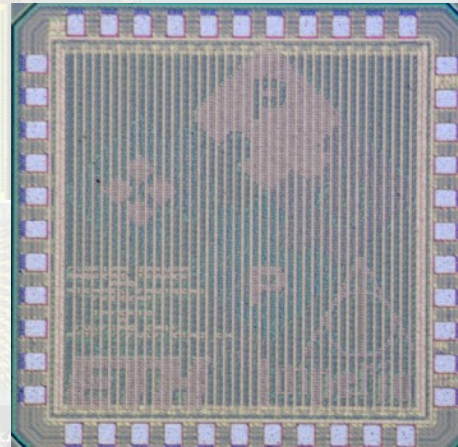


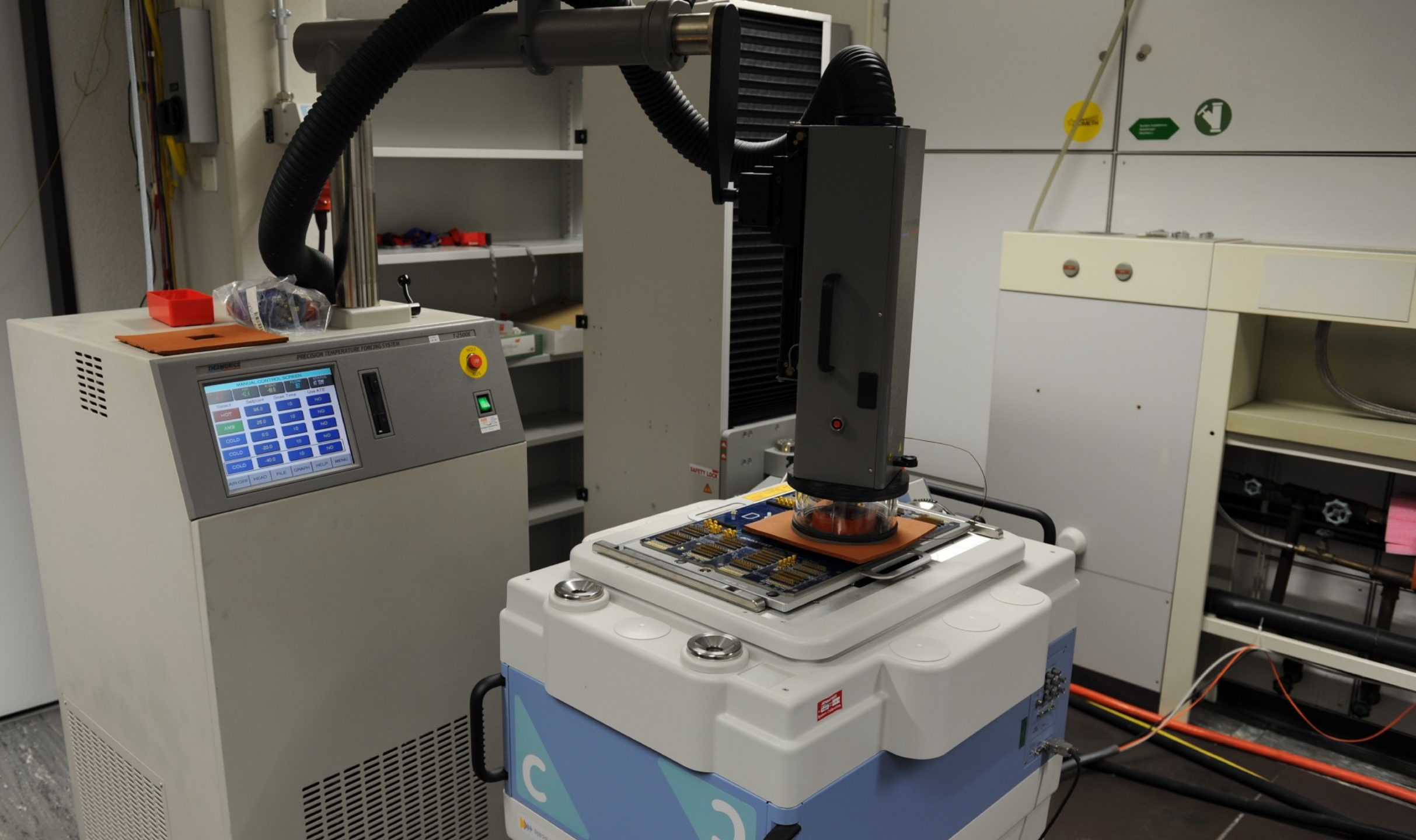


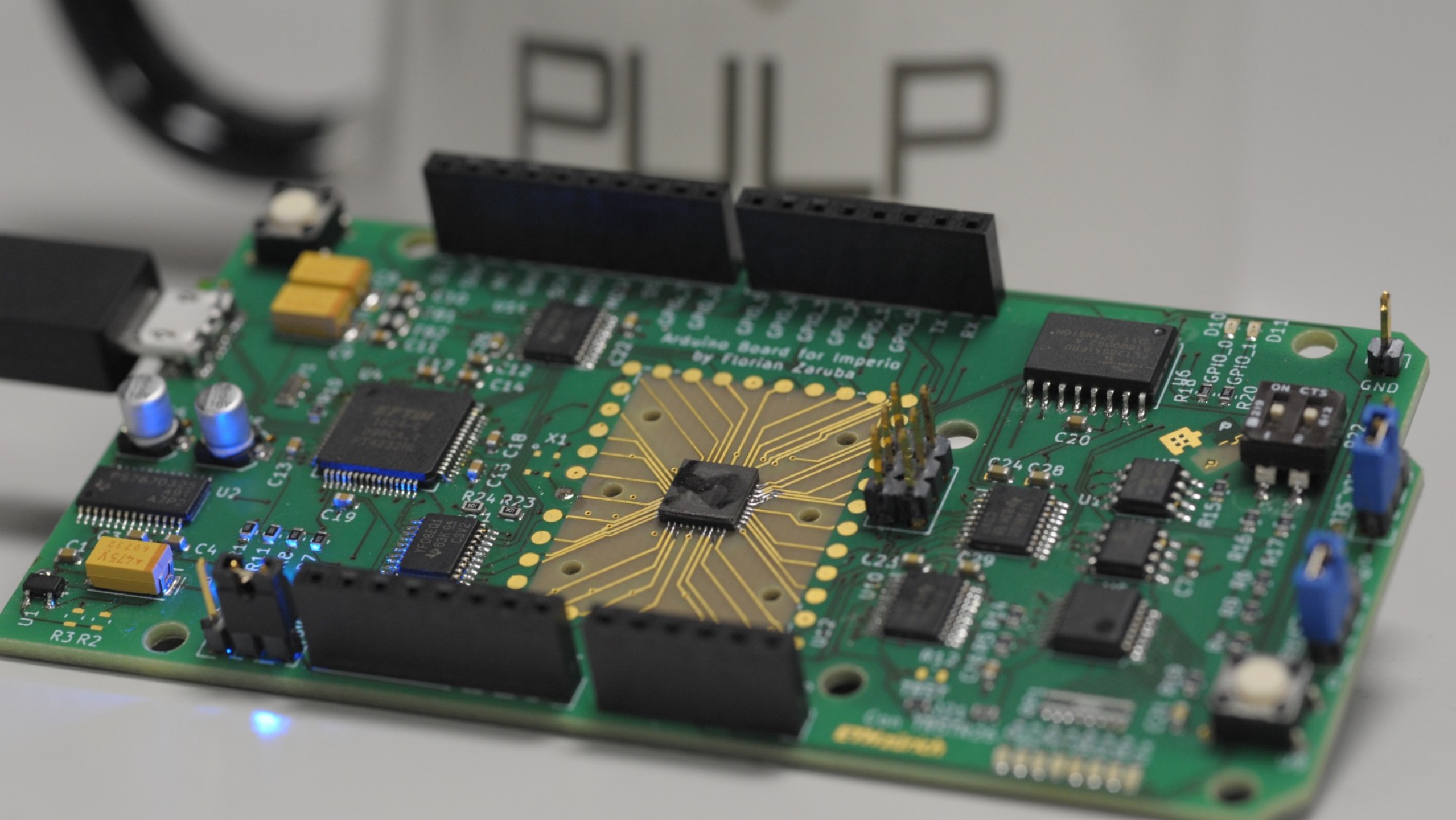


# Imperio

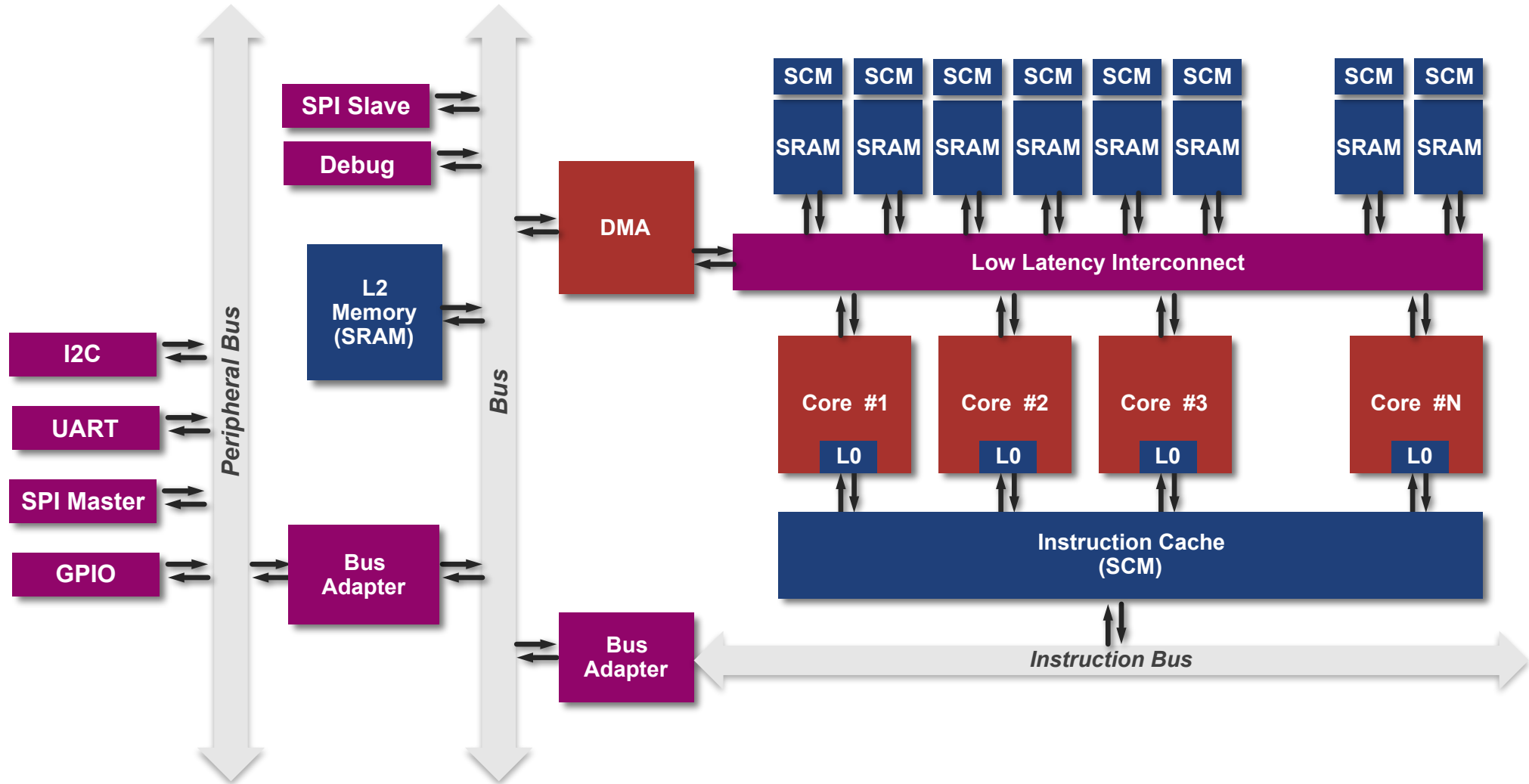
- **First** ASIC of PULPino (UMC 65)
- Complete  $\mu$ C (RV32IMC)
- Integrated FLL
- **Speed:** 500 MHz
- **Peripherals:**
  - 19 GPIOs, UART, I2C, SPI
  - JTAG Debug Interface
- 64 kB RAM
- **Operating Voltage:**
  - 0.9 – 1.2 V
- **Dynamic Power:**
  - 14 – 71  $\mu$ W/MHz, 1.2 V
  - 3 – 15  $\mu$ W/MHz, 0.9 V
- **Leakage:** 150  $\mu$ W
- **Area:**
  - 700 kGE\* (SoC)
  - 40 kGE\* (Core)



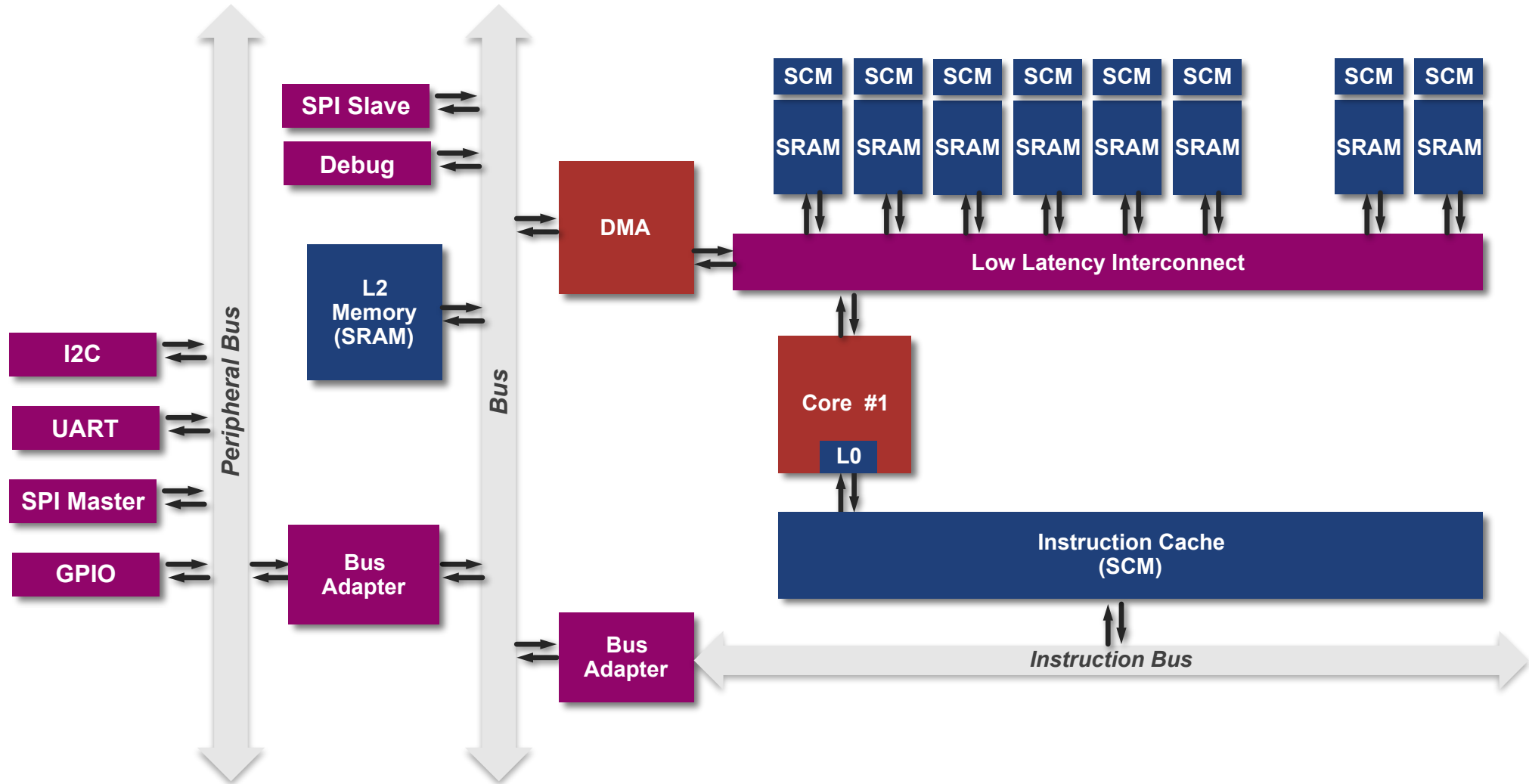




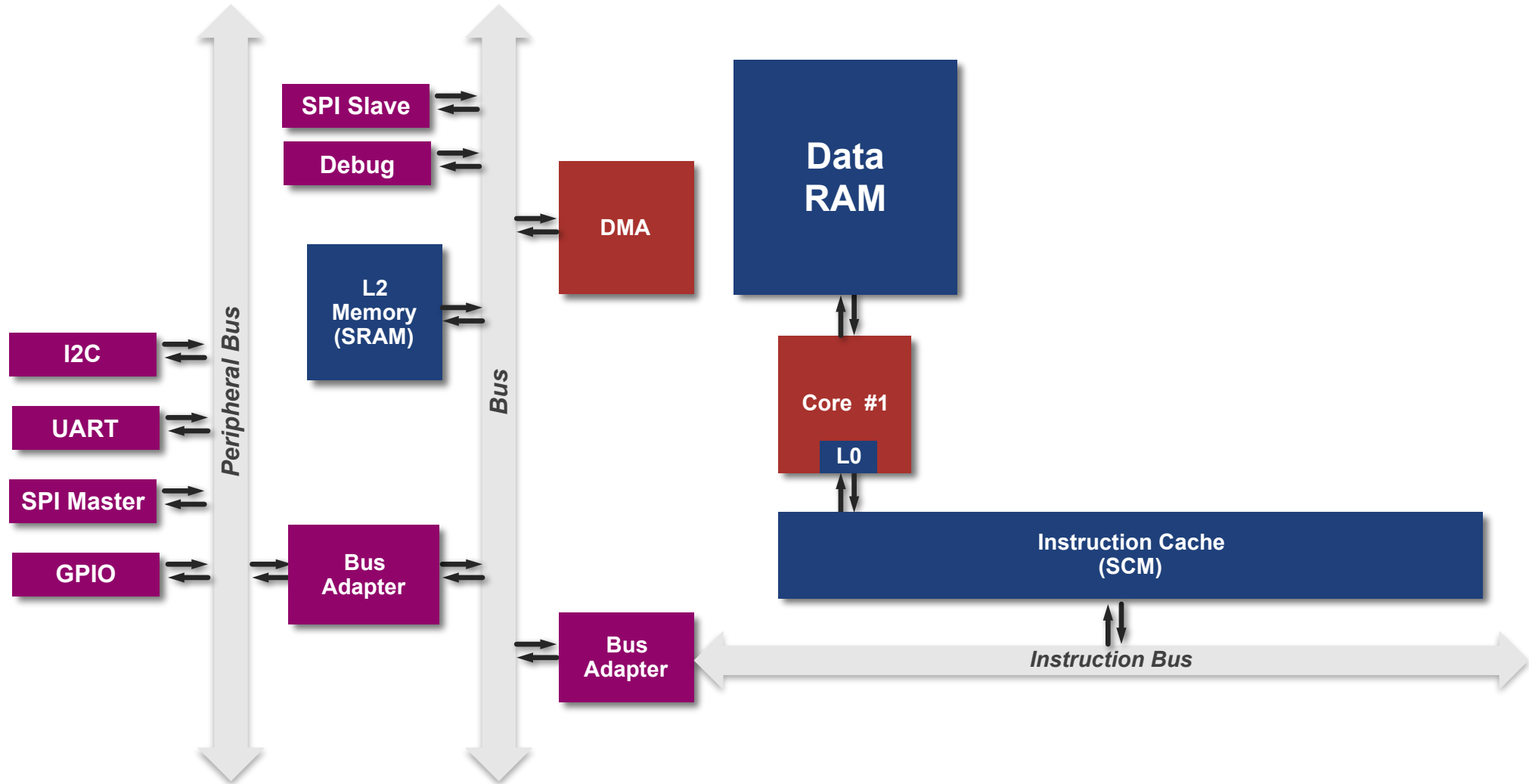
# Parallel Ultra Low Power Platform



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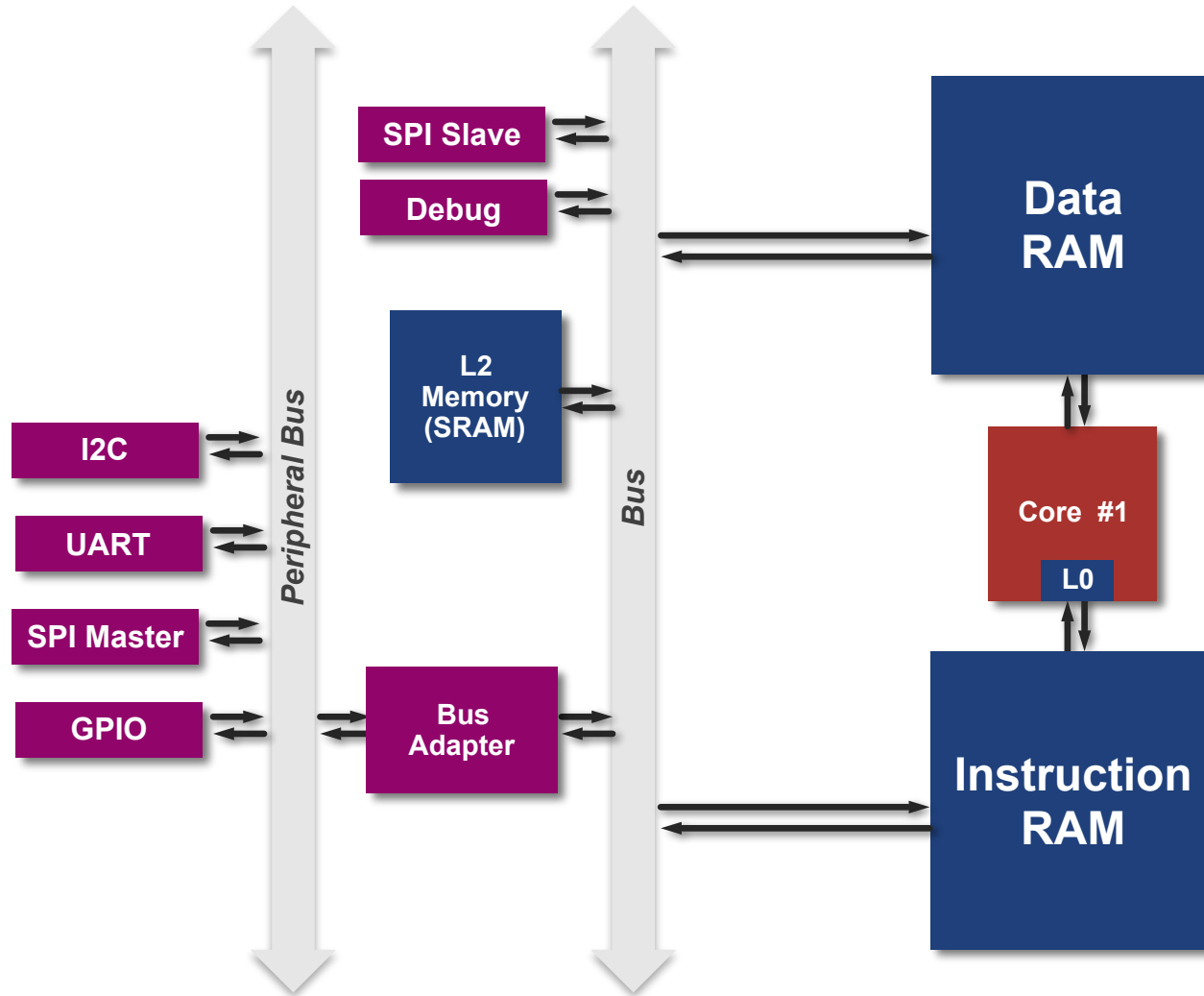


# Parallel Ultra Low Power Platform

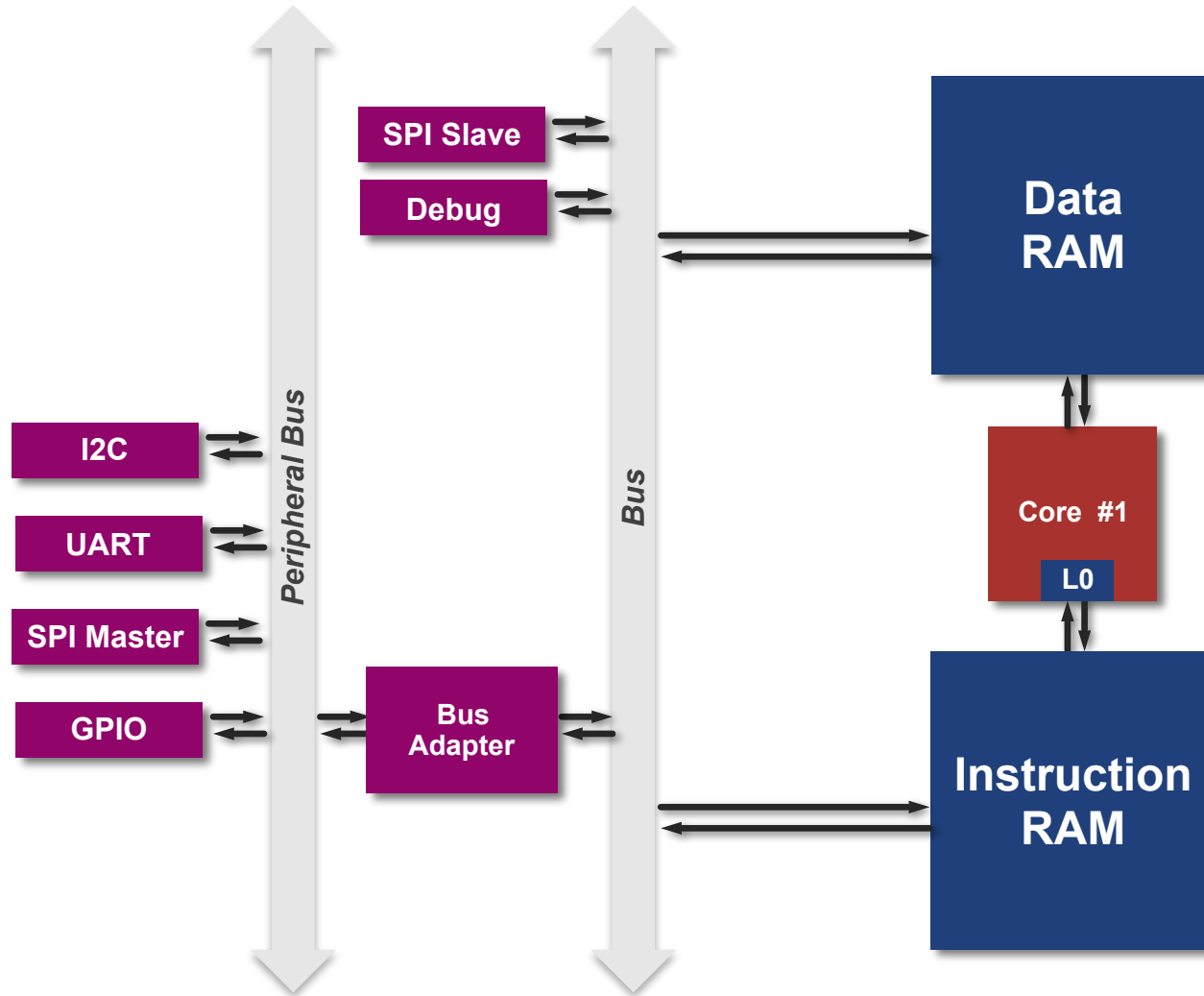




# Parallel Ultra Low Power Platform



# PULPino



# Current State

- RV32ICM + custom instructions
  - Hardware-loops
  - Post-incrementing load and stores
  - SIMD
- Patch for RISC-V toolchain
  - Built-ins for SIMD
  - Infers instructions
- 10x efficiency increase
- Support for **all** targets:
  - RTL simulation
  - FPGA mapping
  - Virtual platform
  - ASIC
- Silicon proven core
- 3.19 Coremark/MHz
- 1.2 DMIPS/MHz

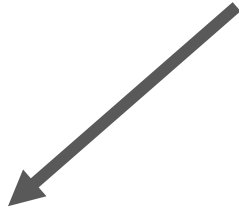




# PULP

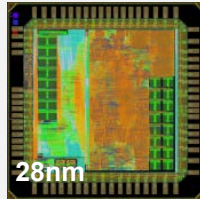
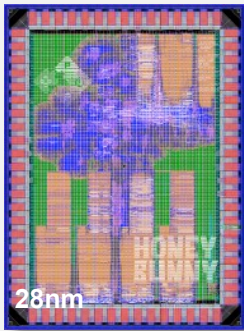


# PULP



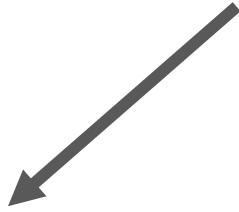
## Multicore Cluster

- PULP
- Research



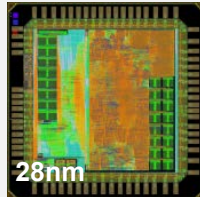
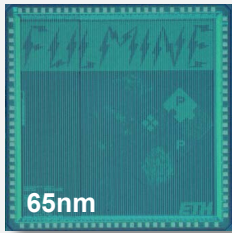
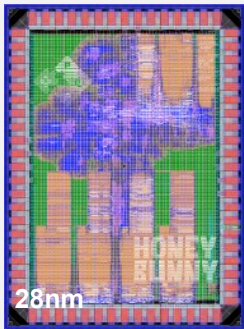


# PULP



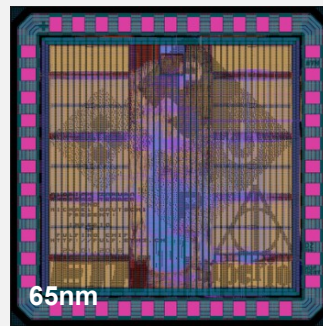
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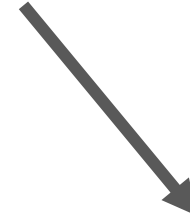
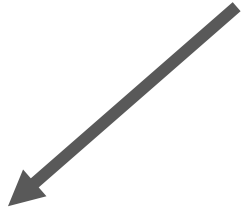
## Standalone µC

- PULPino
- Ease of use



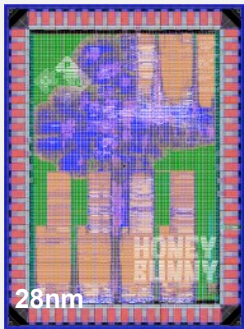


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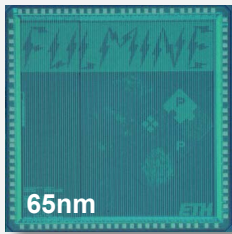


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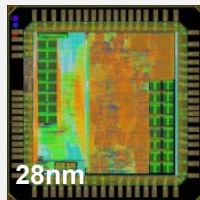
- PULP
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28nm



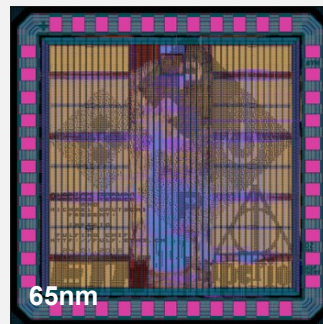
65nm



28nm

## Standalone µC

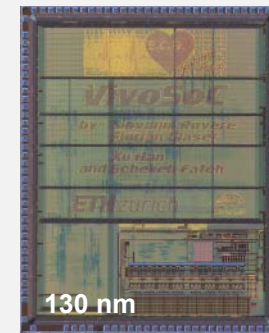
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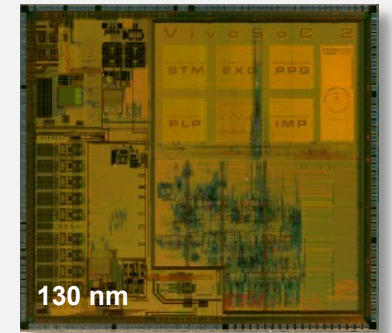
65nm

## Mixed signal

- VivoSoC
- Healthcare



130 nm



130 nm

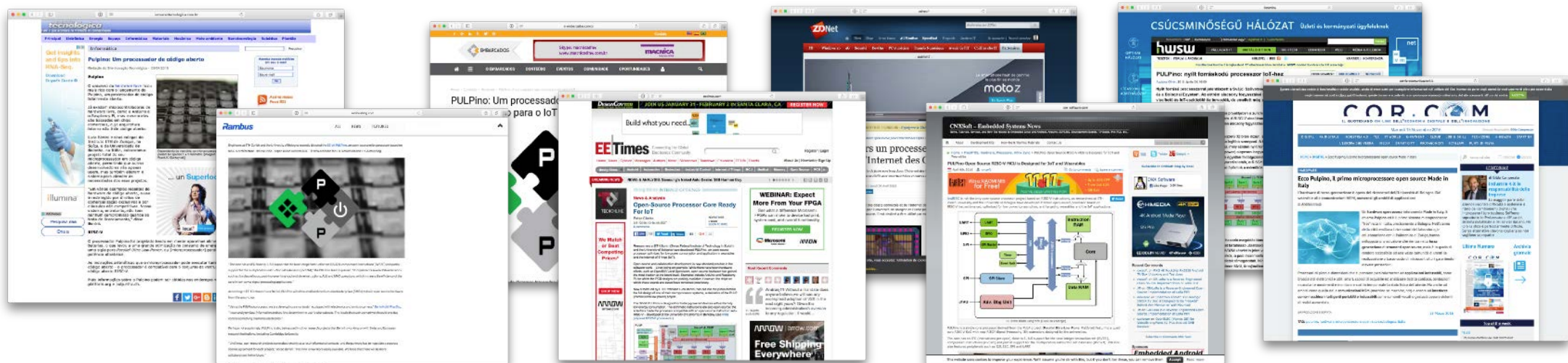
# Open Sourcing PULPino

- We open sourced PULPino on 1<sup>st</sup> March 2016...
- ... and got fantastic media coverage
- Over 15,000 users visited our website
- More than 600 unique clones on GitHub
- Over 20 companies and research institutes use PULPino



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# Future of PULPino (PULPino V2)

- Continue this success
- **PULPino V2:**
  - Support for Verilator simulation
  - IP-XACT description
  - New peripherals ( $\mu$ DMA)
  - New, streamlined event unit
  - SDK
  - Updated compiler
  - Improved documentation and tutorials

- 1 March 2016**  
First release of PULPino
- 2 May 2016**  
Toolchain for our modified RISC-V implementation
- 3 May 2016**  
DSP oriented extensions
- 4 Q1 2017**  
PULPino V2
- 5 Late 2017**  
PULPino V3, Virtual platform (ISS)

# Future Efforts

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## Privileged ISA

- Secure PULPino, MMU
- Sel4 OS



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## < 10 kGE RISC-V

- RV32 IC
- 1 & 3 stage pipeline



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## < 10 kGE RISC-V

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## Heterogeneous configuration

- FPU
- Accelerators



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## Check us out on:



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[https://twitter.com/pulp\\_platform](https://twitter.com/pulp_platform)



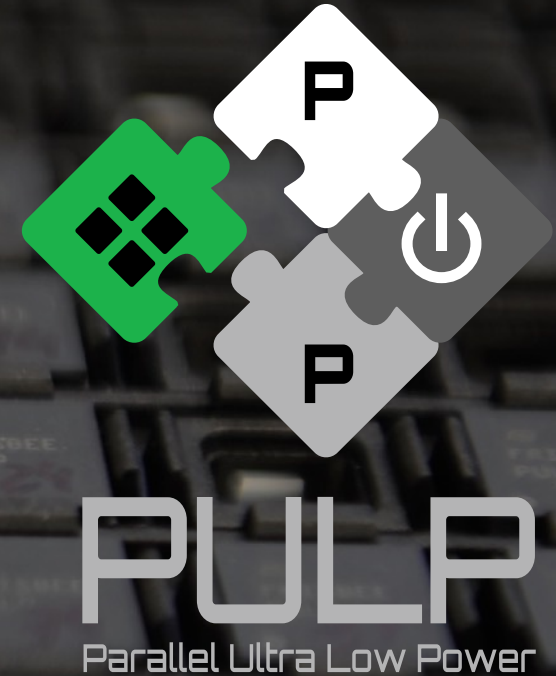
<http://www.pulp-platform.org>



# Questions?

[www.pulp-platform.org](http://www.pulp-platform.org)

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