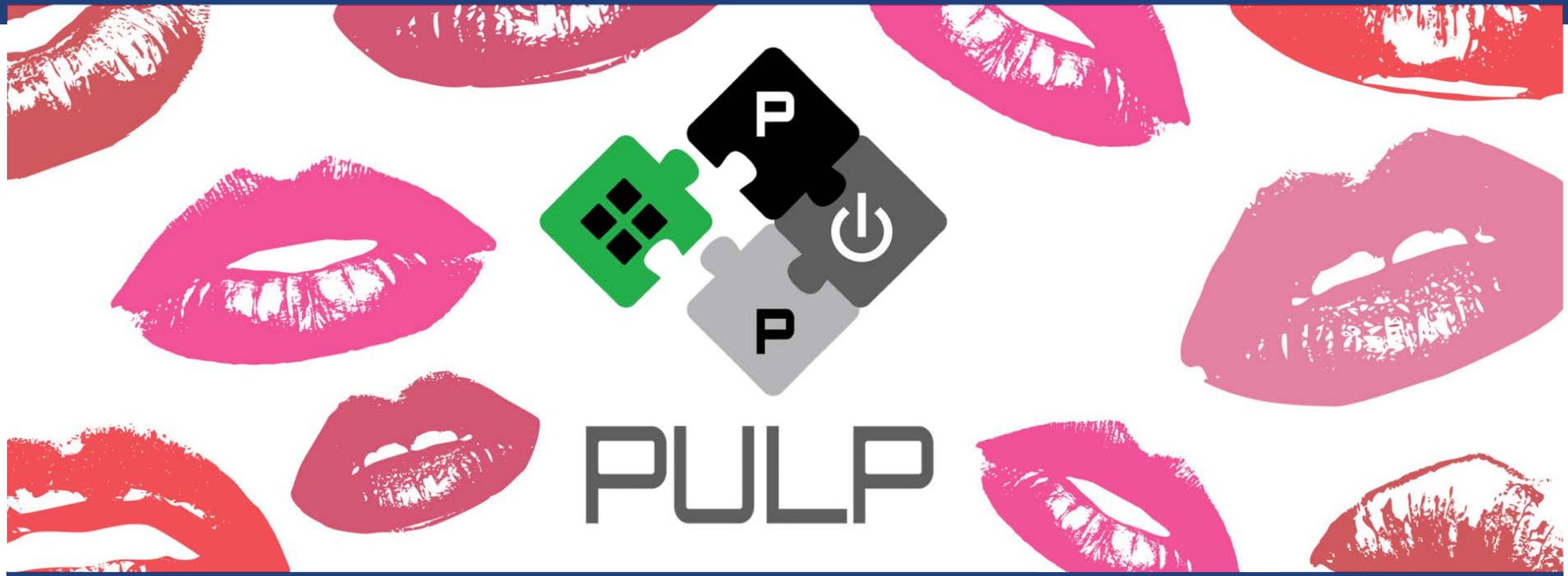
KISS PULPino - Updates on PULPino

updates on PULPino

ETH zürich | ALMA MATER STUDIORUM UNIVERSITÀ DI BOLOGNA

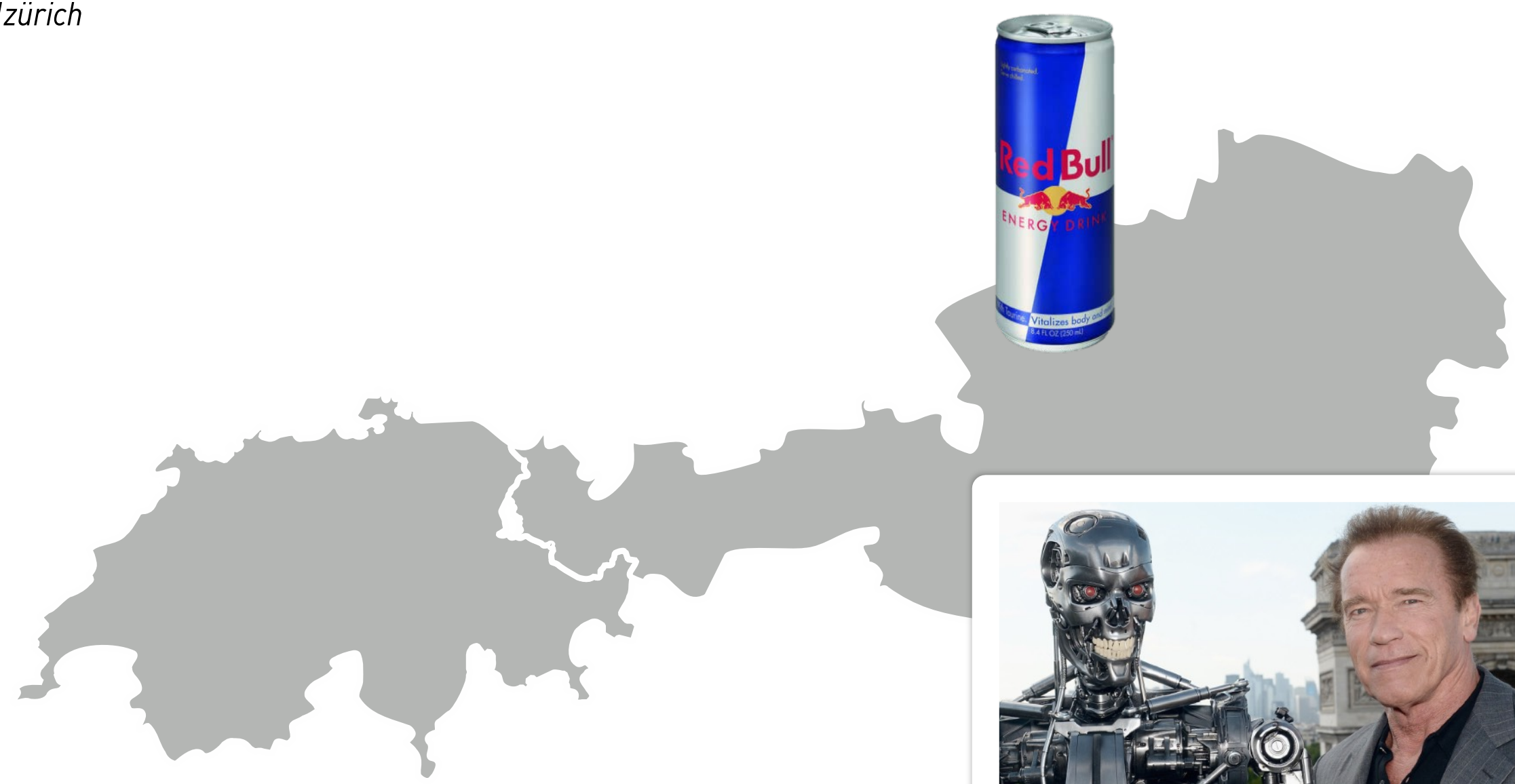


KISS PULPino
Updates on PULPino

5th RISC-V Workshop, Mountain View (California), Florian Zaruba

ETH zürich


Red Bull
ENERGY DRINK
Vitalizes body and
8.4 FL OZ (250 mL)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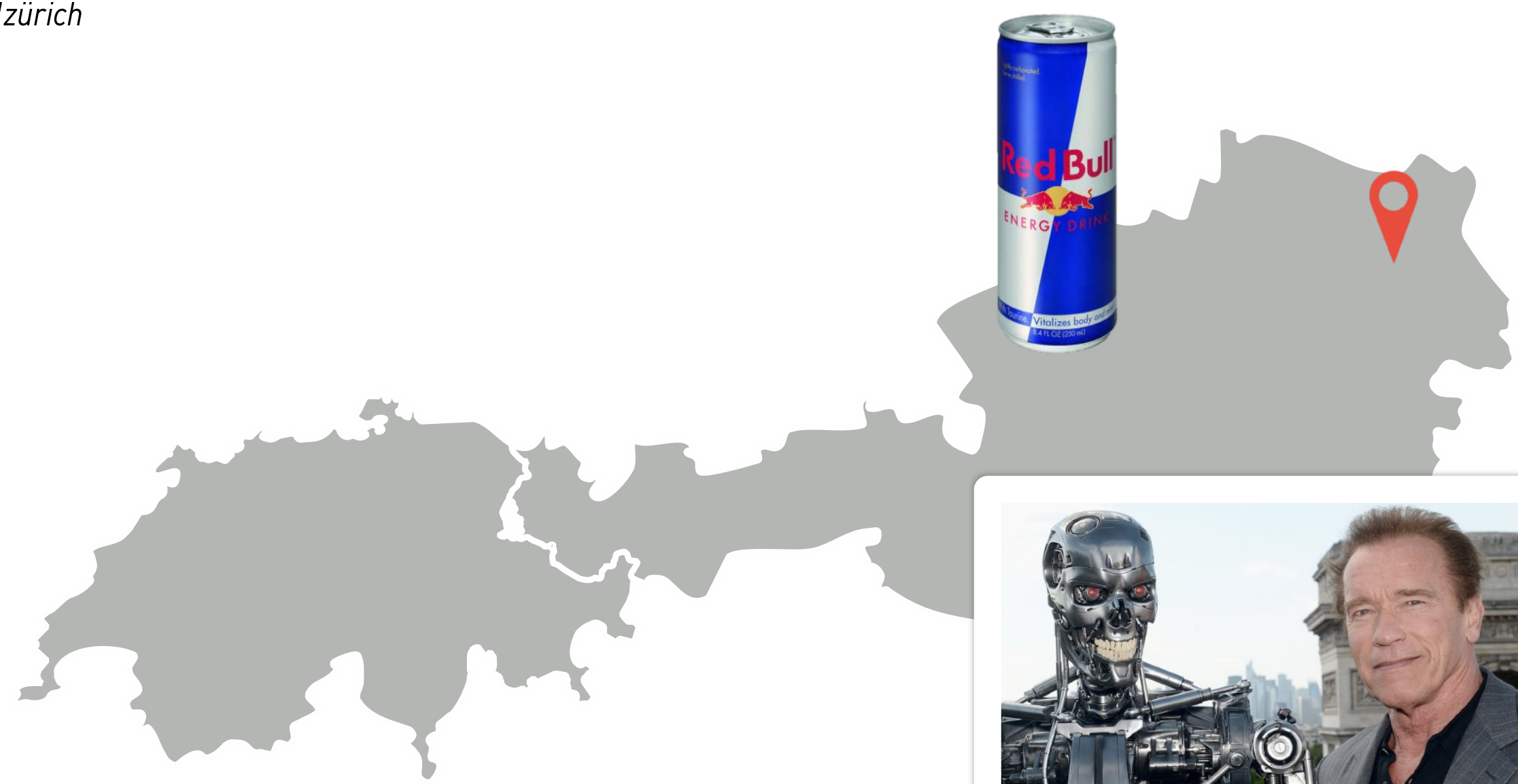
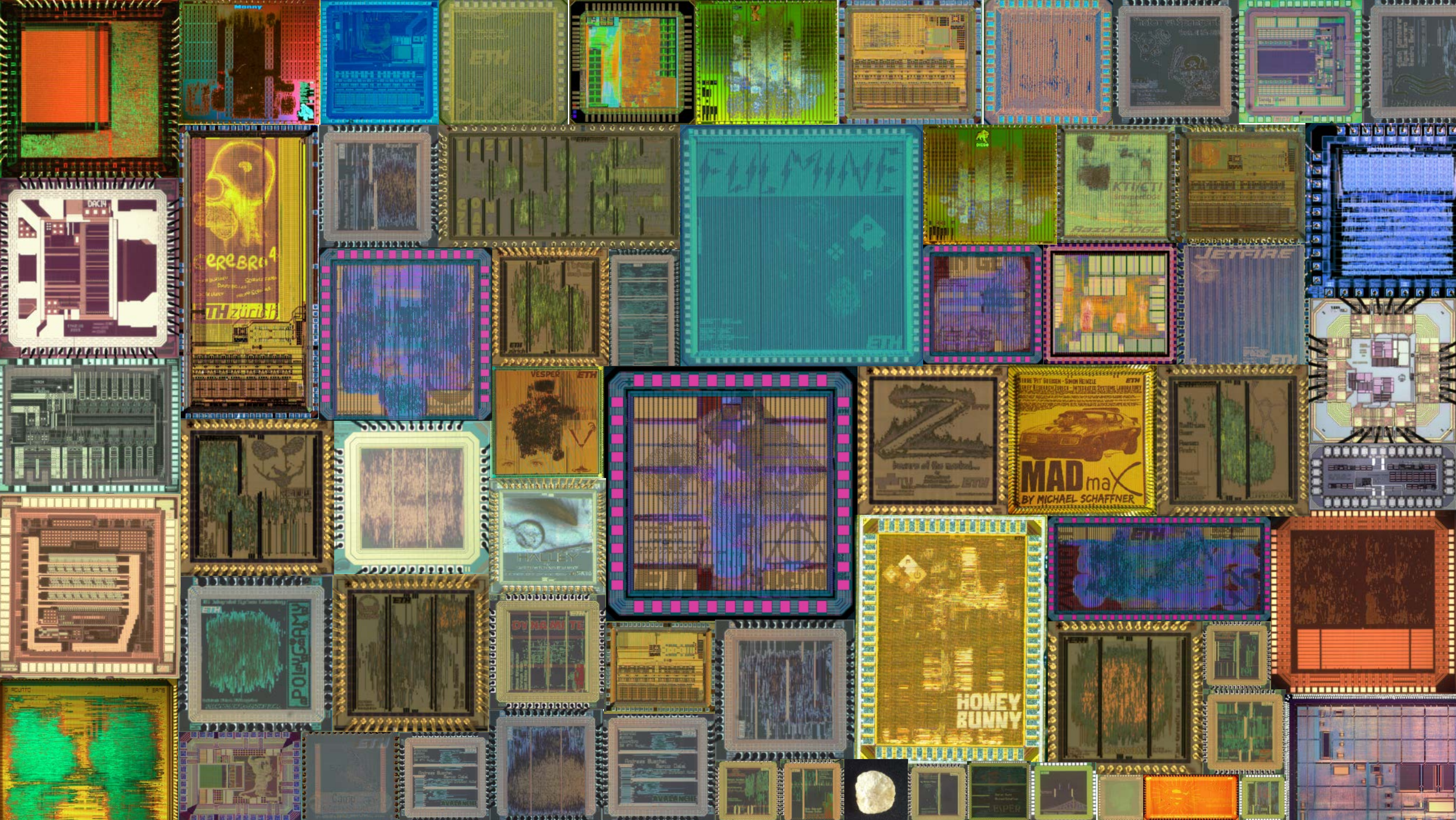

Red Bull
ENERGY DRINK
Vitalizes body and


25

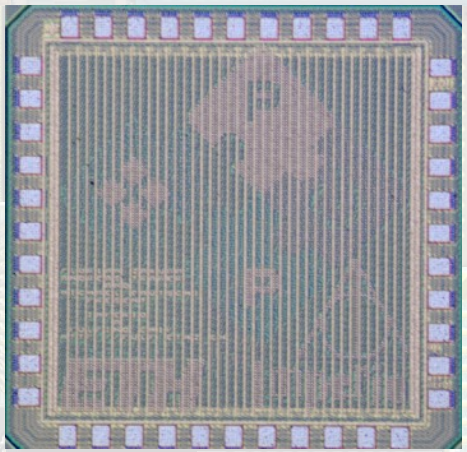

Red Bull
ENERGY DRINK

TOBLERONE
SWISS MILK CHOCOLATE WITH HONEY & ALMOND NOUGAT
OF SWITZERLAND


FULMINE
MAD max
BY MICHAEL SCHAFFNER
HONEY BUNNY
VESPER
HALLEY
DYNAMITE
JETFIRE
ETH

Imperio

- **First** ASIC of PULPino (UMC 65)
- Complete µC (RV32IMC)
- Integrated FLL
- **Speed**: 500 MHz
- Peripherals:
  - 19 GPIOs, UART, I2C, SPI
  - JTAG Debug Interface
- 64 kB RAM

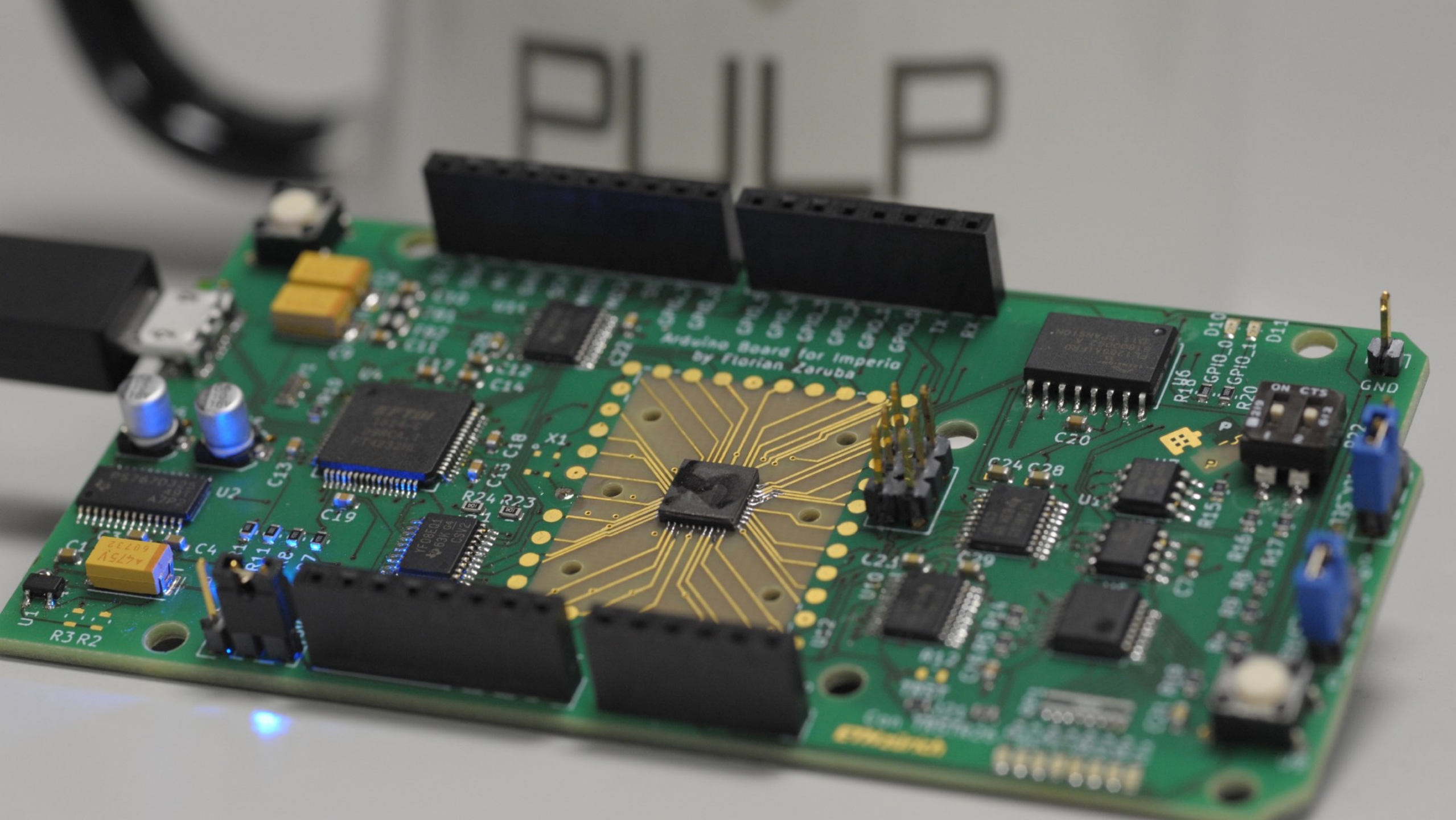


- **Operating Voltage:**
  - 0.9 – 1.2 V
- **Dynamic Power:**
  - 14 – 71 µW/MHz, 1.2 V
  - 3 – 15 µW/MHz, 0.9 V
- **Leakage**: 150 µW
- **Area**:
  - 700 kGE* (SoC)
  - 40 kGE* (Core)

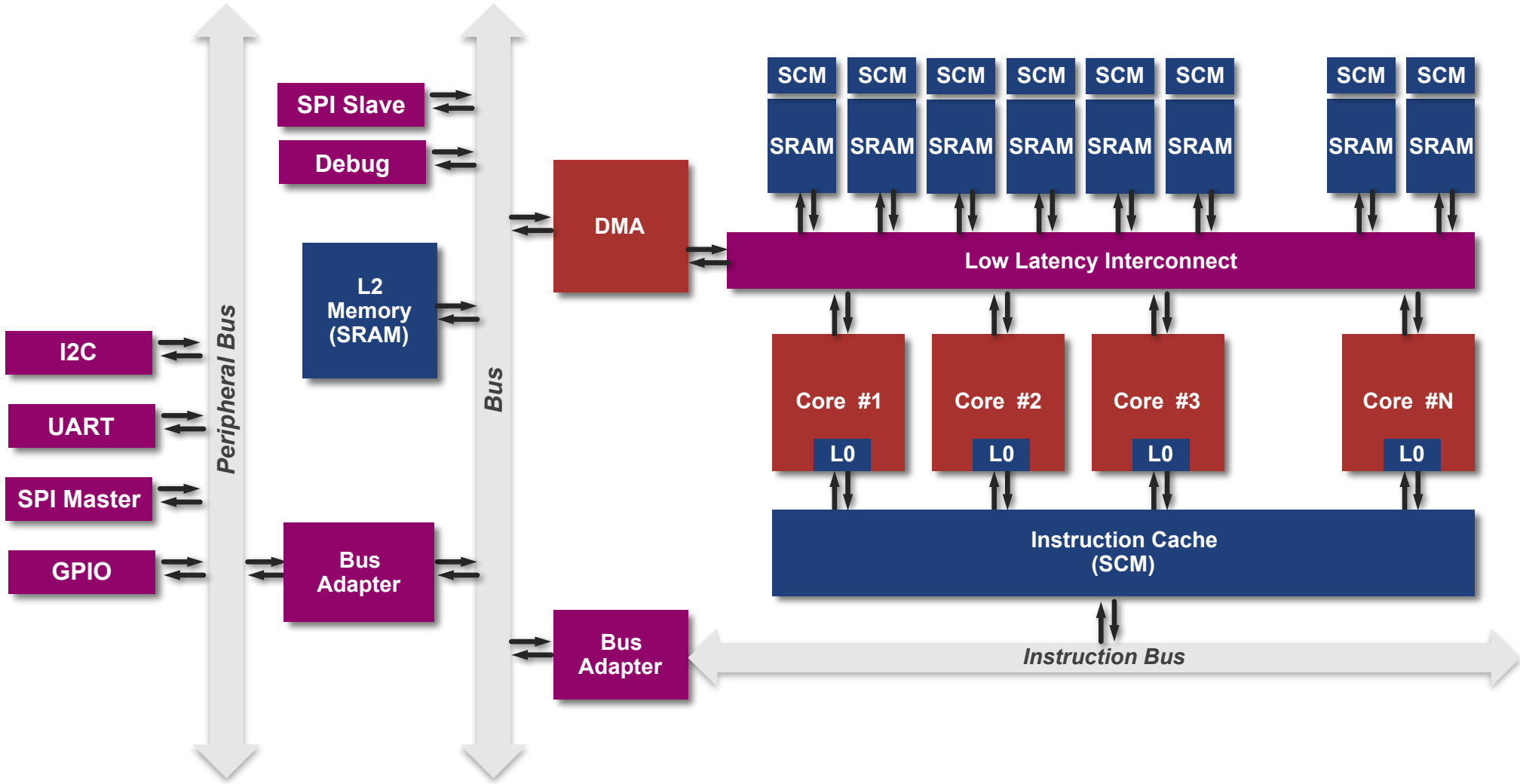
ETH ASIC Gallery: http://asic.ethz.ch/

* 1 kGE = 1.44 µm²

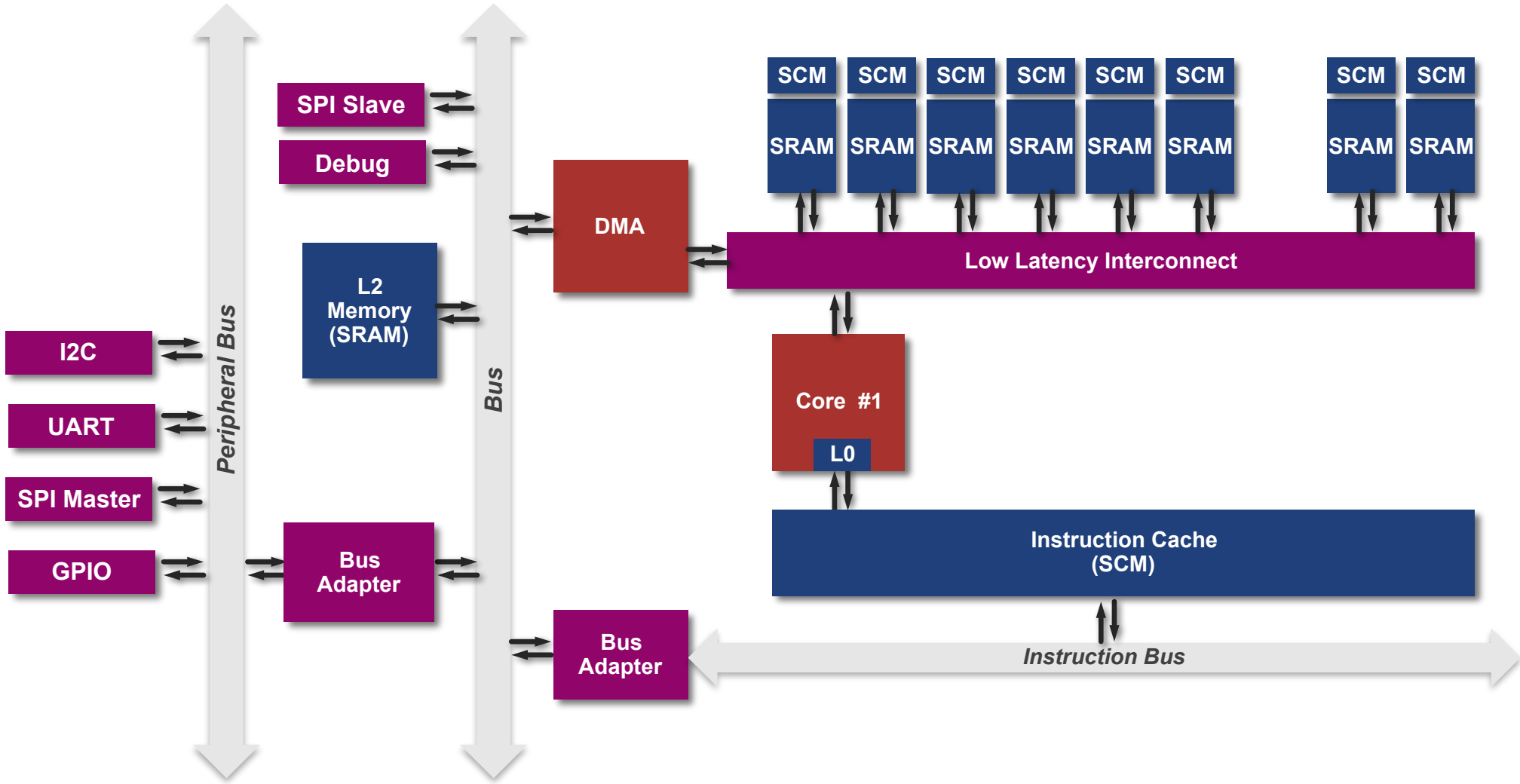

PRECISION TEMPERATURE FORCING SYSTEM
MANUAL CONTROL SCREEN
HOT
AMB
COLD
COLD
COLD
HEAD
FILE
GRAPH
HELP
MENU


PULP
Arduino Board for Imperio
by Florian Zaruba
GND
GPIO_0
GPIO_1
ON
CTS

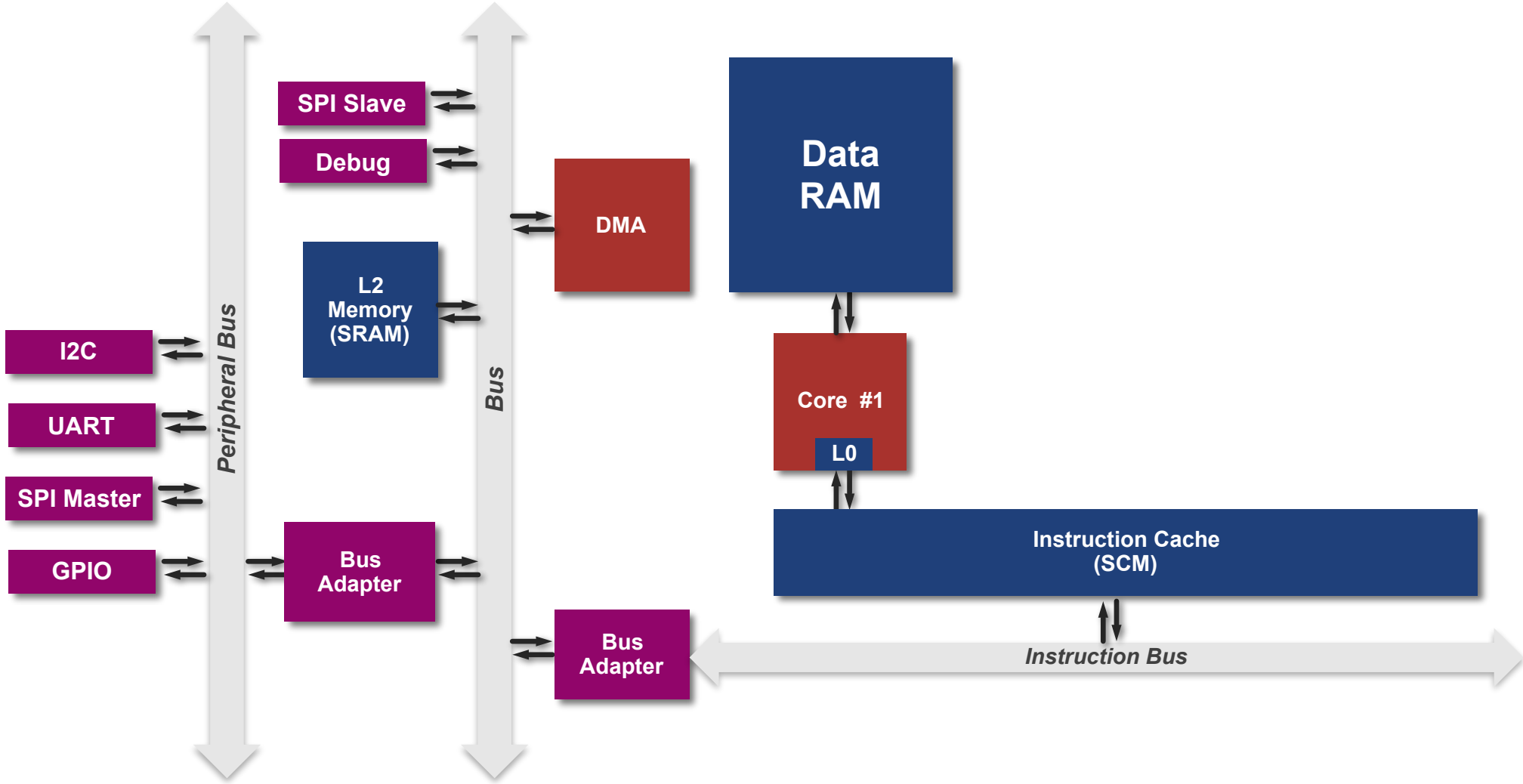
Parallel Ultra Low Power Platform



Parallel Ultra Low Power Platform



Parallel Ultra Low Power Platform



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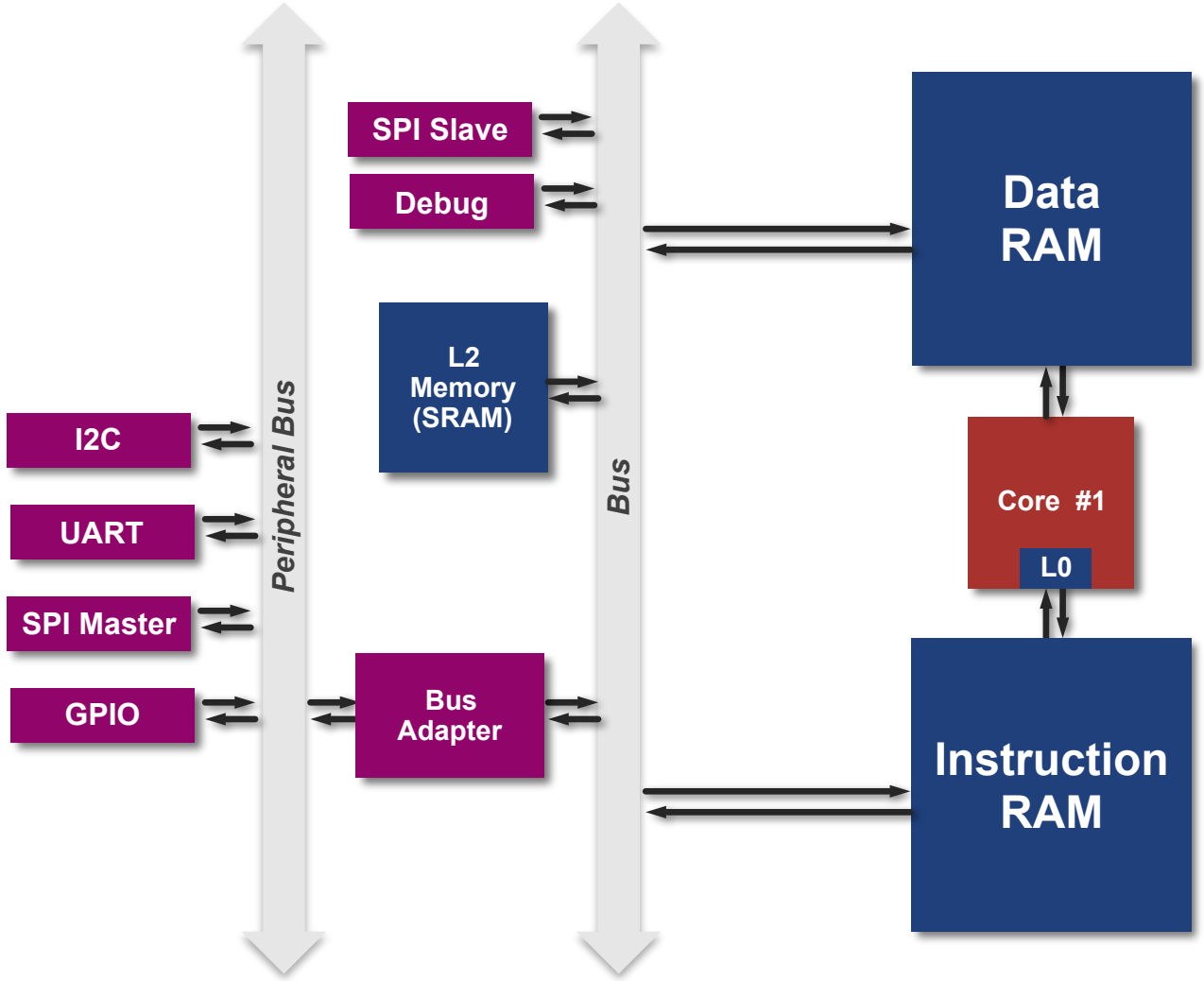
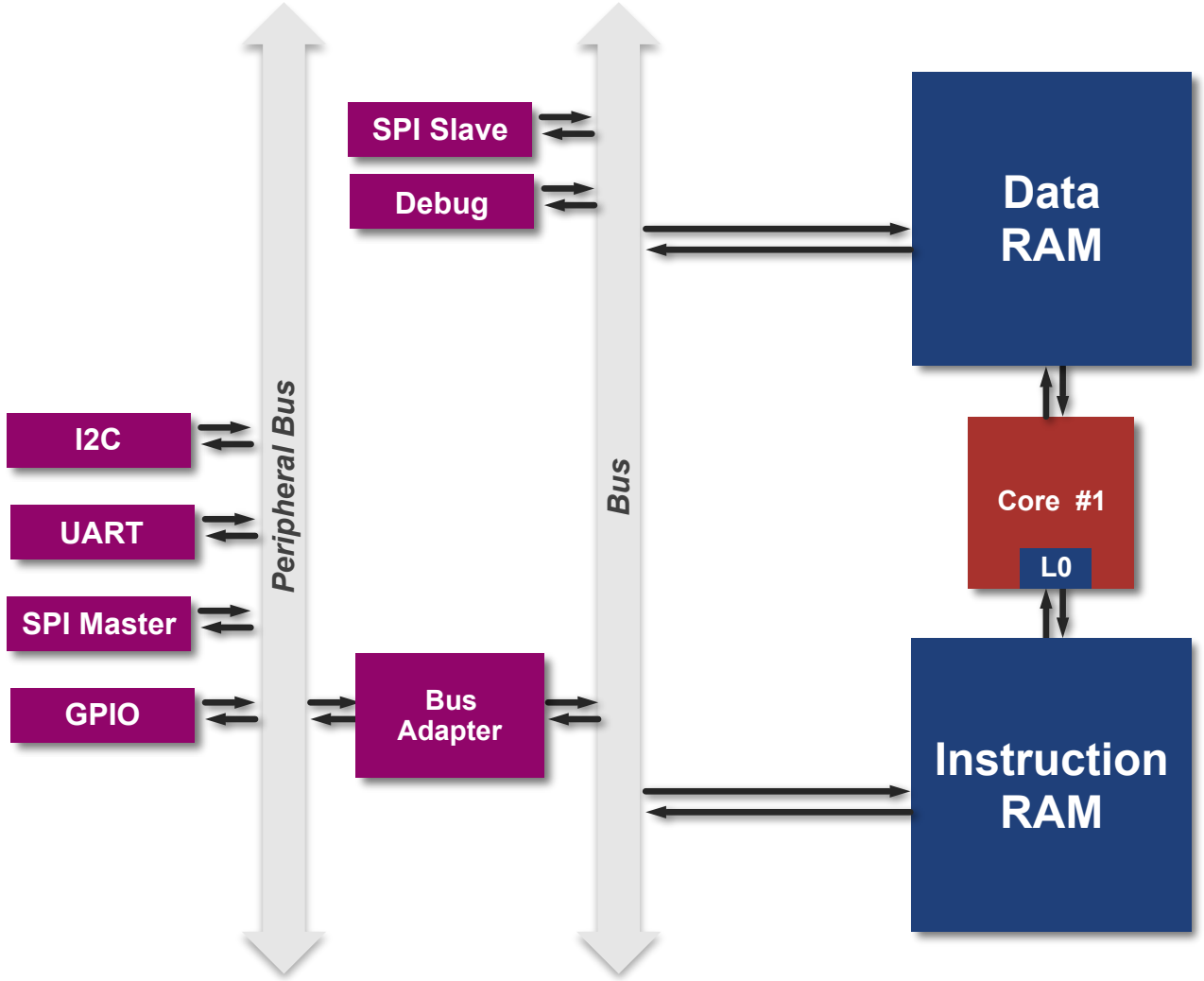


PULPino


SPI Slave
Debug
Data RAM
I2C
UART
SPI Master
GPIO
Peripheral Bus
Bus
Core #1
L0
Bus Adapter
Instruction RAM

Current State

- RV32ICM + custom instructions
  - Hardware-loops
  - Post-incrementing load and stores
  - SIMD
- Patch for RISC-V toolchain
  - Built-ins for SIMD
  - Infers instructions
- 10x efficiency increase

- Support for **all** targets:
  - RTL simulation
  - FPGA mapping
  - Virtual platform
  - ASIC
- Silicon proven core
- 3.19 Coremark/MHz
- 1.2 DMIPS/MHz

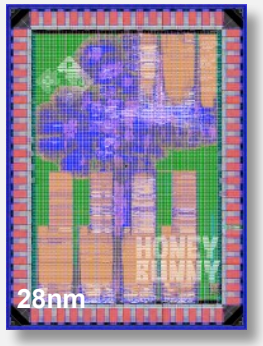
PULP

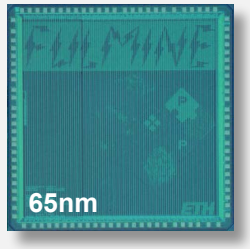

PULP

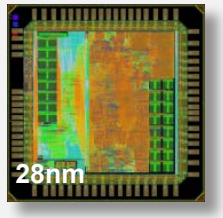
PULP

Multicore Cluster

- PULP
- Research







PULP

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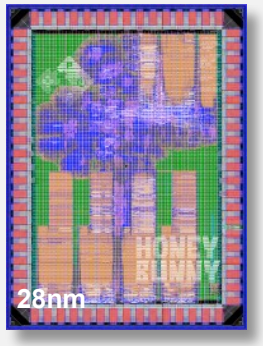
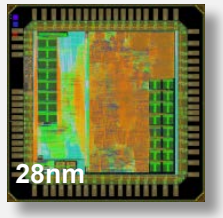
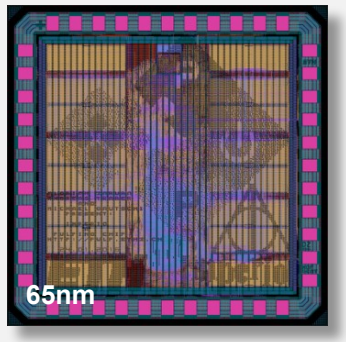




Standalone µC

- PULPino
- Ease of use



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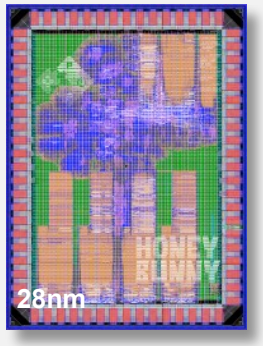

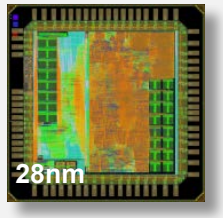

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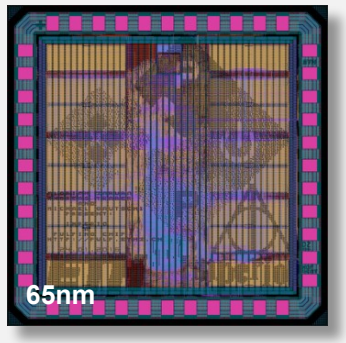
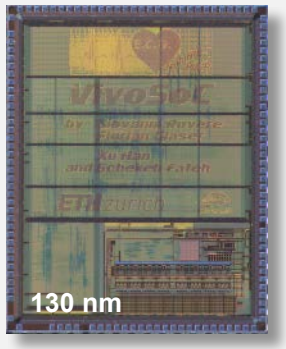
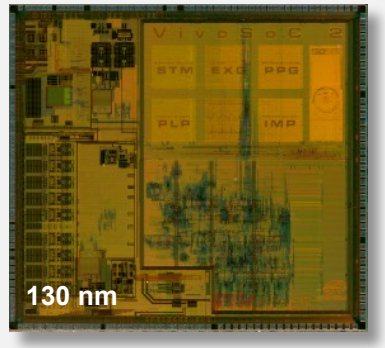


Mixed signal

- VivoSoC
- Healthcare





Open Sourcing PULPino

- We open sourced PULPino on 1st March 2016…
- … and got fantastic media coverage
- Over 15,000 users visited our website
- More than 600 unique clones on GitHub
- Over 20 companies and research institutes use PULPino

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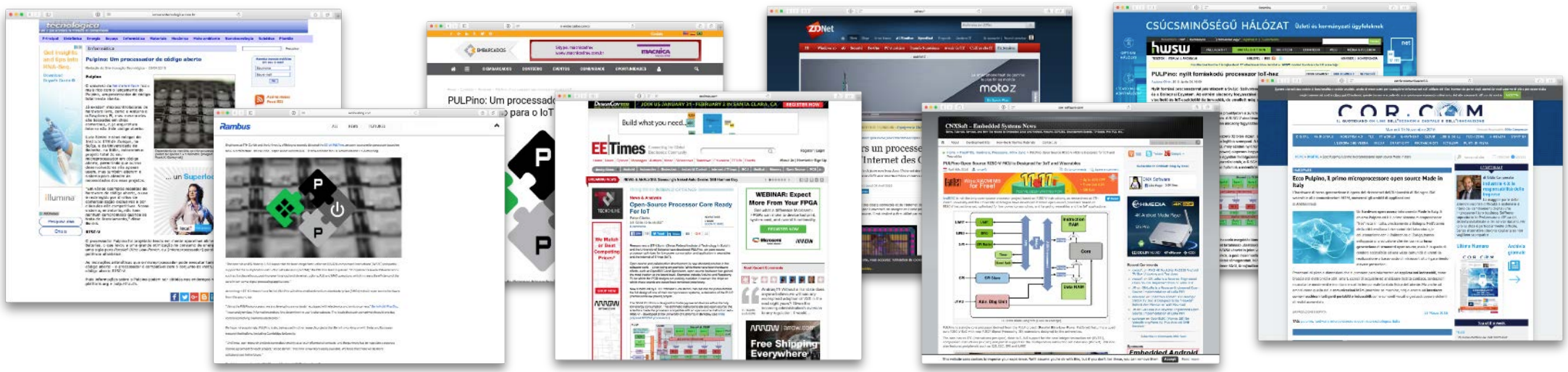

Future of PULPino (PULPino V2)

- Continue this success
- **PULPino V2**:
  - Support for Verilator simulation
  - IP-XACT description
  - New peripherals (µDMA)
  - New, streamlined event unit
  - SDK
  - Updated compiler
  - Improved documentation and tutorials

1 **March 2016**
First release of PULPino

2 **May 2016**
Toolchain for our modified RISC-V implementation

3 **May 2016**
DSP oriented extensions

4 **Q1 2017**
PULPino V2

5 **Late 2017**
PULPino V3, Virtual platform (ISS)

Future Efforts

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Privileged ISA

- Secure PULPino, MMU
- Sel4 OS

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< 10 kGE RISC-V

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- 1 & 3 stage pipeline

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Heterogeneous configuration

- FPU
- Accelerators

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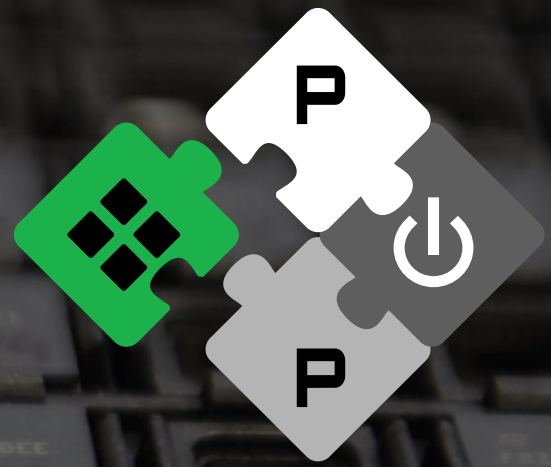
Questions?

www.pulp-platform.org



PULP

Parallel Ultra Low Power

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[1]Department of Electrical, Electronic and Information Engineering

ETH zürich

[2]Integrated Systems Laboratory