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Medium Voltage AC-DC Converter Systems for Ultra-Fast Charging Stations for Electric Vehicles

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Abstract

The environmental impact of petroleum-based transportation infrastructure gained more and more significance during the last decade as fossil fuel powered vehicles lead to high emissions of CO_2 and other greenhouse gases. With the electric mobility becoming a real solution for a sustainable future by using renewable energy sources, the emissions of carbon and in general greenhouse gases can be substantially reduced in order to mitigate the induced ecological effects.

For today's electric vehicles already featuring suitable (but limited) ranges and having advantages over vehicles driven by internal combustion engines as higher engine efficiency, regenerative braking and reduced noise emission, the key element for their success are the charging systems as well as the battery technology. To overcome the range limitations given through the long charging times so-called ultra-fast charging stations have to be developed with a charging power of several 100 kW preferably connected to the medium voltage AC grid which substantially increase the autonomy and the flexibility of electric vehicle drivers.

After presenting a brief motivation for the topic of the electric mobility in **Chapter 1** together with today's charging methods as well as available charging infrastructure, state-of-the-art research approaches for an ultra-fast charging station for electric vehicles with integrated energy storages are summarized.

In **Chapter 2** the design aspects for an ultra-fast charging station are given from which concepts for the realization are developed and the specifications and requirements for the power electronic converter system and the energy storage can be stated.

Then, state-of-the-art medium voltage bidirectional isolated AC-DC converter topologies suitable for the grid interface of an ultra-fast charging station are evaluated in **Chapter 3** with the focus set on the integration of a battery energy storage system as well as the integration of the galvanic isolation on module level from which two single-stage converter systems are identified for a further investigation.

The first converter system is the cascaded AC-DC dual active bridge converter for a split battery energy storage system proposed in **Chapter 4**. For the topology, suitable modulation and control schemes both on module as well as on system level are developed and a hardware prototype of a module is designed and built to experimentally verify the proposed modulation schemes. The overall battery energy storage system is simulated to validate the given theoretical analysis.

The second converter system is the cascaded AC-DC multi-port converter for a split battery energy storage system introduced in **Chapter 5**. For a three-phase AC-DC multi-port converter module, a new modeling approach for the power flows at the AC and the DC ports is presented and suitable modulation schemes are developed. Moreover, the converter module is simulated applying the different modulation schemes to validate the given theoretical analysis.

For the comparison of the proposed single-stage converter systems on module level to the state-of-the-art two-stage solution utilizing an AC-DC H-bridge module connected to a DC-DC dual active bridge converter in terms of efficiency and power density, a multi-objective optimization is implemented and the underlying power component models are described in **Chapter 6**. From the optimization results obtained the efficiencies achieved at a power density of 2.5 kW/L are for the single-stage AC-DC dual active bridge module 96.6 %, for the single-stage AC-DC multi-port module 93.5 % and for the two-stage AC-DC H-bridge module connected to a DC-DC dual active bridge converter 97.1 %.

Finally, **Chapter 7** summarizes and concludes the main achievements of the thesis and presents an outlook on possible future research work.

Kurzfassung

Im letzten Jahrzehnt gewannen die Auswirkungen der auf Erdöl basierten Transportinfrastruktur auf die Umwelt mehr und mehr an Bedeutung. Fahrzeuge betrieben mit fossilen Brennstoffen führen zu hohen Emissionen von CO_2 und weiteren Treibhausgasen. Mit der Elektromobilität eröffnen sich Möglichkeiten für eine nachhaltige Zukunft durch den Einsatz erneuerbarer Energiequellen, um die Emissionen von Kohlenstoff und im Allgemeinen von Treibhausgasen wesentlich reduzieren zu können.

Heutige Elektrofahrzeuge verfügen bereits über eine angemessene wenn auch eingeschränkte Reichweite und bieten einige Vorteile gegenüber Fahrzeugen mit Verbrennungsmotoren wie eine höhere Motoreffizienz, das regenerative Bremsen sowie die reduzierte Geräuschemission. Das Schlüsselelement für den Erfolg sind die Ladesysteme sowie die Batterietechnologie. Um die Limitierung der Reichweite durch die langen Ladezeiten zu überwinden, müssen Schnellladestationen mit einer Ladeleistung von einigen 100 kW, vorzugsweise für den Anschluss an das AC Mittelspannungsnetz, entwickelt werden. Somit können die Autonomie und die Flexibilität der Benutzer von Elektrofahrzeugen gesteigert werden.

Nach einer kurzen Motivation zum Thema Elektromobilität in **Kapitel 1** mit ihren heutigen Lademethoden sowie der vorhandenen Ladeinfrastruktur, werden aktuelle Forschungsansätze für eine Schnellladestation für Elektrofahrzeuge mit integriertem Energiespeicher vorgestellt.
In **Kapitel 2** werden die Designaspekte für eine Schnellladestation diskutiert, mit Hilfe derer Realisierungskonzepte erarbeitet und die Spezifikationen und Anforderungen an das leistungselektronische Konvertersystem und den Energiespeicher aufgestellt werden können.
Danach werden in **Kapitel 3** bidirektionale isolierte AC-DC Konvertertopologien für die Mittelspannungsanbindung gemäss dem Stand der Technik hinsichtlich der Verwendung in einer Schnellladestation evaluiert mit dem Fokus der Integration eines Batteriespeichersystems sowie der Integration der galvanischen Trennung auf Modulebene. Zur weiteren Betrachtung werden zwei einstufige Konvertersysteme identifiziert.

Das erste Konvertersystem stellt den kaskadierten AC-DC Dual Active Bridge Konverter für ein gesplittetes Batteriespeichersystem vorgeschlagen in **Kapitel 4** dar. Für die Topologie werden geeignete Modulations- und Steuerverfahren auf Modul- sowie Systemebene entwickelt, welche mittels dem Design und Aufbau eines Hardwareprototyps experimentell verifiziert werden. Zudem wird das gesamte Batteriespeichersystem simuliert, um die theoretische Analyse zu validieren.

Das zweite Konvertersystem stellt den kaskadierten AC-DC Multi-Port Konverter für ein gesplittetes Batteriespeichersystem eingeführt in **Kapitel 5** dar. Für ein dreiphasiges AC-DC Multi-Port Konvertermodul werden ein neuer Modellierungsansatz für die Leistungsflüsse an den AC und DC Ports beschrieben sowie geeignete Modulationsverfahren entwickelt. Des Weiteren wird ein Konvertermodul zur Verifikation der theoretischen Analyse der verschiedenen Modulationsverfahren simuliert.

Zum Vergleich der vorgeschlagenen einstufigen Konvertersysteme auf Modulebene mit dem zweistufigen Ansatz der Stand der Technik bestehend aus einem AC-DC Vollbrückenmodul verbunden mit einem DC-DC Dual Active Bridge Konverter hinsichtlich Effizienz und Leistungsdichte wird in **Kapitel 6** eine mehrkriterielle Optimierung implementiert sowie die zugrundeliegenden Modelle der Leistungskomponenten erläutert. Anhand der Resultate der Optimierung kann bei einer Leistungsdichte von 2.5 kW/L mit dem einstufigen AC-DC Dual Active Bridge Konvertermodul eine Effizienz von 96.6 %, mit dem einstufigen AC-DC Multi-Port Konvertermodul eine Effizienz von 93.5 % und mit dem zweistufigen AC-DC Vollbrückenmodul verbunden mit einem DC-DC Dual Active Bridge Konverter eine Effizienz von 97.1 % erreicht werden.

Abschliessend werden in **Kapitel 7** die wichtigsten Errungenschaften dieser Arbeit zusammengefasst und ein Ausblick auf mögliche zukünftige Forschungsthemen gegeben.

Glossary

Abbreviations

2D	...	Two Dimensional
3D	...	Three Dimensional
AC	...	Alternating Current
CHAdeMO	...	Charge de Move
CHB	...	Cascaded H-Bridge Converter
CSPI	...	Cooling System Performance Index
DAB	...	Dual Active Bridge
DC	...	Direct Current
DFB	...	Dual Full-Bridge
DHB	...	Dual Half-Bridge
DUT	...	Device Under Test
EMI	...	Electromagnetic Interference
EPR	...	Equivalent Parallel Resistance
ESL	...	Equivalent Series Inductance
ESR	...	Equivalent Series Resistance
EV	...	Electric Vehicle
FEM	...	Finite Element Method
FET	...	Field-Effect Transistor
FPGA	...	Field-Programmable Gate Array
HVDC	...	High Voltage Direct Current
IEC	...	International Electrotechnical Commission
IGBT	...	Insulated-Gate Bipolar Transistor
iGSE	...	Improved Generalized Steinmetz Equation
IT	...	Isolé Terre
LUT	...	Lookup Table
LV	...	Low Voltage
MF	...	Medium Frequency
MMC	...	Modular Multilevel Converter
MOSFET	...	Metal-Oxide-Semiconductor Field-Effect Transistor
MV	...	Medium Voltage

NEDC	...	New European Driving Cycle
NPC	...	Neutral Point Clamped
OSG	...	Orthogonal System Generator
PCB	...	Printed Circuit Board
PF	...	Power Factor
PFC	...	Power Factor Correction
PLL	...	Phase-Locked Loop
PRC	...	Parallel Resonant Converter
PWM	...	Pulse Width Modulation
RMS	...	Root Mean Square
SOC	...	State of Charge
SOGI	...	Second Order Generalized Integrator
SRC	...	Series Resonant Converter
SST	...	Solid State Transformer
STATCOM	...	Static Synchronous Compensator
THD	...	Total Harmonic Distortion
V2G	...	Vehicle to Grid
VHDL	...	Very High Speed Integrated Circuit Hardware Description Language
ZCS	...	Zero Current Switching
ZVS	...	Zero Voltage Switching

Mathematical notation

x	...	Instantaneous value of x
X	...	RMS or DC value of x
$\hat{X}$	...	Peak value of x
$\underline{X}$	...	Complex phasor $Ae^{j\phi}$ of $x = A\cos(\omega t + \phi)$
$\overline{\underline{X}}$	...	Complex conjugate of phasor $\underline{X}$
X^*	...	Reference RMS or DC value of x
$\hat{X}^*$	...	Reference peak value of x
x'	...	x referred to the primary or the AC side of a transformer
$x_{\mathrm{b}i}$	...	Value of x belonging to a module i in phase b

Table of Contents

1 Introduction 1
- 1.1 Motivation 1
- 1.2 Objectives and contributions 8
- 1.3 Outline of the thesis 10
- 1.4 List of publications 12

2 Ultra-Fast Charging Station for Medium Voltage Grids 15
- 2.1 Design aspects 15
  - 2.1.1 Utilization 16
  - 2.1.2 EV battery capacity 16
  - 2.1.3 Charging time 17
  - 2.1.4 Galvanic isolation 18
  - 2.1.5 Summary and discussion 18
- 2.2 Concepts for realization 19
  - 2.2.1 Medium voltage DC bus 20
  - 2.2.2 Integrated battery energy storage 22
  - 2.2.3 Focus of this work 22
- 2.3 Specifications and requirements 23
  - 2.3.1 Charging power 23
  - 2.3.2 Energy storage 25

3 Bidirectional Isolated AC-DC Converter Topologies 27
- 3.1 Non-modular AC-DC topologies 29
  - 3.1.1 Two-stage topologies 30
  - 3.1.2 Single-stage topologies 32
- 3.2 Modular AC-DC topologies 34
  - 3.2.1 Star connection 34
  - 3.2.2 Double star connection 42
  - 3.2.3 Delta connection 47
- 3.3 Topology selection 47
  - 3.3.1 Multilevel converters 48
  - 3.3.2 Phase modularity and scalability 48
  - 3.3.3 Integration of galvanic isolation 49

3.3.4 Single versus double star connection 49
3.3.5 Focus of this work 53

4 Cascaded AC-DC Dual Active Bridge Converter 55
4.1 Converter topology 55
4.1.1 From two-stage to single-stage module 58
4.1.2 AC-DC dual active bridge module topologies . . 58
4.2 Operating principle 61
4.2.1 Module level 61
4.2.2 System level 63
4.3 Module modulation schemes 64
4.3.1 ZCS/ZVS modulation with fixed switching frequency 66
4.3.2 ZVS modulation with variable switching frequency 75
4.4 Converter control 82
4.4.1 Grid and phase PLLs 84
4.4.2 Grid current control 84
4.4.3 Phase SOC balancing 84
4.4.4 Battery SOC balancing 86
4.4.5 Module voltage control 87
4.5 Module design 88
4.5.1 Power components 89
4.5.2 Efficiency calculations 92
4.5.3 Hardware prototype 94
4.5.4 Experimental verification 98
4.6 System simulation 103
4.7 Summary and conclusion 107

5 Cascaded AC-DC Multi-Port Converter 111
5.1 Introduction to multi-port converters 111
5.2 Converter topology 112
5.2.1 Module topology 114
5.2.2 Transformer arrangements 116
5.3 Operating principle 121
5.3.1 Module level 121
5.3.2 System level 123
5.4 Modeling of power flows 124
5.4.1 Power flow between two ports 125
5.4.2 Power flow at AC ports 128
5.5 Module modulation schemes 129

5.5.1 Fundamental phasor modulation 130
5.5.2 ZVS modulation 139
5.5.3 Alternative modulations 148
5.6 Module design 148
5.6.1 Power components 149
5.6.2 Efficiency calculations 154
5.7 Module simulation 156
5.7.1 Fundamental phasor modulation 156
5.7.2 ZVS modulation 160
5.8 Summary and conclusion 164

6 Multi-Objective Optimization and Comparison 167
6.1 Specifications of converter modules 169
6.2 Modeling of power components 173
6.2.1 Semiconductor devices 173
6.2.2 Inductive components 175
6.2.3 Capacitors 186
6.3 Optimization procedure 186
6.3.1 Inductor optimization 192
6.3.2 Transformer optimization 194
6.4 Optimization results 194
6.4.1 AC-DC dual active bridge module 195
6.4.2 AC-DC multi-port module 197
6.4.3 AC-DC H-bridge module with DC-DC dual active bridge 199
6.5 Comparison of converter modules 205
6.6 Summary and conclusion 207

7 Conclusion and Outlook 209
7.1 Summary and conclusion 209
7.2 Outlook 215

A DC-DC Dual Active Bridge Converter 217
A.1 Converter topology 217
A.2 Modulation schemes 218
A.2.1 Phase shift modulation 218
A.2.2 Trapezoidal current mode modulation 219
A.2.3 Triangular current mode modulation 220
A.3 Converter optimization 222
A.3.1 Design example 222

A.3.2 Optimization procedure 224
A.3.3 Optimization results 226

B Loss Models of Power Components 233
B.1 Semiconductor devices 233
B.1.1 IGBT losses 233
B.1.2 MOSFET losses 235
B.1.3 Gate drive losses 236
B.2 Inductive components 237
B.2.1 Winding losses 237
B.2.2 Core losses 242
B.3 Capacitors 243

Bibliography 263

1

Introduction

1.1 Motivation

During the last decade the environmental impact of petroleum-based transportation infrastructure gained more and more significance. Fossil fuel powered vehicles lead to high emissions of CO_2 and other greenhouse gases. The global emission of carbon per year is still growing drastically as depicted in **Fig. 1.1** from 1750 to 2011 with the liquid fuels exhibiting a significant part of over 3000 million tons a year [1].

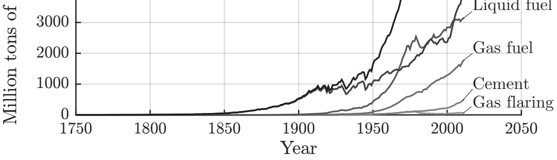

Figure 1.1: Development of the global carbon emission per year given in million tons from 1750 to 2011 [1] originating from gas flaring, cement production as well as gas fuel, liquid fuel and solid fuel consumption.

In order to reduce the emissions of carbon and in general greenhouse gases to mitigate the induced ecological effects, the electric mobility plays an important role in our future transportation infrastructure together with the use of renewable energy sources like hydro power, solar energy or wind power. The electric mobility is becoming a real solution for a sustainable future in combination with the use of renewable energy sources.

Today's electric vehicles (EVs) already feature suitable (but limited) ranges and have advantages over vehicles driven by internal combustion engines as higher engine efficiency, regenerative braking and reduced noise emission. Moreover, EVs can serve as distributed energy storage integrated into the grid for vehicle to grid (V2G) applications in order to provide energy to the grid in times of shortages.

In Switzerland, the number of registered EVs is growing steadily from year to year [13]. **Tab. 1.1** gives a summary of EVs with 4-5 seats available on the market in early 2015 with their range as well as their

Table 1.1: Electric vehicles with 4-5 seats available on the market (early 2015) with their range and battery specifications [2–11]. All of them are using the lithium-ion battery technology.

Model	**Range**[a]	**Battery capacity**	**Battery voltage**[b]
BMW i3	190 km	18.8 kWh	360 V
Fiat 500e	210 km	24 kWh	364 V
Ford Focus Electric	162 km	23 kWh	325 V
Kia Soul EV	212 km	27 kWh	360 V
Mercedes-Benz B-Class Electric	200 km	28 kWh	240 V
Mitsubishi i-MiEV	150 km	16 kWh	330 V
Nissan Leaf	199 km	24 kWh	360 V
Renault Zoe	210 km	22 kWh	400 V
Tesla Model S 70D	442 km	70 kWh	375 V
VW e-Golf	190 km	24.2 kWh	323 V

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[a] The range is given for the New European Driving Cycle (NEDC) set out in UN/ECE Regulation No. 83 for the *Type I test* [12].

[b] Nominal battery voltage.

battery capacity and voltage according to the manufacturers brochures. Most of the available EVs feature ranges of around 200 km given for the New European Driving Cycle (NEDC) which lead to battery capacities of more or less 24 kWh. All of the listed EVs are using the lithium-ion battery technology.

The charging methods for an EV range from a battery swap over inductive up to conductive charging as schematically depicted in **Fig. 1.2**. The battery swap seems to be the simplest solution, at least in theory. In practice it is not beneficial since the manufacturers apply different batteries with different specifications depending on the EV model.

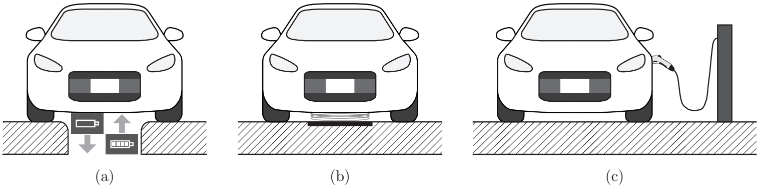

(a) (b) (c)

Figure 1.2: State-of-the-art charging methods for an EV: (a) battery swap, (b) inductive charging, (c) conductive charging with AC or DC current.

The company Better Place founded 2007 in Israel proposed a battery swapping system where an EV driver does not own the battery. The customer is charged a monthly fee for the battery and the electricity based on the driven kilometers comparable to a mobile phone contract [14]. Despite the interest the company gained from various analysts and investors, the business model could not be realized for the EV mass market. The company shut down its business in 2013 [15].

Also Tesla Motors worked on a battery swapping station which allows to change the battery of the Model S in about 90 seconds [16]. The station became operational in January 2015 but is not reaching the popularity as the electric superchargers Tesla provides [17].

In contrast to the mechanical replacement of the EV battery for charging, electric energy can be transferred from a charging station to the EV battery either inductive or conductive. Inductive power transfer (IPT) systems feature a contactless energy transfer from a transmitting coil to a receiving coil based on the operating principle of a transformer. Limiting factors of such systems for EVs are often the required space of the receiver coil in the vehicle as well as the mechanical positioning of the coils in the charging station what strongly influences the transmission efficiency [18]. Moreover, inductive charging involves health risks from the induced electric fields in human tissue so that the magnetic stray field has to be limited.

Besides presented laboratory prototypes of IPT systems for the electric mobility in scientific literature [19,20], various companies are working on inductive charging stations for EVs as for instance Bombardier with their PRIMOVE systems [21], Siemens with their induction-based charging solution SIVETEC CIS [22] as well as many car manufacturers like Audi, BMW and Toyota [23].

The conventional and most popular way of charging an EV battery represents the conductive charging. The IEC 61851-1 standard defines the slow AC charging *mode 1* and *mode 2* from the low voltage (LV) distribution grid with a standard single- or three-phase power outlet with typical phase currents of 16 A and 32 A [24,25]. The AC charging *mode 3* covers slow and fast AC charging from a specific EV socket outlet at an AC charging station either at home or at public places [25]. The currents per phase are typically below 63 A [24]. Besides the AC charging modes the IEC 61851-1 standard defines also the fast DC charging *mode 4* with currents up to 400 A which is derived from the CHAdeMO standard [24–26].

DC fast charging stations and EVs supporting the CHAdeMO standard with a charging power of around 50 kW are already well established on the market. Over 50 % of EVs sold in Europe from 2010 to 2014 are compliant with the CHAdeMO standard [27]. More than 50 different charger manufacturers as for instance ABB, Fuji Electric, Hitachi, Schneider or Siemens offer CHAdeMO DC charging stations as a part of their product portfolios for providing energy to EVs of different brands and models [27]. With the CHAdeMO charging system an EV battery can be almost fully charged in 15 to 30 minutes. Depending on the EV model the charging process takes 5 to 10 minutes for a 40 km to 60 km drive. Besides the CHAdeMO charging stations, Tesla Motors develops its own DC superchargers with a charging power up to 120 kW [28]. A 30 minutes charging operation of the Model S equates to a range of about 270 km.

With the available fast charging solutions, the range of fully electric cars is still limited compared to conventional fossil fuel powered cars. Today's classic mid-size diesel cars with seats for 4-5 adults exhibit an average tank capacity of 60 L that allows to travel distances of more than 1000 km [29]. Compared to the EVs available on the market in early 2015 (see **Tab. 1.1**) the range of common diesel cars is about a factor 5 higher.

In order to increase the autonomy and the flexibility of EV drivers, the range limitations given through the long charging times can be mitigated by the development of so-called ultra-fast charging stations. Such stations would be able to charge an EV battery with charging rates up to 5 kWh/min, so that a charging time of 5 minutes equates to a range of about 200 km. These systems can be placed at key nodes in the road traffic network to provide electricity to the EV drivers faster than the conventional charging infrastructure. The required charging power for ultra-fast charging lies in the range of several 100 kW given by the target charging rate which is supplied by high power electronic converter systems preferably connected to the medium voltage (MV) grid.

State-of-the-art high power charging systems exist for electric buses as for example the eBus system from Siemens [30] with a charging power up to 450 kW which is connected to the LV or the MV grid. The off-board charging station consists of a structural mast for an inversely mounted pantograph where the bus is charged in 6 to 8 minutes depending on the state of charge (SOC) of the battery.

The TOSA 2013 bus project in Geneva with the power electronics from ABB applies stationary batteries at the bus stops which are charged with 50 kW power from the LV grid [31]. The batteries of the bus are then charged via a 400 kW high power charger during a 15 seconds discharge of the stationary energy storage. Additionally, at the terminal stop of the bus a charging power of 200 kW is available for a full recharge.

Moreover, Heliox from the Netherlands offers DC ultra-fast charging systems from 120 kW up to 2.5 MW for electric public transport systems running with 700 V [32]. The electric connection is made by a pantograph mounted on the roof of an electric bus.

Besides high power charging solutions for the public transport, the charging power available for the individual EV traffic is still limited. The most public charging stations feature no more than six charging ports with an output power below 150 kW as for example the worldwide supercharger network of Tesla [28], the solar powered Fastned charging network in the Netherlands [33] or the ChargePoint network in the United States [34]. For large-scale charging stations for instance at highways where several EVs have to be charged simultaneously in a reasonable time, the required charging power reaches a few MW. For such systems the connection to the grid has to be done on the MV level since the currents drawn from the LV grid would become too high.

Research in the area of large-scale charging stations is mainly focusing on concepts applying a DC bus where several chargers, energy storage and renewable energy generation can be attached [35–38]. The proposed architecture in [35] consists of a bipolar DC bus which is coupled via an AC-DC converter and a step-down transformer to the MV grid. At the DC bus several fast charging DC-DC converters providing energy to the EVs as well as a battery energy storage system and renewable energy generation from wind and solar power are connected. Furthermore, in [36] a flywheel energy storage system as part of a fast charging station to mitigate the adverse effects of high power charging for the grid is investigated.

The use of energy storage in an ultra-fast charging station is not only useful to flatten the power demand from the grid during charging activities, moreover it is in general beneficial in the context of smart grid applications for the future energy distribution grid due to the increasing integration of renewable energy sources [39]. The inherently fluctuating and stochastic nature of renewable energy sources demands the placement of energy storage as part of the grid in order to ensure balancing supply and demand [40–42].

Besides the well-known energy storage systems using the potential energy of water (pumped hydroelectric storage systems [43]), in recent years additional concepts based on compressed air [43], flywheels [43, 44], thermal energy storage in molten salt [43, 45] as well as electrochemical storage in batteries [43, 44] have been investigated. The battery based systems offer the advantages of a high energy and power density, a high cycle efficiency as well as being location-independent and easily scalable [43]. Such systems also become more and more important in grid applications for load leveling providing fast frequency regulation [46]. In order to store considerable amounts of energy and ensure the dynamic control of power, suitable high power electronic equipment connecting the storage batteries to the grid plays an important role.

State-of-the-art battery energy storage systems at high power levels are usually connected to the MV grid. Because of the comparable high voltage level, multilevel converter systems are advantageous due to lower harmonics and reduced filtering effort, robust operation and reduced switching losses. Furthermore, no bulky transformers providing voltage adaptation are necessary.

Especially modular converter systems as the modular multilevel converter (MMC) [47] as well as the cascaded H-bridge converter (CHB) [48] offer the benefit to easily split and distribute the battery energy storage among several modules [49–51]. The storage battery is either attached directly to the module DC link [51] or connected via a (isolated) DC-DC converter [49].

Moreover, a modular converter system can be easily scaled according to the specified voltage and power levels. To decrease system downtime in case of a failure, a modular approach offers built-in redundancy which can be considered in the converter and control design process [52]. Additionally, by using standard components in each module manufacturing costs can be kept low.

The functionality of a split battery energy storage system connected to the MV grid can be further extended to an ultra-fast charging station based on the MMC or the CHB [53, 54]. For both converter systems bidirectional isolated DC-DC converters connecting the module DC link to the storage battery provide galvanic isolation and voltage adaptation. With the introduced isolation stage the insulation requirements of the battery packs are reduced and their negative rails can be grounded. Moreover, by applying non-isolated DC-DC converters with their outputs paralleled a high charging power for EVs becomes available. The grid-side introduced isolation stage guarantees further the compliance with EV charging standards (see Section 2.1.4).

The split battery energy storage system as an integral part of an ultra-fast charging station for EVs offers considerable potential for this research work. Especially in the field of modular power electronic converter systems, the integration of module-level galvanic isolation opens possibilities for the investigation of single-stage isolated module topologies and the derived overall converter system. **Fig. 1.3** depicts two possibilities of an ultra-fast charging station based on a split battery energy storage system with integrated galvanic isolation on module level. The outputs of the non-isolated DC-DC converters are paralleled, so that a high charging power for the EV battery becomes available.

Besides the evaluation on topology level, modulation and control schemes can be developed considering soft-switching conditions for the general applied semiconductor devices of IGBTs and MOSFETs. Furthermore, top-level control algorithms that ensure balancing the SOCs of the storage batteries in the context of the modular converter system can be studied.

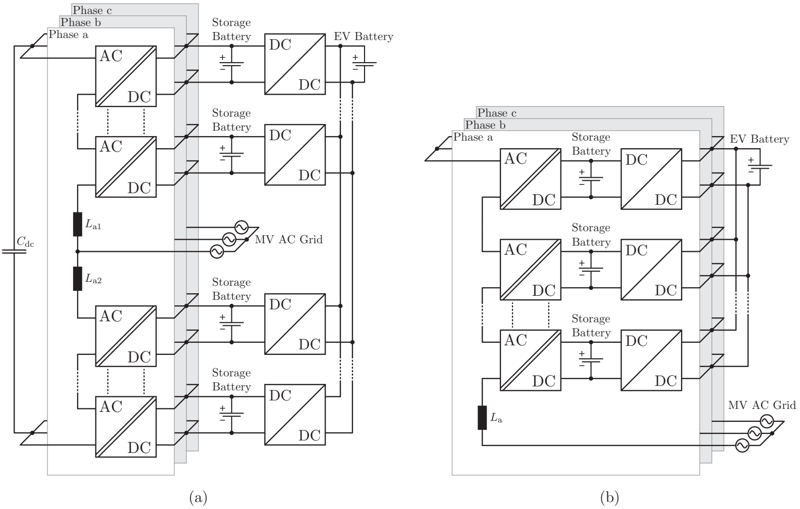


Figure 1.3: Ultra-fast charging station based on a split battery energy storage system applying the modular multilevel converter (MMC) in (a) and the cascaded H-bridge converter (CHB) in (b). The required galvanic isolation between the grid and the EV battery (see Section 2.1.4) is realized on the grid-side module level. With non-isolated DC-DC converters connecting the storage batteries to the EV battery a high charging power for a short charging process becomes available.

1.2 Objectives and contributions

The objective of this thesis is to develop, analyze and identify realization concepts and converter topologies for an ultra-fast charging station for electric vehicles with an integrated split battery energy storage system connected to a MV AC grid. The focus lies on the development and the electric as well as magnetic modeling of grid-connected modular converter systems with integrated galvanic isolation on the module level. For the promising module topologies new modulation schemes utilizing soft-switching are developed, analyzed, optimized and verified with a hardware prototype and/or in simulation. The main contributions of this thesis are given in the following.

New concept of a three-phase cascaded AC-DC (two-port) dual active bridge converter which is modular on the phase level

- Based on the state-of-the-art cascaded H-bridge converter and the well-known DC-DC/AC-DC dual active bridge converter, a *new phase-modular concept of a cascaded AC-DC dual active bridge converter* for a split battery energy storage system is developed (Chapter 4, Section 4.1, **Fig. 4.1**), modeled and its operating principle analyzed (Chapter 4, Section 4.2) and validated in simulation (Chapter 4, Section 4.6).

- For the proposed concept, a single-phase AC-DC dual active bridge converter as module is investigated. A *modulation scheme* that allows soft-switching for all semiconductor devices over the full AC mains period considering also the variation of the switching frequency is developed and optimized (Chapter 4, Section 4.3.2).

- For the module, a hardware prototype of a single-phase AC-DC dual active bridge converter is designed and implemented for the experimental verification of the proposed modulation scheme with variable switching frequency (Chapter 4, Section 4.5).

- Finally for the proposed concept, the *converter control structure of a split battery energy storage system* is investigated. For controlling the grid currents and the state of charges of the batteries the control structure is designed (Chapter 4, Section 4.4) as well as implemented and validated in simulation (Chapter 4, Section 4.6).

New concept of a three-phase cascaded AC-DC multi-port converter which is modular on the phase level

- Based on the state-of-the-art cascaded H-bridge converter and known DC-DC multi-port converters (typically three-port systems), a *new phase-modular concept of a cascaded AC-DC multi-port converter* for a split battery energy storage system is developed (Chapter 5, Section 5.2, **Fig. 5.1**), modeled and its operating principle analyzed (Chapter 5, Section 5.3) as well as a converter module simulated (Chapter 5, Section 5.7).

- A *new generalized modeling approach of the power flows* in a multi-port converter with an arbitrary number of ports connected in series (e.g. dual active bridge converter) is developed (Chapter 5, Section 5.4). The modeling approach leads to analytical power flow equations including all possible modulation schemes.

- For the proposed concept, a three-phase AC-DC multi-port converter module is investigated and *new modulation schemes* are developed, analyzed, modeled and optimized: Firstly based on a fundamental wave approach (Chapter 5, Section 5.5.1) and secondly considering soft-switching conditions for all semiconductor devices over the full AC mains period (Chapter 5, Section 5.5.2). The proposed modulation schemes are validated in simulation (Chapter 5, Section 5.7).

Multi-objective optimization and comparison of the converter modules for the proposed concepts

- A multi-objective optimization of the proposed converter systems on the module level (Chapter 6, Section 6.1) applying state-of-the-art power component models in the electric, magnetic and thermal domain (Chapter 6, Section 6.2) is implemented. Finally, the converter modules are compared and discussed concerning efficiency and power density (Chapter 6, Section 6.4, Section 6.5).

- Additionally, a general optimization of the modulation scheme for a DC-DC dual active bridge converter design example applying the new modeling approach of the power flows (Chapter 5, Section 5.4) is carried out (Appendix A, Section A.3). Besides the clamping intervals and the phase shift, also the variation of the switching frequency is considered for the control.

1.3 Outline of the thesis

The thesis covers all valuable achievements of the investigations of medium voltage converter systems for an ultra-fast charging station for electric vehicles combined with a split battery energy storage system.

Chapter 1 starts with a motivation for the topic of the electric mobility and presents the state-of-the-art charging methods as well as today's available charging infrastructure. For an ultra-fast charging station for electric vehicles, state-of-the-art research approaches with integrated energy storage are summarized.

Chapter 2 presents the design aspects for an ultra-fast charging station for electric vehicles from which concepts for the realization are developed and the specifications and requirements for the converter system and the energy storage can be stated.

Chapter 3 evaluates state-of-the-art medium voltage bidirectional isolated AC-DC converter topologies suitable for the grid interface of an ultra-fast charging station for electric vehicles with the focus on the integration of a battery energy storage system as well as the integration of the galvanic isolation on module level.

Chapter 4 proposes a new cascaded AC-DC dual active bridge converter for a split battery energy storage system. For the topology, suitable modulation and control schemes both on module as well as on system level are developed. A hardware prototype of a module is designed and built to experimentally verify the proposed modulation schemes. The overall battery energy storage system is simulated to validate the given theoretical analysis.

Chapter 5 introduces a new cascaded AC-DC multi-port converter for a split battery energy storage system. For a three-phase AC-DC multi-port converter module, a new modeling approach for the power flows at the AC and the DC ports is presented and suitable modulation schemes are developed. The converter module is simulated to validate the given theoretical analysis.

Chapter 6 presents a multi-objective optimization and comparison of the proposed converter systems on module level in terms of efficiency and power density. Besides the applied models of the power components the optimization procedure for each converter module is shown. Finally, the obtained optimization results are discussed and the proposed converter modules compared to the conventional two-stage AC-DC H-bridge module connected to a DC-DC dual active bridge converter.

Chapter 7 summarizes and concludes the main achievements of the thesis and presents an outlook on possible future research work.

Appendix A recapitulates state-of-the-art modulation schemes for DC-DC dual active bridge converters and presents a general optimization of a DC-DC dual active bridge converter design example based on the new modeling approach for the power flows. Besides the clamping intervals and the phase shift also the variation of the switching frequency for control is considered in the optimization.

Appendix B covers the loss models of the power components used for the calculations throughout the thesis including semiconductor losses for IGBTs and MOSFETs, inductor and transformer losses in terms of skin effect, proximity effect and core losses as well as capacitor losses.

1.4 List of publications

Different parts of this thesis including texts, tables, figures and equations have been previously published in scientific publications in international journals and conference proceedings. The publications are listed in the following.

Conference papers

1. F. Jauch, J. Biela, *Bidirectional Isolated ZVS DC-DC Converter with Nonpulsating Input & Output Current*, 11th Brazilian Power Electronic Conference (COBEP), Natal, Brazil, September 11-15, 2011.

2. F. Jauch, J. Biela, *An Innovative Bidirectional Isolated Multi-Port Converter with Multi-Phase AC Ports and DC Ports*, 5th EPE Joint Wind Energy and T&D Chapters Seminar, Aalborg, Denmark, June 28-29, 2012.

3. F. Jauch, J. Biela, *Single-Phase Single-Stage Bidirectional Isolated ZVS AC-DC Converter with PFC*, 15th International Power

Electronics and Motion Control Conference and Exposition (EPE-PEMC), Novi Sad, Serbia, September 4-6, 2012.

4. F. Jauch, J. Biela, *Modelling and ZVS Control of an Isolated Three-Phase Bidirectional AC-DC Converter*, 15th European Conference on Power Electronics and Applications, Lille, France, September 3-5, 2013.
5. F. Jauch, J. Biela, *Generalized Modeling and Optimization of a Bidirectional Dual Active Bridge DC-DC Converter including Frequency Variation*, International Power Electronics Conference (ECCE Asia), Hiroshima, Japan, May 18-21, 2014.
6. F. Jauch, J. Biela, *Novel Isolated Cascaded Half-Bridge Converter for Battery Energy Storage Systems*, 16th European Conference on Power Electronics and Applications, Lappeenranta, Finland, August 26-28, 2014.
7. D. Christen, F. Jauch, J. Biela, *Ultra-Fast Charging Station for Electric Vehicles with integrated split Grid Storage*, 17th European Conference on Power Electronics and Applications, Geneva, Switzerland, September 8-10, 2015.

Journal papers

1. F. Jauch, J. Biela, *Generalized Modeling and Optimization of a Bidirectional Dual Active Bridge DC-DC Converter Including Frequency Variation*, IEEJ Journal of Industry Applications, vol. 4, no. 5, pp. 593-601, 2015
2. F. Jauch, J. Biela, *Combined Phase Shift and Frequency Modulation of a Dual Active Bridge AC-DC Converter with PFC*, IEEE Transactions on Power Electronics, accepted for publication

Patents

1. F. Jauch, J. Biela, *Konverterschaltung und Verfahren zum Ansteuern einer Konverterschaltung*, CH 706 337 A2, April 2, 2012.

2

Ultra-Fast Charging Station for Medium Voltage Grids

In the design process of an ultra-fast charging station for the medium voltage grid, the requirements and the specifications according to the intended application area have to be evaluated first. Main factors like the amount of electric vehicles (EVs) to be charged during a specific time, the average energy content of an EV battery and the desired charging time per energy unit play an important role. Based on these aspects, concepts for the realization of an ultra-fast charging station can be developed.

2.1 Design aspects

When designing an ultra-fast charging station several aspects have to be taken into account including

- the amount of EVs to be charged during a specific time,
- the average energy content of an EV battery,
- the desired/required charging time per energy unit,
- meeting the EV battery galvanic isolation standards [55, 56].

The first three aspects define the required charging power the station has to deliver to the EV whereas the fourth one guarantees compliance with standards for safety reasons. In the following, two scenarios of an ultra-fast charging station are discussed - a large charging station near

Table 2.1: Ultra-fast charging station scenarios for a large charging station near highways and a small charging station in urban regions. It is assumed that the battery capacity for EVs charging at a highway station is higher because of long distance drives compared to EVs charging in urban regions.

Parameter	**Large station near highways**	**Small station in urban regions**
EVs per day	200	50
EVs charging in parallel	6	1
Typical battery capacity	48 kWh	24 kWh
Charging rate	9.6 kWh/min	4.8 kWh/min
Charging power per EV[a]	576 kW	288 kW
Total charging power[b]	3.46 MW	288 kW

---

[a] Effective charging power not covering losses.

[b] Total effective charging power not covering losses.

highways and a small charging station in urban regions. The scenarios are summarized in **Tab. 2.1**.

2.1.1 Utilization

In [57, 58] Monte Carlo simulations of different utilization scenarios of an ultra-fast charging station are performed. The utilizations range from 50 EVs per day up to 200 EVs per day which are based on typical traffic density distributions in Switzerland. In this work, the utilization of a small charging station is assumed to be 50 EVs per day whereas for the large charging station 200 EVs per day are considered.

2.1.2 EV battery capacity

The typical battery energy content of a medium-sized EV is assumed to be 24 kWh which is exactly the median of the listed EVs in **Tab. 1.1** available on the market in early 2015. This battery capacity allows driving around 200 km. Due to the limited range, such EVs are especially used in urban regions. Travelling long distances require higher ranges and therefore an increased battery capacity. With the Tesla Model S 70D listed in **Tab. 1.1** ranges over 400 km are possible. Nevertheless, it is currently the only available EV with such a high range and a relatively large battery capacity of 70 kWh. For the large charging station, it is assumed that the typical battery capacity is around 48 kWh since near highways especially EVs driving long distances are charged. The average consumption of these EVs is considered to be 12 kWh/100 km for the New European Driving Cycle (NEDC) [12].

2.1.3 Charging time

In the European 400 V AC low voltage distribution grid[1], currents at home or at workplaces are often limited to 16 A per phase/socket. For instance with a 3.3 kW single-phase charger[2] the charging process for a typical medium-sized EV takes up to 8 h for a full battery recharge [26]. With a three-phase connection the available charging power is increased to 10 kW so that the charging time can be reduced by a factor of 3. Nevertheless, it stays in the range of a few hours.

Considering such long charging times, especially for long distance drives, the EV loses its practical application. Drivers have to fundamentally change their habits and adapt to the restricted mobility what is rather difficult to achieve. For this reason, fast charging modes are established to cut down charging times, so that drivers feel comfortable when they can recharge whenever they like.

The CHAdeMO standard defines DC fast charging with voltages up to 500 V and currents up to 120 A [26] which is covered by the *charging mode 4* according to the IEC 61851-1 standard [25]. Furthermore, in the IEC 61851-1 standard AC fast charging from the 400 V low voltage grid is covered with phase currents of 32 A and 63 A respectively [24–26]. Increasing the charging power to 50 kW according to the CHAdeMO standard [27], EV batteries can be recharged in 20 min to 30 min depending on their capacities. Many manufacturers of EVs and charging stations deliver their products compliant with the CHAdeMO standard. In spring 2015, already 8’000 CHAdeMO charging stations are placed all over the world [27].

The focus of this work is on DC ultra-fast charging which means to cut down charging times to 5 min for a typical EV battery with 24 kWh [57]. This leads to a charging rate of 4.8 kWh/min which requires a charging power of 288 kW for a lossless charging process. This is the scenario considered for a small charging station. For large charging stations near highways a 5 min charging process for an EV battery with double the capacity is assumed. The required effective charging power is then given by 576 kW.

---

[1] 230 V phase voltage and 400 V phase-to-phase voltage.

[2] Power electronic converter with an efficiency of 90 %.

2.1.4 Galvanic isolation

The galvanic isolation requirement for EV chargers between the AC distribution grid and the EV battery is commonly related to safety issues [55]. In [56] case studies investigate the outcome of a human touching the AC line while he/she is connected to the EV chassis ground. Simulations show that for non-isolated chargers a person gets shocked while for isolated chargers with no connection from the neutral to the ground this is not the case.

In case of DC chargers with a direct coupling to the EV battery, the IEC 61851-23 standard states the isolation requirements between the AC distribution grid and the EV battery [30, 59]. The output side of the DC charging system has to be designed as an unearthed DC power supply (IT system) with insulation monitoring.

For ultra-fast charging stations with an integrated energy storage and comparable low grid power connection [60] it is more beneficial to integrate the galvanic isolation in the low power frontend converter connected to the grid than in the high power charging converter itself from the efficiency point of view.

2.1.5 Summary and discussion

For a charging station the required charging power is mainly determined by the EV battery capacity and the charging rate. Especially for DC ultra-fast charging the charging power is relatively high compared to a DC fast charging station compliant with the CHAdeMO standard. Furthermore, with increasing charging currents the resistive losses caused by internal battery cell resistances as well as contact resistances grow. The faster the charging process, not only the more effective charging power is required, but also the power to cover the losses is increased.

Considering a battery pack with an internal resistance r_{bat} and an open-circuit voltage v_{bat} (mainly dependent on the state of charge (SOC)), the required charging power delivered from the power electronic system is given by

$$P_{\mathrm{ch}} = \frac{1}{t_{\mathrm{ch}}} \int_0^{t_{\mathrm{ch}}} v_{\mathrm{bat}}(t) i_{\mathrm{ch}}(t) + i_{\mathrm{ch}}(t)^2 r_{\mathrm{bat}}(t) \; \mathrm{d}t \tag{2.1}$$

where t_{ch} represents the charging time. v_{bat} and r_{bat} depend on the non-linear characteristic of the battery pack and vary according to the applied charge pattern. With conversion efficiencies η_{g} of an AC-DC grid interface and η_{ch} of a connected DC-DC charger the grid power input is

$$P_{\mathrm{g}} = \frac{P_{\mathrm{ch}}}{\eta_{\mathrm{g}} \eta_{\mathrm{ch}}}. \tag{2.2}$$

Using a three-phase connection to the 400 V low voltage distribution grid would lead to phase currents in excess of 400 A for ultra-fast charging of one EV which results in an overload of the copper cables [61]. A reasonable approach for an ultra-fast charging station in public areas should therefore focus on medium voltage grid connections so that also several EVs in parallel could be charged. Furthermore, buffering of energy should be considered, especially for times when the grid power is limited or energy from distributed generation has to be stored. Hence, the integration of energy storage can lead to a reduction of the rated power of the station. The energy for the charging process is then partly or fully drawn from an intermediate energy storage.

Addressing the battery technology, ultra-fast charging requires comparable high power densities of the battery cells. Optimizations of lithium-ion cells in [62] show that with an increased power density the energy density of the cell rapidly drops. In general it is a trade-off between power density and energy density when designing a lithium-ion cell. The faster a cell can be charged, the lower its energy density is. For an EV suitable for ultra-fast charging, this means also a drastic increase in weight.

2.2 Concepts for realization

In the following, two concepts for the realization of an ultra-fast charging station for the medium voltage AC grid are given. First, a solution based on a medium voltage DC bus which suits large charging stations for instance near highways is presented. Secondly, an integrated charging solution based on a battery storage system connected directly to the medium voltage AC grid is introduced. This solution is mainly intended to be used in urban regions with a low amount of charging slots. Both concepts basically exhibit an AC-DC grid interface and one or more energy transfer units for charging the EV batteries.

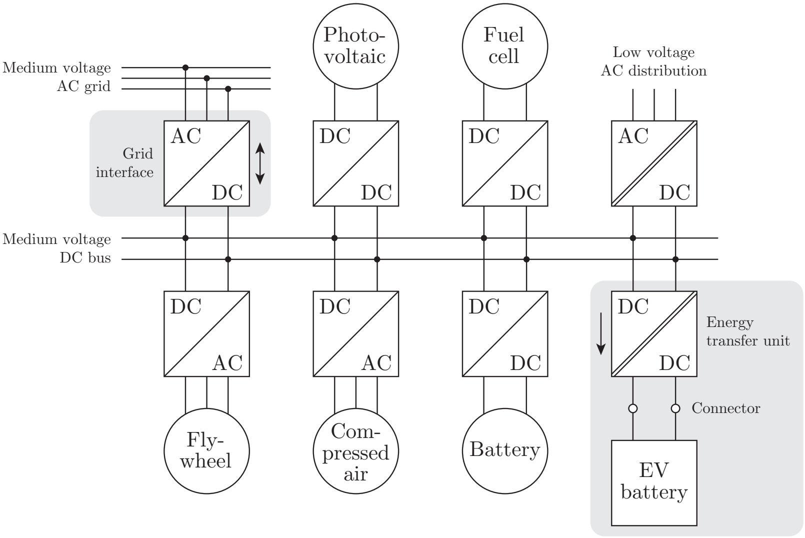

Medium voltage
AC grid
Photo-
voltaic
Fuel
cell
Low voltage
AC distribution
Grid
interface
AC
DC
DC
DC
DC
DC
AC
DC
Medium voltage
DC bus
DC
AC
DC
AC
DC
DC
DC
DC
Energy
transfer unit
Connector
Fly-
wheel
Com-
pressed
air
Battery
EV
battery

Figure 2.1: Ultra-fast charging station concept with a medium voltage DC bus suitable for large electric charging stations near highways. The station consists mainly of a non-isolated AC-DC grid interface to couple the DC bus to the medium voltage AC grid and an isolated DC-DC energy transfer unit for charging the EV battery. Additionally, energy storage can be attached to the DC bus such as flywheels, compressed air storage or battery storage systems. The station could also provide energy to EVs from own generation such as photovoltaic panels or fuel cells.

2.2.1 Medium voltage DC bus

A concept of an ultra-fast charging station with a medium voltage DC bus is depicted in **Fig. 2.1**. The DC bus allows the connection of energy storage like flywheels, compressed air storage, battery storage systems, ultra-capacitors and so on. Furthermore, the station can include own generation for instance from renewables like solar or wind power. The various storage medias and generation units are directly coupled to the DC bus by non-isolated AC-DC or DC-DC converters respectively. The DC bus could also be seen as a DC grid around big cities with a large amount of distributed generation and interfaces to an AC or even a DC low voltage distribution grid.

Besides generation and storage units, a non-isolated AC-DC grid interface couples the station to the medium voltage AC grid. The DC-DC energy transfer unit serves as a high power charging converter where also the galvanic isolation from the DC bus is integrated. The AC-DC grid interface is capable of bidirectional power flow whereas the DC-DC energy transfer unit only delivers power to the EV battery. For vehicle to grid applications, one could also think of a bidirectional energy transfer unit.

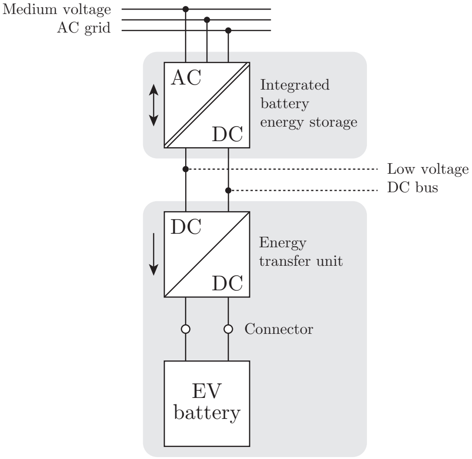


Figure 2.2: Ultra-fast charging station concept with an integrated battery energy storage suitable for urban electric charging stations. The station consists of an isolated AC-DC grid interface where storage batteries are included. The non-isolated DC-DC energy transfer unit connects the AC-DC converter to the EV battery for charging operation.

2.2.2 Integrated battery energy storage

In **Fig. 2.2** a concept of an ultra-fast charging station with integrated battery energy storage suitable for urban regions is shown. The AC-DC grid interface integrates the galvanic isolation from the medium voltage AC grid as well as storage batteries to provide sufficient energy for the charging process in times with low grid power available.

The grid interface basically combines the purposes of charging EVs and storing energy from the grid. Especially with the increasing generation from renewables, energy storage systems become an important part of the electricity infrastructure in order to maintain the stable operation of the grid in the long run.

The DC-DC energy transfer unit connects the grid interface to the EV battery and is non-isolated as the isolation stage is already included in the grid interface. The converter provides unidirectional power flow as long as no vehicle to grid applications are needed. An additional low voltage DC bus is available where the voltage fluctuates with the SOC of the storage batteries. This could be used for instance for powering auxiliaries like the charging control.

2.2.3 Focus of this work

Due to range limitations and relatively long charging times of EVs compared to fossil fuel powered cars, the large-scale application of EVs is still developing very slowly. Nevertheless, in urban regions where driving distances are short and EVs exhibit long parking times at home or at work the electric mobility gains interest. In and around big cities more and more charging infrastructure will be established in the next few years. Besides slow and fast charging of EVs, also the demand for ultra-fast charging will increase.

Therefore, this work focuses on an ultra-fast charging station with an integrated battery energy storage system as shown in **Fig. 2.2** for the application in urban regions. For the AC-DC grid interface, power electronic converter topologies and modulation schemes are developed, optimized and evaluated concerning achievable efficiency and power density. The main goal is the integration of the galvanic isolation into state-of-the-art converter topologies in order to reduce the number of conversion stages. The DC-DC energy transfer unit is not covered in this work. A possible approach is described in [60] where an ultra-fast charging station for the low voltage distribution grid is presented.

2.3 Specifications and requirements

For an ultra-fast charging station with an integrated battery energy storage system (see **Fig. 2.2**), detailed specifications and requirements are derived in the following. These are relevant for selecting and developing suitable power electronic converter systems in this work. In **Tab. 2.2** the AC-DC grid interface parameters are summarized.

First of all, the voltage level of the AC medium voltage grid and the rated power of the AC-DC converter are specified. According to IEC 60038 voltage standards [63] a nominal system voltage of 6.6 kV is considered. Due to the integrated battery energy storage in the AC-DC grid interface the nominal power can be lower than the charging power listed in **Tab. 2.1**. In this work, the nominal grid power is fixed to 150 kW and the energy storage sized depending on the charging power as shown in the following.

2.3.1 Charging power

In order to size the energy storage, the total charging power considering the losses in the EV battery pack has to be determined. Assuming a constant open-circuit battery pack voltage V_{bat}, a constant internal resistance R_{bat} and a constant DC current I_{ch} during the ultra-fast

Table 2.2: Specifications and requirements for the AC-DC grid interface with an integrated battery energy storage system used in an ultra-fast charging station in urban regions (see **Fig. 2.2**).

	Parameter	**Value**
AC-DC converter	AC grid voltage	6.6 kV
	Nominal output power	150 kW
	Galvanic isolation	Required
	Bidirectional power flow	Required
Battery storage	Storage capacity	1 MWh
	Battery technology	Lithium-ion
	Battery voltage	< 1000 V

Table 2.3: Parameters for an ultra-fast charging process of a typical EV battery pack built with lithium-ion polymer cells. The data corresponds to the Nissan Leaf battery pack which includes cells from AESC [64, 65].

Open-circuit voltage	V_{bat}	$360\,\mathrm{V}$[a]
Internal resistance	R_{bat}	$125\,\mathrm{m\Omega}$[b]
Charging current	I_{ch}	$800\,\mathrm{A}$
Effective charging power	$P_{\mathrm{ch,eff}}$	$288\,\mathrm{kW}$
Charging losses	$P_{\mathrm{ch,loss}}$	$80\,\mathrm{kW}$
Charging power	P_{ch}	$368\,\mathrm{kW}$
Charging efficiency	η_{ch}	$78\,\%$

---

[a] The nominal cell voltage of the AESC lithium-ion polymer cell is 3.75 V [65].

[b] The internal battery pack resistance is approximated by the measurements given in [64]. The number of cells in series is $N_{\mathrm{cell,s}} = 96$ and the number of strings in parallel $N_{\mathrm{cell,p}} = 2$ [64].

charging process, (2.1) simplifies to

$$P_{\mathrm{ch}} = V_{\mathrm{bat}} I_{\mathrm{ch}} + I_{\mathrm{ch}}^2 R_{\mathrm{bat}} = P_{\mathrm{ch,eff}} + P_{\mathrm{ch,loss}}. \tag{2.3}$$

The required charging power consists of an effective part $P_{\mathrm{ch,eff}}$ to deliver energy to the battery cells as well as a resistive part $P_{\mathrm{ch,loss}}$ that covers the losses. The internal resistance R_{bat} of the battery pack depends on the number of cells connected in series $N_{\mathrm{cell,s}}$, the strings connected in parallel $N_{\mathrm{cell,p}}$ and the cell resistance R_{cell} given by the manufacturer and is written as

$$R_{\mathrm{bat}} = \frac{N_{\mathrm{cell,s}} R_{\mathrm{cell}}}{N_{\mathrm{cell,p}}}. \tag{2.4}$$

Given the effective charging power $P_{\mathrm{ch,eff}} = 288\,\mathrm{kW}$ from **Tab. 2.1** and an average battery voltage $V_{\mathrm{bat}} = 360\,\mathrm{V}$, the DC charging current is calculated to be $I_{\mathrm{ch}} = 800\,\mathrm{A}$. With the internal battery pack resistance $R_{\mathrm{bat}} = 125\,\mathrm{m\Omega}$ of the Nissan Leaf [64], the required charging power yields $P_{\mathrm{ch}} = 368\,\mathrm{kW}$ which leads to a charging efficiency of $\eta_{\mathrm{ch}} = 78\,\%$. The results are summarized in **Tab. 2.3**.

2.3.2 Energy storage

The charging power P_{ch} given in (2.3) can be divided into two parts: The power P_{g} delivered from the grid and the power P_{s} from the battery energy storage (energy E_{s} delivered during t_{ch}). This leads to

$$P_{\mathrm{ch}} = \eta_{\mathrm{ch}} \left(\eta_{\mathrm{g}} P_{\mathrm{g}} + P_{\mathrm{s}}\right) = \eta_{\mathrm{ch}} \left(\eta_{\mathrm{g}} P_{\mathrm{g}} + \frac{E_{\mathrm{s}}}{t_{\mathrm{ch}}}\right) \tag{2.5}$$

with η_{ch} being the efficiency of the DC-DC energy transfer unit and η_{g} the efficiency of the AC-DC grid interface. Assuming a fixed grid power P_{g} and N_{ev} EVs to be charged per day from the grid and the energy storage, the required energy buffer can be determined as

$$E_{\mathrm{bess}} = N_{\mathrm{ev}} E_{\mathrm{s}} = N_{\mathrm{ev}} \left(\frac{P_{\mathrm{ch}} t_{\mathrm{ch}}}{\eta_{\mathrm{ch}}} - \eta_{\mathrm{g}} P_{\mathrm{g}} t_{\mathrm{ch}}\right). \tag{2.6}$$

With this calculation the buffer will be empty after 24 h without recharging operation between the EV charging processes. The time available for recharging the energy buffer is

$$T_{\mathrm{bess}} = 24\,\mathrm{h} - N_{\mathrm{ev}} t_{\mathrm{ch}} \tag{2.7}$$

from which the recharging constraint

$$E_{\mathrm{bess}} \leq \eta_{\mathrm{g}} P_{\mathrm{g}} T_{\mathrm{bess}} = \eta_{\mathrm{g}} P_{\mathrm{g}} \left(24\,\mathrm{h} - N_{\mathrm{ev}} t_{\mathrm{ch}}\right) \tag{2.8}$$

arises that guarantees the buffer to be recharged during a day. The maximum number of EVs that can be charged a day is reached at the equality of the recharging constraint. There, T_{bess} gets minimal so that the recharging operation exactly covers the energy which is consumed by the EVs charged during a day.

The numerical evaluation of (2.6) for the grid power $P_{\mathrm{g}} = 150\,\mathrm{kW}$, the charging power $P_{\mathrm{ch}} = 368\,\mathrm{kW}$, converter efficiencies $\eta_{\mathrm{g}} = \eta_{\mathrm{ch}} = 95\,\%$, a charging time of $t_{\mathrm{ch}} = 5\,\mathrm{min}$ and $N_{\mathrm{ev}} = 50$ leads to the required energy storage $E_{\mathrm{bess}} = 1\,\mathrm{MWh}$.

3

Bidirectional Isolated AC-DC Converter Topologies

For an ultra-fast charging station with an integrated battery energy storage system as presented in **Fig. 2.2**, suitable power electronic converter topologies for the AC-DC grid interface are evaluated in this chapter. As previously mentioned, the high power DC-DC energy transfer unit is not considered in this work. The focus lies on medium voltage (MV) AC-DC converter concepts where the integration of a battery energy storage system is possible. The specifications and requirements are summarized as follows:

- Three-phase MV AC grid connection,
- integration of battery packs at the DC side,
- galvanic isolation between the AC grid and the DC side,
- bidirectional power flow (charging and discharging operation of the storage batteries).

Possible MV converter topologies are classified according to their phase modularity, the number of conversion stages and the type of interconnection of the modules in modular topologies. **Fig. 3.1** gives an overview of state-of-the-art bidirectional isolated AC-DC converter topologies which are further described in this chapter. The primary focus in this thesis is on phase-modular single-stage converter topologies (gray shaded area in **Fig. 3.1**).

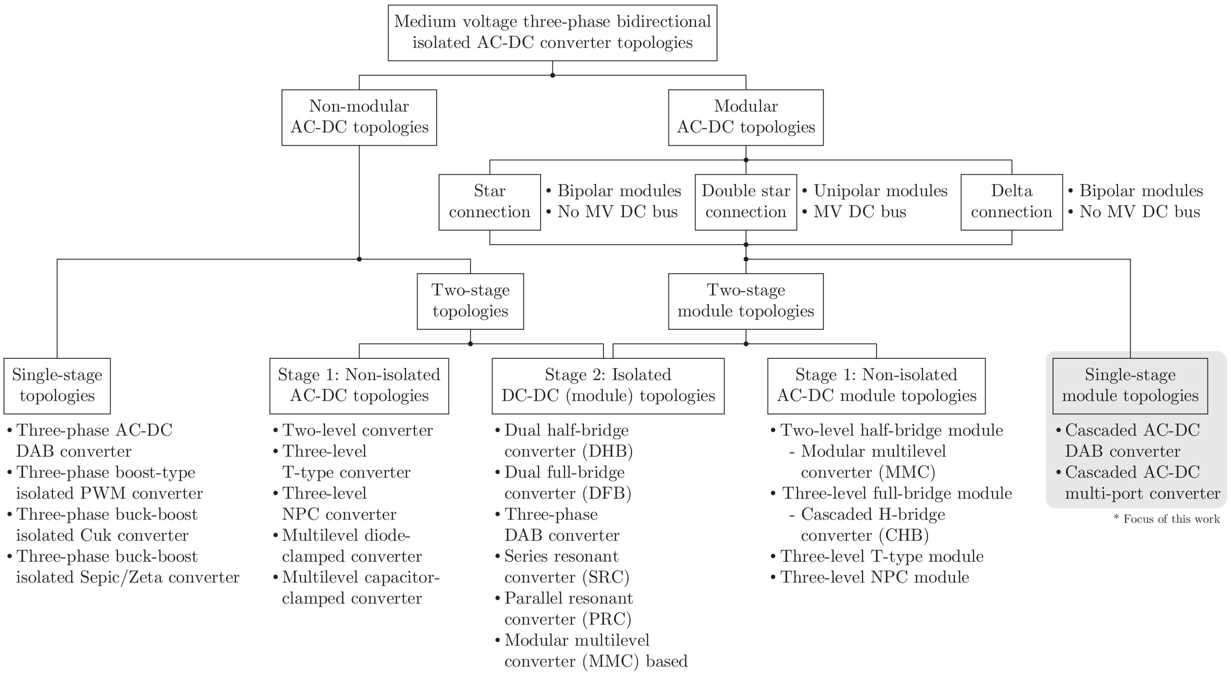
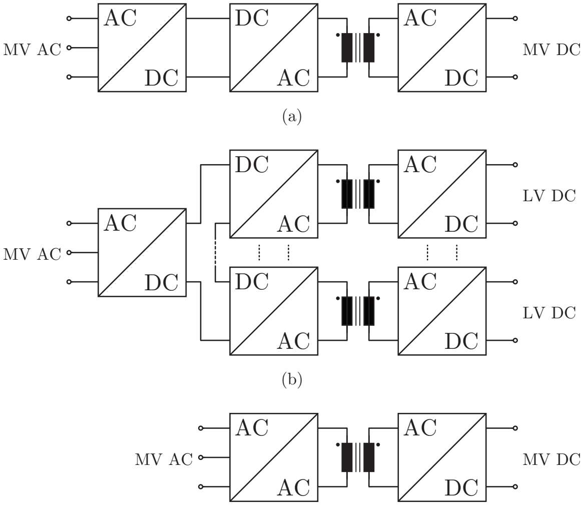

Medium voltage three-phase bidirectional isolated AC-DC converter topologies
Non-modular AC-DC topologies
Modular AC-DC topologies
Star connection
• Bipolar modules
• No MV DC bus
Double star connection
• Unipolar modules
• MV DC bus
Delta connection
• Bipolar modules
• No MV DC bus
Two-stage topologies
Two-stage module topologies
Single-stage topologies
• Three-phase AC-DC DAB converter
• Three-phase boost-type isolated PWM converter
• Three-phase buck-boost isolated Cuk converter
• Three-phase buck-boost isolated Sepic/Zeta converter
Stage 1: Non-isolated AC-DC topologies
• Two-level converter
• Three-level T-type converter
• Three-level NPC converter
• Multilevel diode-clamped converter
• Multilevel capacitor-clamped converter
Stage 2: Isolated DC-DC (module) topologies
• Dual half-bridge converter (DHB)
• Dual full-bridge converter (DFB)
• Three-phase DAB converter
• Series resonant converter (SRC)
• Parallel resonant converter (PRC)
• Modular multilevel converter (MMC) based
Stage 1: Non-isolated AC-DC module topologies
• Two-level half-bridge module
- Modular multilevel converter (MMC)
• Three-level full-bridge module
- Cascaded H-bridge converter (CHB)
• Three-level T-type module
• Three-level NPC module
Single-stage module topologies
• Cascaded AC-DC DAB converter
• Cascaded AC-DC multi-port converter
* Focus of this work

Figure 3.1: Overview of medium voltage bidirectional isolated AC-DC converter topologies classified by the phase modularity, the number of conversion stages and the type of interconnection of the modules in modular converter topologies.

3.1 Non-modular AC-DC topologies

In low voltage (LV) applications the use of conventional two-level or three-level three-phase AC-DC rectifier/inverter systems is quite common. Their inherently given non-modular structure does not allow a series connection of converters at the AC side to share the voltage across several terminals. In the case of a connection to a MV AC grid, suitable high power semiconductors have to be employed in such designs.



(a)

(b)

(c)

Figure 3.2: General three-phase non-modular AC-DC topologies with galvanic isolation: (a) two-stage isolated AC-DC converter with MV DC output, (b) two-stage isolated AC-DC converter with split LV DC outputs, (c) single-stage isolated AC-DC converter with MV DC output. The split LV DC outputs in (b) can be connected in series to form a MV DC output or in parallel to form a high current LV DC output.

Fig. 3.2 depicts general three-phase non-modular AC-DC topologies with galvanic isolation. For a two-stage solution, an isolated DC-DC converter is connected to a non-isolated AC-DC input stage to provide an isolated MV DC output. Besides a single DC-DC converter, also a series connection of DC-DC converter modules with split LV DC outputs can be employed. Moreover, solutions for an isolated single-stage conversion from three-phase AC to DC exist.

3.1.1 Two-stage topologies

For a two-stage power conversion, a non-isolated AC-DC converter coupled to the MV grid is further connected to a DC-DC isolation stage (see **Fig. 3.2**). In the following, state-of-the-art topologies both for the non-modular AC-DC converter system and the connected isolated DC-DC converter system are summarized.

Non-isolated AC-DC converter

For low voltage and low power applications, two-level or three-level voltage source AC-DC converters [66, 67] are quite common. For medium voltage applications these topologies demand high power semiconductor devices with a high blocking voltage (several kV) and a reasonable current capability. Using a series connection of semiconductor devices controlled by the same gate signal [68] can further extend the blocking voltage capability.

In multilevel converters, the required blocking voltage of the semiconductor devices is reduced by increasing the number of voltage levels. Furthermore, the harmonic content decreases as more levels to create the staircase voltage become available.

A generalized multilevel AC-DC converter topology is presented in [69] from where the well-known diode-clamped and capacitor-clamped (flying capacitor) multilevel converter topologies [67, 70] can be derived. The schematics of one phase leg for the two topologies are depicted in **Fig. 3.3** exemplarily for a five-level converter.

With the increasing number of voltage levels, the hardware complexity rises in terms of a high number of switches, diodes/capacitors and gate drives. Also the commutation paths get more critical as lead inductances of the semiconductor devices connected in series add up. Moreover, the number of redundant switching states grows which leads to an increased complexity in selecting the switching states. In the end, for a relatively high number of levels, these multilevel topologies are not practical to implement (the typical limit is seven or nine levels).

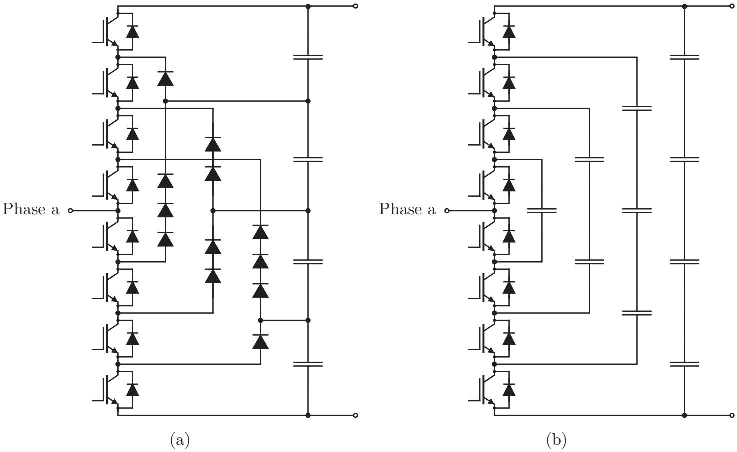


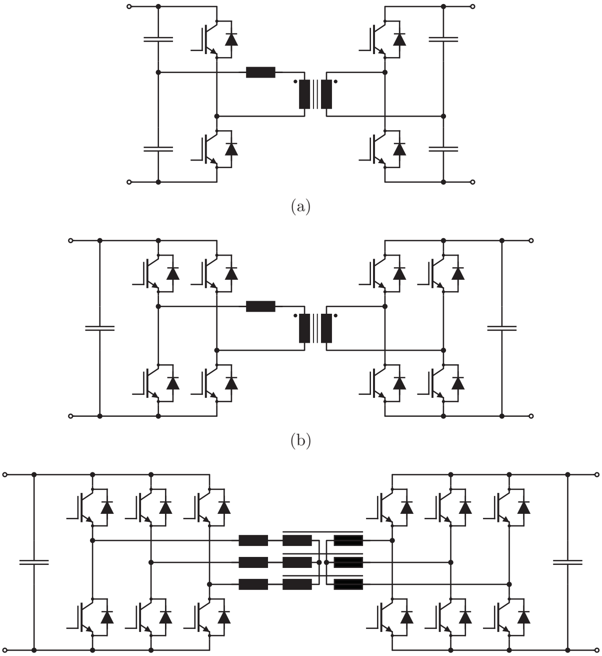
Figure 3.3: Five-level diode-clamped multilevel converter topology (a) and five-level capacitor-clamped multilevel converter topology (b) exemplarily shown for one phase leg.

Isolated DC-DC converter

For high power bidirectional DC-DC power conversion with galvanic isolation dual active bridge (DAB) converters are widely used [71]. The most prominent topologies are shown in **Fig. 3.4** and comprise the dual half-bridge (DHB) converter with a single-phase transformer and split DC input/output [72], the dual full-bridge (DFB) converter with a single-phase transformer [73] as well as the three-phase dual active bridge (DAB) converter with a three-phase transformer [74]. Integrating a resonant circuit in these topologies further leads to the series resonant converter (SRC) or the parallel resonant converter (PRC) [75]. Besides DAB topologies with voltage ports, also topologies with two current ports or mixed voltage and current ports exist [76].

Practical implementations of DAB converters for medium voltage applications comprise for instance a 15 kV silicon carbide MOSFET based 20 kW DHB system [77], a 1 MW 12 kV to 1.2 kV DFB converter [78] or a 5 MW three-phase DAB demonstrator with a 5 kV input and a 5 kV output [79].

Furthermore, medium voltage DC-DC conversion can be also based on a modular approach. The use of DABs as modules connected in series at the input (see **Fig. 3.2(b)**) and in series/parallel at the output is presented in [72] for a 10 kW 12 kV to 400 V converter. Another modular solution is based on the modular multilevel converter (MMC) with two phase strings (four arms) at the primary and the secondary side of a single-phase transformer [80].


(a)

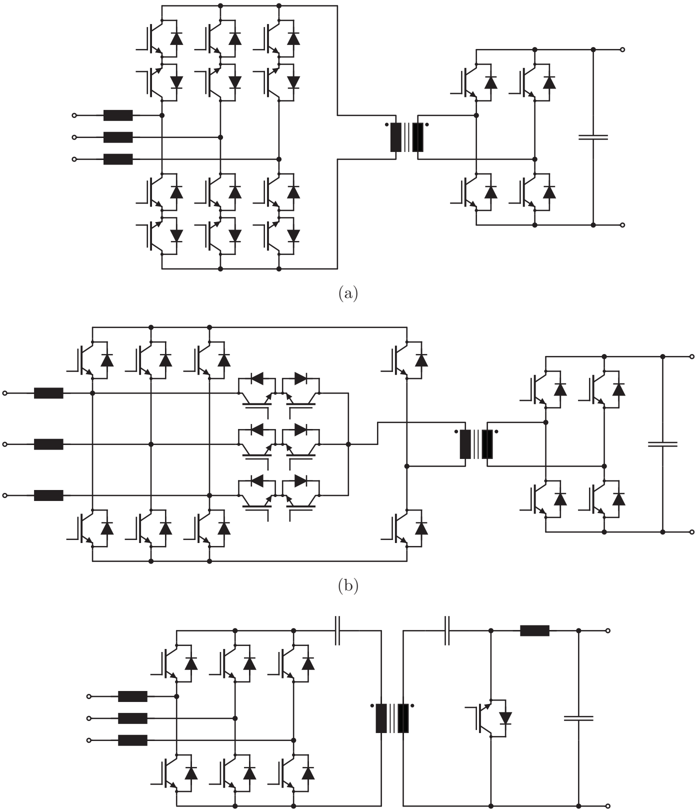
(b)

(c)

Figure 3.4: Isolated DC-DC dual active bridge (DAB) topologies: (a) dual half-bridge (DHB) converter with a single-phase transformer, (b) dual full-bridge (DFB) converter with a single-phase transformer and (c) three-phase dual active bridge converter with a three-phase transformer.

3.1.2 Single-stage topologies

Besides the two-stage power conversion approach, single-stage solutions exist with a two-level or a three-level AC input. **Fig. 3.5** shows possible three-phase converter systems with integrated galvanic isolation and bidirectional power flow capability summarized in the following.



(a)

(b)

(c)

Figure 3.5: Single-stage three-phase bidirectional isolated AC-DC converter topologies: (a) three-phase AC-DC dual active bridge [81,82], (b) three-phase boost-type isolated PWM converter [83,84] (c) three-phase buck-boost isolated Cuk converter [85–87].

A three-phase AC-DC DAB converter is presented in [81, 82] (see **Fig. 3.5(a)**) consisting of an AC-side cycloconverter and a DC-side full-bridge. The converter uses bidirectional switches at the AC side since the virtual DC link changes the polarity depending on the DC-side applied voltage at the transformer. For the different modulation schemes proposed in [81, 82], soft-switching in terms of zero voltage switching (ZVS) and zero current switching (ZCS) is achieved for a wide load range.

In [83, 84] a single-stage boost-type high-frequency isolated PWM converter system is introduced which consists of a combined three-phase T-type and half-bridge AC side and a full-bridge at the DC side (see **Fig. 3.5(b)**). [83] proposes only the unidirectional topology whereas [84] investigates its bidirectional operation with a modified space vector PWM modulation to keep the voltage-second product balance of the transformer.

Fig. 3.5(c) depicts a three-phase buck-boost isolated converter that is based on the Cuk converter. The unidirectional isolated topology is proposed in [86, 87] whereas the non-isolated bidirectional topology is discussed in [85]. The modulation scheme for bidirectional operation presented in [85] can be adjusted for the use in the isolated version of the converter system. Moreover, by rearranging the switch and the inductor at the DC side, a bidirectional isolated Sepic/Zeta AC-DC converter can be built.

3.2 Modular AC-DC topologies

Conventional three-phase AC-DC converter systems suffer from the disadvantage of being non-modular and can therefore not be connected in series to split the phase voltage between single converters. To overcome this, phase-modular AC-DC topologies have been developed which use several converter modules that are series-connected in phase strings. Especially for MV applications, modular converter topologies are highly attractive due to their scalability in terms of voltage and power levels. The possibilities of interconnecting the phase strings comprise the star, the delta and the double star connection. Recent research also shows a triple star connection for bidirectional AC-AC conversion [88].

3.2.1 Star connection

The general three-phase modular AC-DC topology in star connection with galvanic isolation integrated in the converter modules is shown in **Fig. 3.6**. A MV DC bus is not directly available, but could be formed by connecting the split DC outputs in series (this is only possible with isolated modules). Since the AC voltage of the converter modules exhibits a positive and a negative polarity, bipolar module topologies are required. For the isolated AC-DC modules, possible two-stage and single-stage solutions are presented in the following.

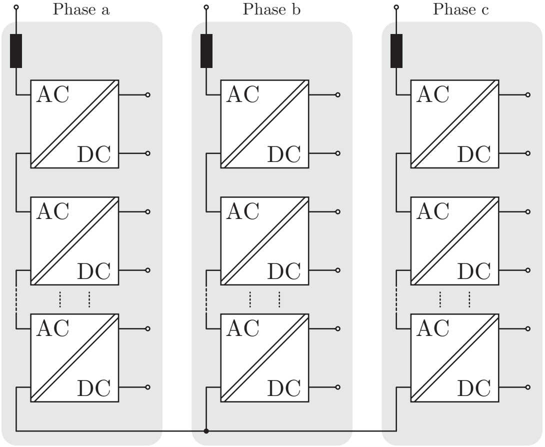


Figure 3.6: General three-phase modular AC-DC topology in star connection with galvanic isolation on module level. Multiple isolated AC-DC modules per phase string are connected in series depending on the AC voltage. The split DC outputs of the modules can be connected in series or in parallel.

Two-stage topologies

In a two-stage topology, the converter modules consist of a bipolar non-isolated AC-DC input stage connected to an isolated DC-DC converter as depicted in **Fig. 3.7**. The DC output of the AC-DC input stage buffers the pulsating power with twice the AC grid frequency in a comparably large DC link capacitor, so that the connected DC-DC converter is operated at a constant output power. Depending on voltage and power requirements the LV DC outputs of the modules can be connected in series or in parallel.

Possible bipolar non-isolated AC-DC module topologies for the application in a modular two-stage isolated AC-DC converter in star connection comprise the two-level half-bridge, the three-level full-bridge, the three-level T-type and the three-level NPC module (see **Fig. 3.8**). In theory, any multilevel module topology is applicable (e.g. five-level topologies shown in **Fig. 3.3**), but in practice no more than three levels are used for the cells in a modular converter system.

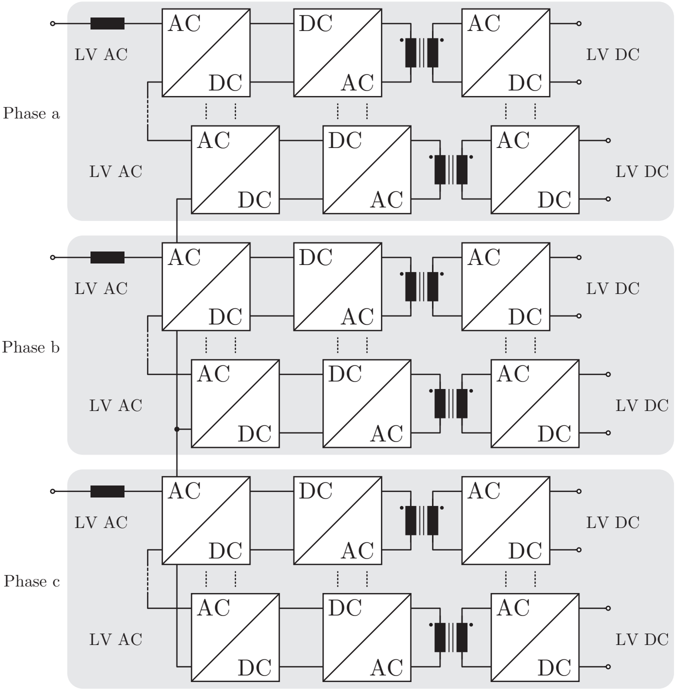


Figure 3.7: Two-stage isolated AC-DC converter with MV AC input (series-connected LV AC module inputs) and split LV DC outputs in star connection. The split LV DC outputs can be connected in series to form a MV DC output or in parallel to form a high current LV DC output.

In [48, 89] a multilevel cascade voltage source inverter having series-connected full-bridge inverters with separate DC sources per phase leg is introduced, also known as the cascaded H-bridge converter (CHB). The converter generates a multilevel staircase voltage waveform with the switches only switched once per AC line cycle. Thus, a nearly sinusoidal output voltage is reached by increasing the number of cascaded full-bridges. The application areas of the converter include for instance MV motor drive inverters [50], reactive power compensators [89] and interfacing fuel cell or photovoltaic systems [90]. Furthermore, the CHB gains interest in split battery energy storage systems where each full-bridge module connects to a storage battery pack [91–94].

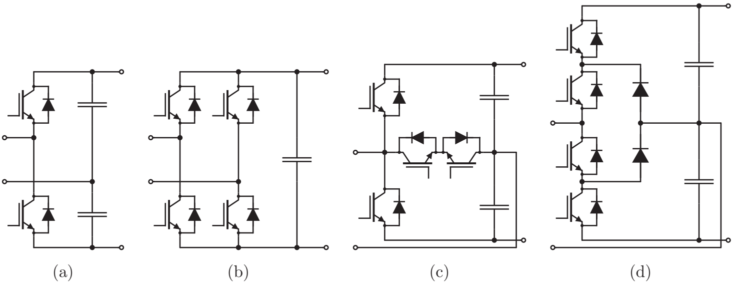

(a) (b) (c) (d)

Figure 3.8: Bipolar non-isolated AC-DC module topologies for the application in a modular two-stage isolated AC-DC converter in star/delta connection (e.g. cascaded H-bridge converter [48,89]): (a) two-level half-bridge module, (b) three-level full-bridge module, (c) three-level T-type module, (d) three-level NPC module.

For providing the galvanic isolation, each AC-DC module is connected to an isolated DC-DC converter. From the topology point of view, the most attractive converter systems for an input/output voltage of several 100 V represent DAB converters as previously described in Section 3.1.1 and shown in **Fig. 3.4**. [95, 96] propose a solid state transformer (SST) based on a CHB with a module-level isolation stage consisting of DAB converters. The same topology is applied in [97] for a large-scale photovoltaic grid integration and in [98] for a battery energy storage system.

Single-stage topologies

Besides the two-stage approach, single-stage solutions exist with either split LV DC outputs with pulsating power as shown in **Fig. 3.9** or split LV DC outputs with constant power as depicted in **Fig. 3.10**. The first topology simply represents a cascade of single-phase single-stage bidirectional isolated AC-DC converters whereas the second one uses a multi-port structure by magnetically coupling the AC module inputs of three different phases to a single DC output. Again, the split LV DC outputs can be connected in series or in parallel according to voltage and current requirements.

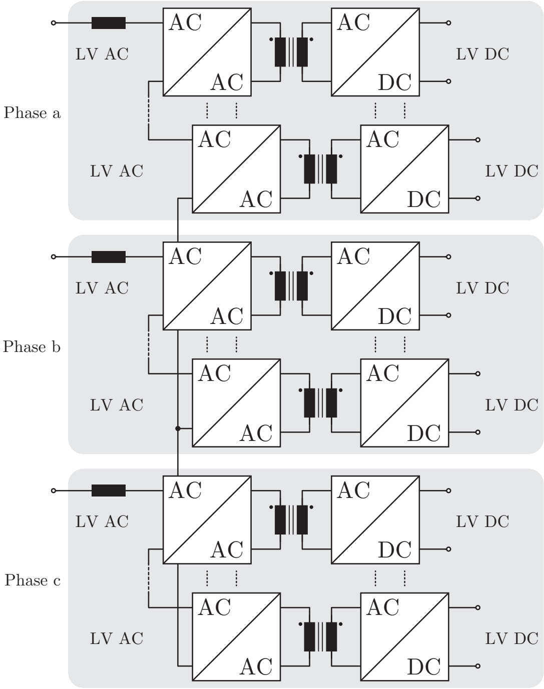


Figure 3.9: Single-stage isolated AC-DC converter with MV AC input (series-connected LV AC module inputs) and split LV DC outputs (with pulsating power) in star connection. The split LV DC outputs can be connected in series to form a MV DC output or in parallel to form a high current LV DC output.

Based on the approach of two actively switched bridges (DAB converters), possible isolated module topologies are derived by combining AC- and DC-side module blocks both with voltage ports. The AC-side voltage port changes its polarity with twice the AC grid frequency such that semiconductor devices with a reverse voltage blocking capability have to be applied.

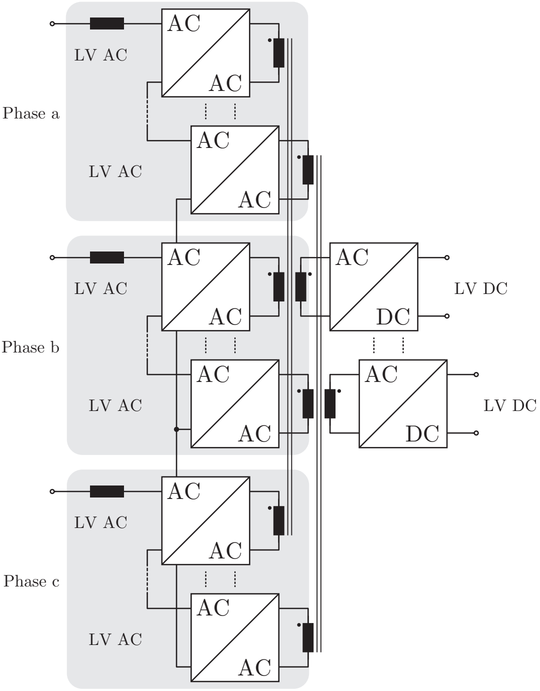


Figure 3.10: Single-stage isolated AC-DC converter with MV AC input (series-connected LV AC module inputs) and split LV DC outputs (with constant power) among the three different phases (multi-port structure) in star connection. The split LV DC outputs can be connected in series to form a MV DC output or in parallel to form a high current LV DC output.

Fig. 3.11 depicts the most useful AC module blocks like the two-level half-bridge, the three-level full-bridge and the three-level T-type block. All of these variants use an anti-serial connection of two IGBT co-packs to realize a bidirectional (four-quadrant) switch. For the DC side, possible module blocks are shown in **Fig. 3.12** and comprise the two-level half-bridge, the three-level full-bridge, the three-level T-type and the three-level NPC blocks. In contrast to the AC side, only unidirectional (two-quadrant) switches are necessary.

Examples for isolated AC-DC modules in a modular converter system as shown in **Fig. 3.9** include AC-DC DAB converters with either bidirectional switches at the AC side [99–102] or with a frontend synchronous rectifier in place [103]. The modulation schemes proposed in [99] and [102] achieve ZCS or ZVS conditions for all semiconductor devices in all points of operations whereas [103] presents an optimal modulation to guarantee ZVS for the full operating range.

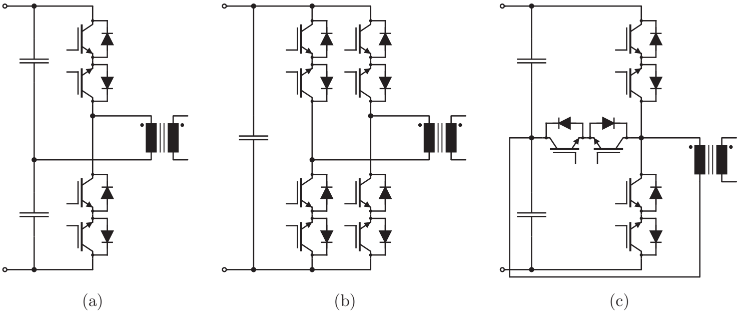

(a) (b) (c)

Figure 3.11: Bipolar isolated AC-side module blocks for the application in a modular single-stage isolated AC-DC converter in star/delta connection (e.g. cascaded H-bridge converter [48, 89]): (a) two-level half-bridge module block, (b) three-level full-bridge module block, (c) three-level T-type module block.

In [104] a modular high power converter consisting of series-connected DC-DC DAB converters for the connection to a MV DC grid is presented. The converter serves as a battery energy storage system where each of the DAB modules connect to a battery pack. Further research on series-connected AC-AC DAB converters is done in the field of SSTs for providing single-stage bidirectional isolated AC-AC conversion [105–107]. The proposed concepts can be also applied to series-connected AC-DC DAB converters with the DAB module topologies summarized above.

For the multi-port converter approach shown in **Fig. 3.10** research has mainly focused on DC-DC conversion. Examples of proposed multi-port converter systems comprise the bidirectional isolated three-port DC-DC converter based on the single-phase DAB converter [108–113] or on the three-phase DAB converter [114]. In [115] the multi-port DC-DC converter concept is further extended to four ports whereas [116, 117] present a general N-port DC-DC converter. Most of these topologies are operated by the conventional phase shift modulation. Nevertheless, by integrating a resonant tank into the multi-port converter also resonant operation is possible as for instance shown in [118] for a series resonant three-port DC-DC converter. Usually, port topologies like half-bridge [110, 112] or full-bridge cells [109, 111, 113, 117] are used either voltage-fed or current-fed [108].

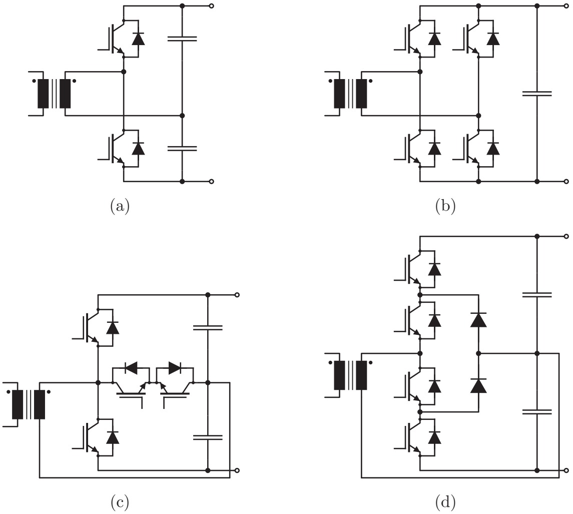


Figure 3.12: Unipolar isolated DC-side module blocks for the application in a modular single-stage isolated AC-DC converter in star/delta connection (e.g. cascaded H-bridge converter [48, 89]): (a) two-level half-bridge module block, (b) three-level full-bridge module block, (c) three-level T-type module block, (d) three-level NPC module block.

Isolated multi-port converters with combined AC and DC ports (see **Fig. 3.10**) have been rarely discussed in literature. Publications have mainly focused on three-phase isolated rectifier topologies based on a multi-port structure. Examples are converters employing three two-winding transformers with their DC-side windings either connected in series applying a diode rectifier stage [119–121], a current doubler rectifier stage [119, 122] or connected in star connection applying a three-phase diode rectifier stage [123, 124].

A three-phase bidirectional isolated AC-DC converter based on a multi-port approach by utilizing half-bridge cells in a push-pull stage at the AC-side ports and a three-phase DAB stage at the DC port is proposed in [125]. The galvanic isolation is realized with three three-winding transformers where the DC-side windings are connected in star connection. In [126] a multi-port converter for the coupling of the utility grid to a stationary storage battery as well as an electric vehicle (EV) battery is presented. The topology employs also three three-winding transformers with each phase of the grid connected to a different transformer through a cycloconverter. The two DC ports consist of a six-leg inverter and a three-leg inverter respectively coupled to each three-winding transformer via two different windings.

3.2.2 Double star connection

Besides the single star connection, a double star connection of series-connected isolated AC-DC modules is possible as depicted in **Fig. 3.13**. The converter topology consists of three phase strings/legs where each of them has two arms (gray shaded areas in **Fig. 3.13**). Compared to the single star connection, only unipolar modules are necessary since the AC voltage of the converter modules exhibit only a positive polarity. Furthermore, the converter topology directly provides a non-isolated MV DC bus. In the following, two-stage and single-stage topologies for the isolated AC-DC modules are summarized.

Two-stage topologies

In a two-stage solution, the converter modules consist of an unipolar non-isolated AC-DC input stage connected to an isolated DC-DC converter as previously shown for the single star connection in **Fig. 3.7**. In the double star configuration, two of the single stars are paralleled at the phase connections. The LV DC outputs of the two-stage converter modules can be connected in series and/or parallel according to voltage and power requirements.

For the application in a modular two-stage isolated AC-DC converter in double star connection, unipolar non-isolated AC-DC module topologies like the two-level half-bridge, the three-level T-type as well as the three-level NPC module (see **Fig. 3.14**) are possible. As previously mentioned, commonly no more than three levels are used for the cells in a modular converter system.

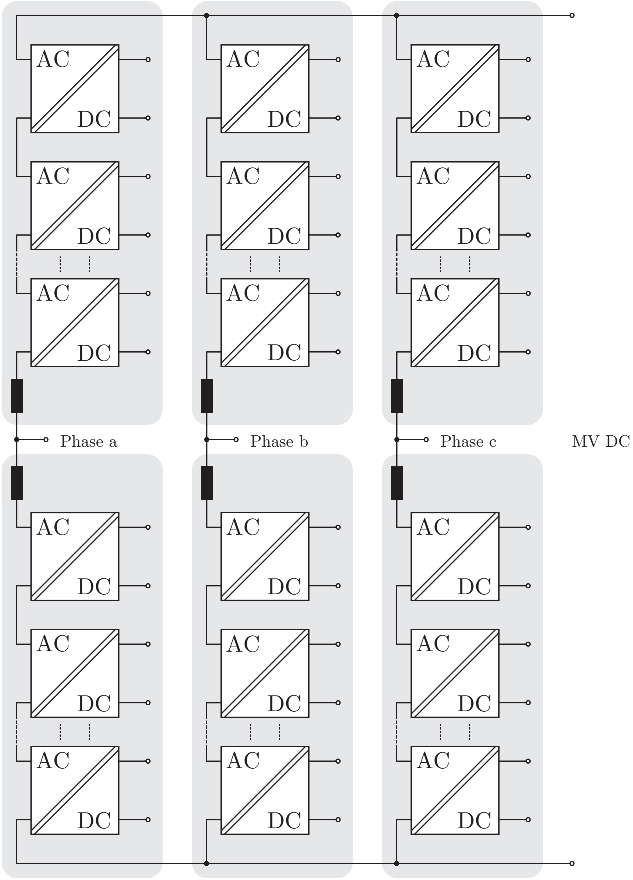


Figure 3.13: General three-phase modular AC-DC topology in double star connection with galvanic isolation on module level and a non-isolated MV DC bus. Multiple isolated AC-DC modules are connected in series in each of the two phase strings (arms) depending on the MV AC voltage and the MV DC voltage. The split DC outputs of the modules can be connected in series or in parallel.

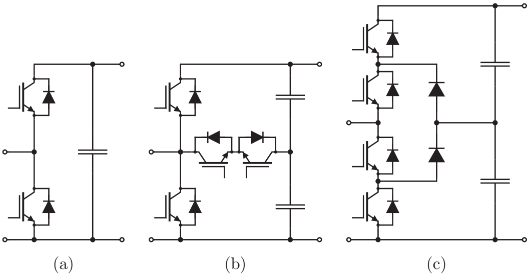

(a) (b) (c)

Figure 3.14: Unipolar non-isolated AC-DC module topologies for the application in a modular two-stage isolated AC-DC converter in double star connection (e.g. modular multilevel converter [47,127,128]): (a) two-level half-bridge module, (b) three-level T-type module, (c) three-level NPC module.

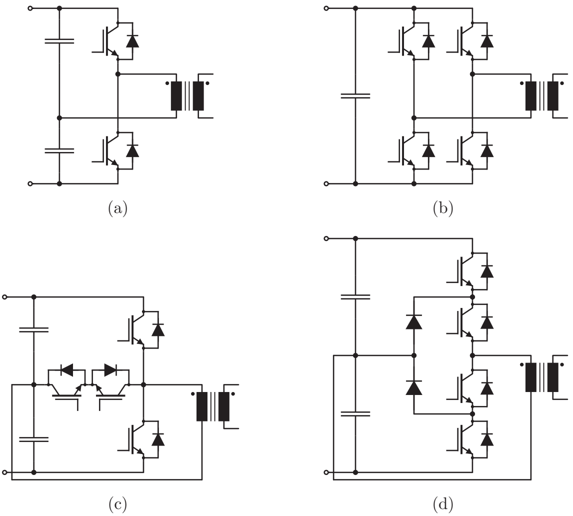
The most prominent modular converter topology in double star connection is the modular multilevel converter (MMC) introduced in [47, 127, 128]. The converter topology employs series-connected unipolar two-level half-bridges (see **Fig. 3.14(a)**) in a converter arm and inherently provides a DC bus. The modules either switch their DC capacitor voltage to the AC output or are bypassed. In this way, similar to the CHB converter, a staircase voltage is formed at each of the phase connections which reaches a nearly sinusoidal waveform by increasing the number of modules per converter arm. The application areas of the MMC cover for instance MV motor drive inverters [129], HVDC power transmission systems for future energy systems [130], reactive power compensators (e.g. STATCOM) [131] or split battery energy storage systems [49, 132].

For providing the galvanic isolation on module level, DC-DC DAB converters (see Section 3.1.1 and **Fig. 3.4**) can be connected to the AC-DC half-bridge modules. This approach is presented for example in [49] for a battery energy storage system applying DC-DC DAB converters with a module-side half-bridge and a battery-side full-bridge. In [133] a microgrid interface based on an MMC for hybrid AC and DC grids is proposed connecting an isolated LV DC bus to both a three-phase AC distribution system and a future MV DC distribution system. The galvanic isolation of the LV DC bus is realized by DC-DC DAB converters which are attached to the module DC capacitors and their isolated outputs connected in parallel.

Single-stage topologies

Possible single-stage solutions in double star connection look like the single star connection depicted in **Fig. 3.9** for a cascade of isolated AC-DC modules or in **Fig. 3.10** for a multi-port structure. Through the interconnection in double star configuration (two single stars in parallel at the phase connections) only unipolar AC-side module blocks are necessary.

In **Fig. 3.15** unipolar isolated AC- or DC-side module blocks with voltage ports for the application in a modular single-stage isolated AC-DC converter in double star connection are shown. The isolated AC-DC modules can be realized by combining two of the blocks, one block for the AC side and one block for the DC side. The most useful variants are the two-level half-bridge, the three-level full-bridge, the three-level T-type and the three-level NPC block.



(a) (b)

(c) (d)

Figure 3.15: Unipolar isolated AC- or DC-side module blocks for the application in a modular single-stage isolated AC-DC converter in double star connection (e.g. modular multilevel converter [47, 127, 128]): (a) two-level half-bridge module block, (b) three-level full-bridge module block, (c) three-level T-type module block, (d) three-level NPC module block.

The use of single-stage isolated AC-DC modules in a double star configuration is a rather special case since neither a constant DC voltage nor a symmetrical AC voltage (constant amplitude, no DC offset) is applied to the voltage port at the module input. As shown later in Section 3.3.4, for the same average module power, the isolation transformer has to cope with a 33 % higher peak power in a double star configuration compared to a single star configuration. From a realization point of view this is not advantageous because the transformer has to be designed for a higher peak power at the same average power.

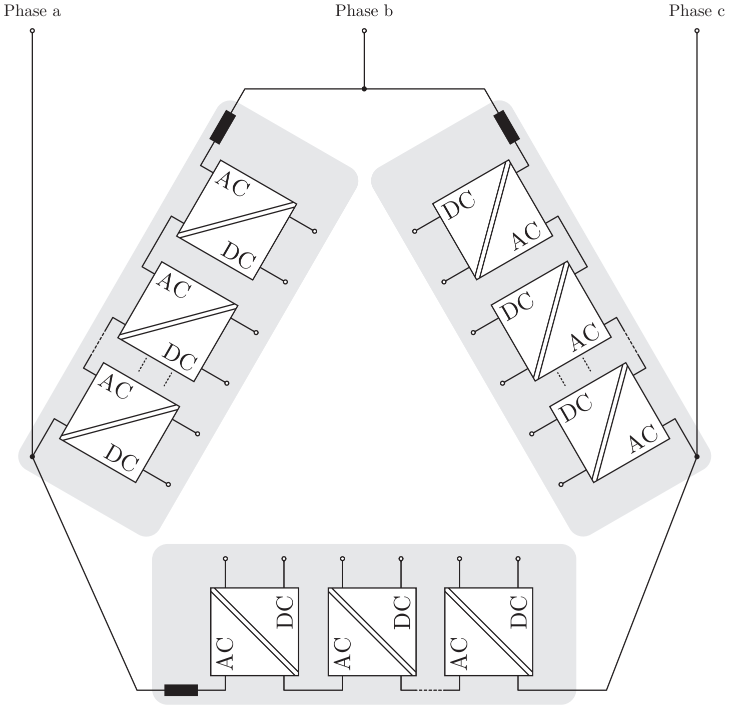


Figure 3.16: General three-phase modular AC-DC topology in delta connection with galvanic isolation on module level. Multiple isolated AC-DC modules per phase-to-phase string are connected in series depending on the MV AC voltage. The split DC outputs of the modules can be connected in series or in parallel.

In theory, any AC-DC DAB converter topology could be used in such a converter system consisting for instance of the module blocks shown in **Fig. 3.15**.

3.2.3 Delta connection

Besides the star and the double star connection also the delta/triangle configuration of series-connected isolated AC-DC modules as depicted in **Fig. 3.16** is possible. As in the case of a star connection, the modules are exposed to a positive and a negative voltage polarity at their AC ports what demands the use of bipolar module inputs (see **Fig. 3.8**, **Fig. 3.11**). Moreover, no MV DC bus is directly available. Suitable single-stage and two-stage isolated module topologies in a delta connection comprise the same solutions as already discussed for the star connection in Section 3.2.1. Compared to the star connection, the voltage across a module branch is increased by a factor of $\sqrt{3}$. For an equivalent delta connection with the same characteristic towards the AC grid, the branch current decreases by $\frac{1}{\sqrt{3}}$.

Proposed modular converter systems in delta connection comprise for example a PWM STATCOM based on a modular multilevel cascade converter [134] or a CHB converter for a split battery energy storage system [54] where each H-bridge module is connected to a storage battery pack.

3.3 Topology selection

Based on the previously presented overview of state-of-the-art bidirectional isolated AC-DC converter topologies (see **Fig. 3.1**), this section deals with the selection of topologies suitable for the AC-DC grid interface in an ultra-fast charging station with integrated battery energy storage system as shown in **Fig. 2.2**. The basic requirements such as the galvanic isolation and the bidirectional power flow are inherently given by the summarized topologies. Further selection criteria as the need of multilevel converters, the phase modularity and scalability, the number of conversion stages and the interconnection possibilities of the converter modules are discussed in the following.

3.3.1 Multilevel converters

For medium voltage applications, topologies like two-level or three-level voltage/current source AC-DC converters require high power semiconductor devices with a high blocking voltage (several kV) and a reasonable current capability. The switching frequency is quite limited (usually no more than some kHz) what induces significant harmonic distortion of the voltages/currents so that the filtering effort becomes relatively high with the need of bulky passive components.

With the use of multilevel topologies, switching devices with lower blocking voltage and therefore lower on-state resistance can be employed what leads to reduced conduction losses and a thermal distribution of the losses across more devices. Moreover, the switching frequency can be increased so that the harmonic content of the voltages/currents is lowered what in turn causes the passive components to shrink. Increasing the number of voltage levels also decreases the harmonic distortion as more levels to create a staircase voltage become available.

On the other hand, a high number of switching devices needs also the corresponding amount of gate drive circuits and increases the hardware complexity of the control. Furthermore, the greater the amount of active components in the design, the more sources of failure exist that could lead to a reduced system reliability.

3.3.2 Phase modularity and scalability

When looking at multilevel topologies as the well-known diode-clamped or capacitor-clamped converter (see **Fig. 3.3** for the five-level examples), the hardware design can get quite complex with a high number of levels as a high number of gate drives is necessary and the commutation paths and therefore the parasitic inductances drastically increase. In the case of a diode-clamped converter, a large amount of diodes is necessary whereas with a capacitor-clamped (flying capacitor) converter an overall large capacitance has to be built into the system. Furthermore, the control of such converters can reach a high complexity as a high number of possible switching states are available as well as capacitor voltages have to be balanced.

With the use of a phase-modular structure, multilevel converter topologies can be built by cascading several equal modules in a series connection depending on the grid voltage specification. Through the modularized approach, such systems are highly scalable in terms of voltage, current and power requirements. Moreover, modular converter systems offer built-in redundancy where in times of a failure single modules can be bypassed without the need of instantly shutting down the whole converter system. From an economic perspective, a modular system is beneficial for mass production with the same components used in every module in order to reduce investment and maintenance costs.

For a battery energy storage system, a modular solution is advantageous over the conventional multilevel topologies since the storage batteries can be distributed among the modules and the state of charges (SOC) easily balanced by controlling the power flow of the modules. An additional balancer circuit is therefore omitted. Another point is the high isolation requirement of the battery packs if a series connection of storage batteries at a MV DC link is used what is rather impractical.

3.3.3 Integration of galvanic isolation

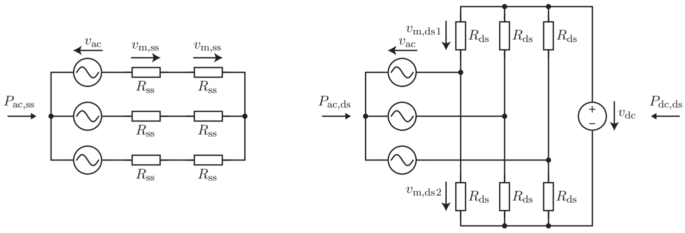
One of the main specifications of the AC-DC grid interface is the integration of galvanic isolation between the AC grid and the DC-side storage batteries. Besides the commonly used two-stage approach with an additional isolated DC-DC converter connected to the module, this work especially focuses on integrating the galvanic isolation on module level in order to develop modular single-stage isolated converter solutions. The main challenges which arise from a single-stage isolated AC-DC module are

- the transfer of the pulsating power with twice the AC grid frequency over the isolation transformer,
- ensuring a sinusoidal AC current shape with a low harmonic distortion and PFC,
- achieving soft-switching conditions over the whole AC module voltage,
- keeping the AC-side voltage within the limits of the blocking voltage capability of the semiconductor devices.

3.3.4 Single versus double star connection

In the following, a simple comparison of the single and the double star connection of a modular AC-DC converter suitable for a battery energy storage system is shown. Since the delta connection requires a higher module branch voltage compared to the star configuration it is excluded from the selection of a module interconnection.

Fig. 3.17 shows the basic schematics of a single star and a double star connection where the modules are modeled as ohmic loads $R_{\mathrm{ss}}, R_{\mathrm{ds}}$. The model represents the charging operation of a battery energy storage system where the module behaviour is assumed to be purely passive and the reactive power drawn from filter components is neglected. The goal is to investigate the time-dependent module power that has to be transferred over the isolation transformer to compare the single and the double star configuration. The comparison is done for the same number of modules (ohmic loads), the same total power feed-in and an equal AC voltage grid. In the case of the double star configuration, an additional DC voltage grid is connected.


v_{ac}
$v_{\mathrm{m,ss}}$
$v_{\mathrm{m,ss}}$
R_{ss}
R_{ss}
$P_{\mathrm{ac,ss}}$
R_{ss}
R_{ss}
R_{ss}
R_{ss}
$v_{\mathrm{m,ds1}}$
v_{ac}
R_{ds}
R_{ds}
R_{ds}
$P_{\mathrm{ac,ds}}$
+
−
v_{dc}
$P_{\mathrm{dc,ds}}$
$v_{\mathrm{m,ds2}}$
R_{ds}
R_{ds}
R_{ds}

(a) (b)

Figure 3.17: Basic schematic of a single star connection (e.g. CHB) (a) with the modules modeled as equal ohmic loads R_{ss} and power feed-in $P_{\mathrm{ac,ss}}$ as well as of a double star connection (e.g. MMC) (b) with the modules modeled as ohmic loads R_{ds} and the power feed-in $P_{\mathrm{ac,ds}} + P_{\mathrm{dc,ds}}$. The two circuits exhibit the same number of modules (ohmic loads), the same total power feed-in and are connected to an equal AC voltage grid. The double star configuration is additionally connected to a DC voltage grid.

Given a purely sinusoidal three-phase AC voltage grid with

$$v_{\mathrm{ac}} = \frac{v_{\mathrm{dc}}}{2} \sin(\omega t) \tag{3.1}$$

and thus assuming constant star-point voltages the module voltage in single star connection is given by

$$v_{\mathrm{m,ss}} = \frac{v_{\mathrm{ac}}}{N_{\mathrm{ss}}} \tag{3.2}$$

with N_{ss} being the number of modules in a phase string. The module power is then written as

$$p_{\mathrm{m,ss}} = \frac{v_{\mathrm{m,ss}}^2}{R_{\mathrm{ss}}} = \frac{v_{\mathrm{ac}}^2}{N_{\mathrm{ss}}^2 R_{\mathrm{ss}}}. \tag{3.3}$$

For the double star connection with N_{ds} number of modules per phase string (two arms) the module voltage in the upper arm is

$$v_{\mathrm{m,ds1}} = \frac{\frac{v_{\mathrm{dc}}}{2} - v_{\mathrm{ac}}}{N_{\mathrm{ds}}} \tag{3.4}$$

whereas in the lower arm

$$v_{\mathrm{m,ds2}} = \frac{\frac{v_{\mathrm{dc}}}{2} + v_{\mathrm{ac}}}{N_{\mathrm{ds}}}. \tag{3.5}$$

The module power in the upper arm is then calculated as

$$p_{\mathrm{m,ds1}} = \frac{v_{\mathrm{m,ds1}}^2}{R_{\mathrm{ds}}} = \frac{\left(\frac{v_{\mathrm{dc}}}{2} - v_{\mathrm{ac}}\right)^2}{N_{\mathrm{ds}}^2 R_{\mathrm{ds}}} \tag{3.6}$$

and in the lower arm as

$$p_{\mathrm{m,ds2}} = \frac{v_{\mathrm{m,ds2}}^2}{R_{\mathrm{ds}}} = \frac{\left(\frac{v_{\mathrm{dc}}}{2} + v_{\mathrm{ac}}\right)^2}{N_{\mathrm{ds}}^2 R_{\mathrm{ds}}}. \tag{3.7}$$

For the same average module power $p_{\mathrm{m,avg}}$ over a 50 Hz grid cycle **Fig. 3.18** depicts the time-dependent module power $p_{\mathrm{m,ss}}$, $p_{\mathrm{m,ds1}}$, $p_{\mathrm{m,ds2}}$ normalized to the peak module power in single star connection. Each phase string applies two modules, so that $N_{\mathrm{ss}} = N_{\mathrm{ds}} = 6$. It can be seen that for the same average module power a 33 % higher peak power occurs in a double star connection compared to a single star or delta connection that has to be considered in the isolation transformer design. This phenomenon is inherently given by a converter in double star connection (e.g. MMC) where the power flows mainly in the lower arm during the positive half-wave (modules in the upper arm are mainly bypassed) and through the upper arm during the negative half-wave of the AC grid voltage (modules in the lower arm are mainly bypassed). This is also clearly seen from the curves $p_{\mathrm{m,ds1}}, p_{\mathrm{m,ds2}}$ given in **Fig. 3.18**.

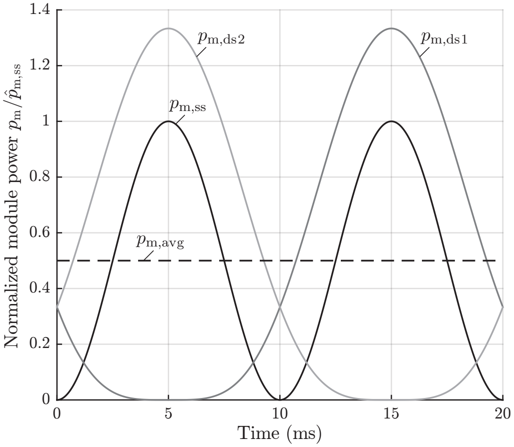


Figure 3.18: Comparison of the module input power in star connection (CHB based) and in double star connection (MMC based) with the series-connected modules modeled as equal ohmic loads (see **Fig. 3.17**) for the same number of modules ($N_{\mathrm{ss}} = N_{\mathrm{ds}} = 6$) and the same average module power $p_{\mathrm{m,avg}}$ (over a 50 Hz grid cycle). The overall converter power in single star connection (AC port power feed-in $P_{\mathrm{ac,ss}}$) equals the one of the double star connection (AC and DC port power feed-in $P_{\mathrm{ac,ds}} + P_{\mathrm{dc,ds}}$).

Besides the module power, the module voltages $v_{\mathrm{m,ss}}$, $v_{\mathrm{m,ds1}}$, $v_{\mathrm{m,ds2}}$ are given in **Fig. 3.19** together with the AC grid voltage v_{ac}. The voltages are normalized to the peak module voltage in single star connection. The module voltages in double star connection exhibit only positive polarity with twice the peak-to-peak voltage than the modules in single star connection. For the same number of modules this is obvious since in single star connection the AC voltage v_{ac} can be distributed among double the number of modules compared to a double star connection.

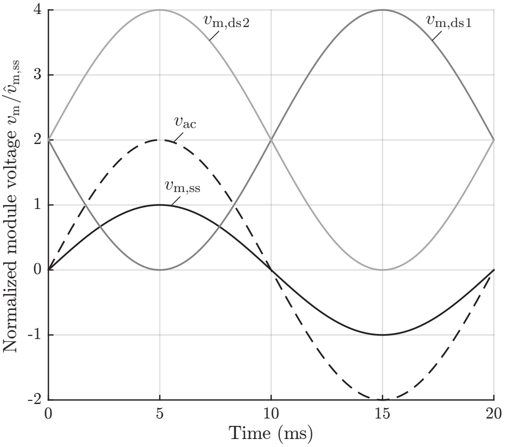


Figure 3.19: Comparison of the module input voltage in star connection (CHB based) and in double star connection (MMC based) with the series-connected modules modeled as equal ohmic loads (see **Fig. 3.17**) for the same number of modules ($N_{\mathrm{ss}} = N_{\mathrm{ds}} = 6$) and the same average module power $p_{\mathrm{m,avg}}$ (over a 50 Hz grid cycle). The AC grid voltage v_{ac} in single star connection equals the one of the double star connection. For the same number of modules, the double star connection exhibits twice the peak-to-peak module voltage.

Concluding the investigations on module level in single and double star connection, for a battery energy storage system with single-stage isolated AC-DC modules the single star configuration is the most suitable since the isolation transformer can be designed for a lower peak power if the same overall amount of modules is considered. Usually the additional MV DC link that is available in double star connection is not needed for the single purpose of storing energy in a MV AC distribution grid.

3.3.5 Focus of this work

Based on the selection criteria discussed above, for the ultra-fast charging station with an integrated battery energy storage system a phase-modular single-stage AC-DC grid interface solution in a single star connection is chosen. As shown in [135] for a battery energy storage system, a CHB converter with split storage batteries is generally better suited than an MMC with a bulky battery at the MV DC link since higher efficiencies can be reached and the balancing control of the batteries gets easier. Nevertheless, also with the MMC the battery packs can be distributed among the modules [132], but usually the MV DC link is not needed for a pure grid storage system.

In the following chapters, mainly two phase-modular single-stage AC-DC converter topologies are proposed and investigated. These are

- the cascaded AC-DC DAB converter,
- the cascaded AC-DC multi-port converter with a three-phase AC port and a DC port.

For the topologies, suitable modulation schemes are developed and optimized with respect to converter efficiency and power density. Moreover, control algorithms are presented for the overall battery energy storage system in order to balance the SOCs of the battery packs. For each of the considered converter systems, a module prototype is designed and its key performance indicators as efficiency and power density evaluated. Additionally, for the cascaded AC-DC DAB converter, a hardware prototype of a module is built to validate the proposed modulation scheme and its practical applicability.

Finally, the proposed converter modules are compared to the standard CHB-based solution consisting of a full-bridge input stage and an isolated DC-DC DAB converter in terms of efficiency and power density by implementing a multi-objective optimization for each module topology. This allows to identify the main advantages and drawbacks of the integration of galvanic isolation on module level and to draw a final conclusion.

4

Cascaded AC-DC Dual Active Bridge Converter

In this chapter, a new cascaded AC-DC dual active bridge (DAB) converter for battery energy storage systems is proposed. The topology is derived from a state-of-the-art cascaded H-bridge (CHB) converter and integrates module-level galvanic isolation using series-connected single-stage bidirectional isolated AC-DC converter modules. For the topology, suitable modulation and control schemes both on module as well as on system level are developed. A converter module is designed, its components and losses modeled and a hardware prototype built to validate the proposed modulation schemes. Finally, the overall battery energy storage system is simulated to validate the theoretical analysis on module and system level.

4.1 Converter topology

The CHB converter proposed in [48, 89] represents the basic topology from which the cascaded AC-DC DAB converter depicted in **Fig. 4.1** with a module exemplarily shown for phase b is derived. The converter consists of three phase strings/legs which are tied together at a common star point. In a phase string, several bidirectional isolated AC-DC modules are connected in series with a filter inductor L_{ac}. Each of the modules exhibit a grid-side low-frequency (LF) AC voltage port (with capacitors C_{ac}) and a DC voltage port (with capacitor C_{dc}).

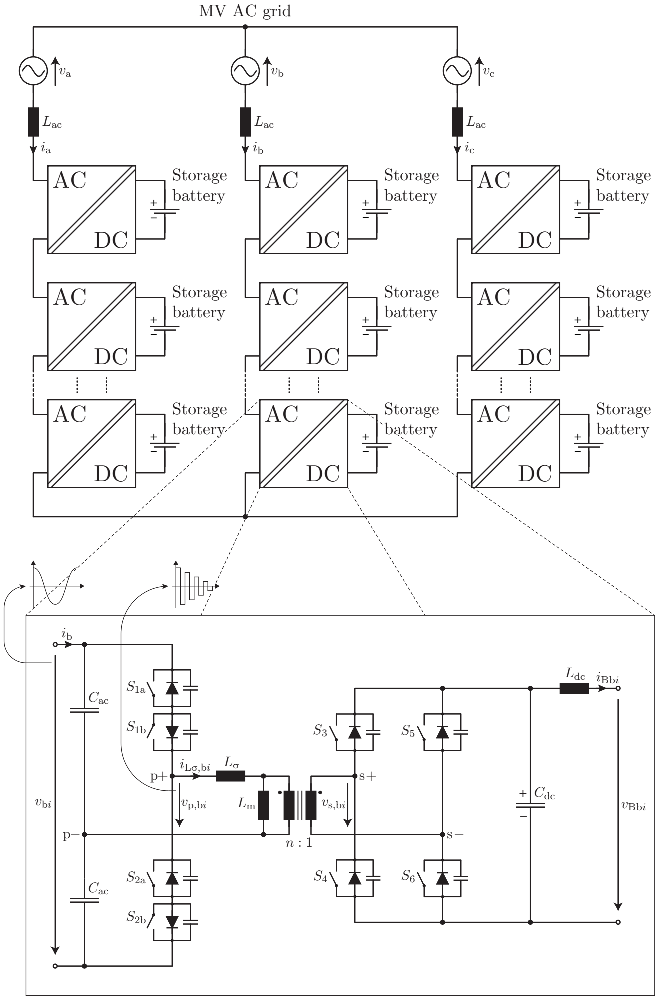
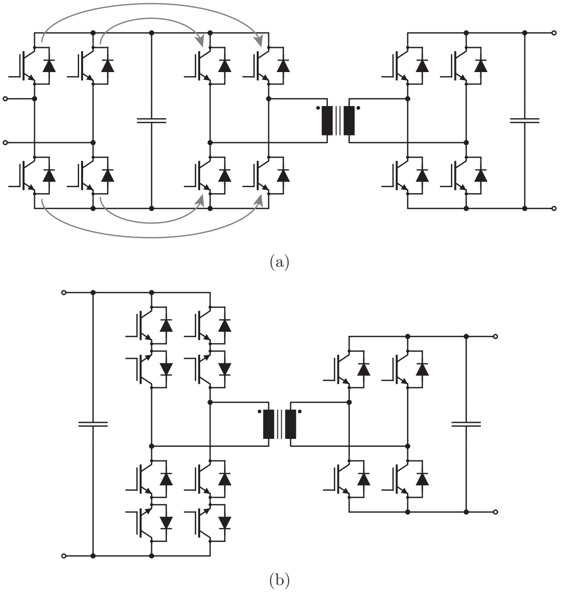

MV AC grid
v_{a}
v_{b}
v_{c}
L_{ac}
L_{ac}
L_{ac}
i_{a}
i_{b}
i_{c}
AC
DC
Storage battery
+
−
i_{b}
C_{ac}
$S_{1\mathrm{a}}$
$S_{1\mathrm{b}}$
$i_{\mathrm{L}\sigma,\mathrm{b}i}$
L_{σ}
p+
p−
$v_{\mathrm{b}i}$
$v_{\mathrm{p,b}i}$
L_{m}
$v_{\mathrm{s,b}i}$
$n:1$
s+
s−
S_3
S_5
S_4
S_6
$S_{2\mathrm{a}}$
$S_{2\mathrm{b}}$
C_{ac}
L_{dc}
$i_{\mathrm{Bb}i}$
C_{dc}
$v_{\mathrm{Bb}i}$

Figure 4.1: Cascaded AC-DC DAB converter in star connection for battery energy storage systems with series-connected AC-DC DAB modules applying grid-side half-bridges with bidirectional switches, battery-side full-bridges with unidirectional switches and medium-frequency transformers providing galvanic isolation. Each module is connected to a storage battery at the DC side. The module input voltage $v_{\mathrm{b}i}$ corresponds to a sinusoidal voltage waveform with the grid frequency.

The DC voltage port is connected through a filter inductor L_{dc} to a storage battery. The module topology is basically a DAB converter with a grid-side half-bridge applying bidirectional switches and a battery-side full-bridge applying unidirectional switches. The medium-frequency (MF) transformer provides the galvanic isolation between the medium voltage (MV) grid and the storage battery, so that the batteries can be connected to earth for safety reasons and do not have to be designed for a high insulation voltage. Nevertheless, the module transformer has to be designed for the appropriate insulation voltage for the application in such a converter system. The transformer is modeled by the primary referred leakage inductance L_σ and the magnetizing inductance L_{m}. The ratio between the AC-side number of turns N_{p} and the DC-side number of turns N_{s} is given by the turns ratio $n = \frac{N_{\mathrm{p}}}{N_{\mathrm{s}}}$.



(a)

(b)

Figure 4.2: Conventional two-stage bidirectional isolated module topology with an H-bridge input stage and a DC-DC DAB converter (a) in a CHB converter from which the single-stage AC-DC DAB converter module (b) can be derived by distributing the switches of the H-bridge input stage to the grid-side full-bridge of the DAB converter.

4.1.1 From two-stage to single-stage module

The module topology shown in **Fig. 4.1** is derived from a conventional two-stage solution connecting a DC-DC isolation stage to the H-bridge module of a CHB converter as previously shown in **Fig. 3.7** and presented in [95–98]. This is shown in **Fig. 4.2(a)** where a standard DAB converter is employed. One step further, the switches of the H-bridge module can be distributed to the grid-side full-bridge of the DAB converter as depicted in **Fig. 4.2(b)** forming a full-bridge with bidirectional switches.

4.1.2 AC-DC dual active bridge module topologies

Besides the DAB applying two three-level full-bridges (dual full-bridge (DFB) converter), also topologies applying two-level half-bridges, three-level T-type or NPC circuits and any combination of them are possible (see **Fig. 3.11** for possible AC-side circuits and **Fig. 3.12** for possible DC-side circuits). The combinations considering half-bridge, full-bridge and T-type circuits are summarized in **Tab. 4.1** where the degrees of freedom in control for a symmetrical duty cycle operation are listed. The asymmetrical duty cycle operation as for instance discussed in [136] for a dual half-bridge (DHB) converter with an additional control variable for capacitor voltage balancing is not considered. In contrast to the majority of proposed modulation schemes for DAB converters, in this work also the switching frequency is used as a control variable.

Degrees of freedom in control

The AC-DC DAB derived above and shown in **Fig. 4.2** offers four degrees of freedom (see **Tab. 4.1**): The two clamping intervals of the AC- and the DC-side full-bridges, the phase shift in between as well as the switching frequency. The degrees of freedom in control for the AC-DC module are used for

- the AC current shaping (power transfer constraint),
- maintaining soft-switching conditions in terms of ZCS and/or ZVS,
- the minimization of the transformer RMS currents.

Table 4.1: Possible two-/three-level AC-DC DAB circuit topologies with their degrees of freedom in control. Only symmetrical duty cycle operation is considered.

Circuit 1	Circuit 2	Degrees of freedom in control
Half-bridge	Half-bridge	Phase shift, switching frequency (2)
Half-bridge	Full-bridge	Phase shift, 1 clamping interval, switching frequency (3)
Half-bridge	T-type	Phase shift, 1 clamping interval, switching frequency (3)
Full-bridge	Full-bridge	Phase shift, 2 clamping intervals, switching frequency (4)
Full-bridge	T-type	Phase shift, 2 clamping intervals, switching frequency (4)
T-type	T-type	Phase shift, 2 clamping intervals, switching frequency (4)

A minimum of two degrees of freedom is necessary for a proper operation of the module under soft-switching conditions, a third and a fourth one can be utilized for optimization purposes. Restricting the module to three degrees of freedom, the number of semiconductor devices can be reduced from twelve (AC full-bridge, DC full-bridge) to eight (AC half-bridge, DC full-bridge) what significantly reduces the hardware control effort in terms of gate drives and the overall system costs. The resulting AC-DC module topology is depicted in **Fig. 4.1** for the application in the battery energy storage system. Despite losing a degree of freedom, with taking the switching frequency into consideration for control, still one degree of freedom for optimizing the transformer RMS currents is available.

In terms of control possibilities, a T-type circuit is comparable to a full-bridge circuit (see **Tab. 4.1**) with the same amount of switches. For the bidirectional clamping switch, semiconductor devices with a lower voltage rating are used and a split DC link capacitor is needed. Nevertheless, using semiconductor devices with the same voltage rating is in most cases beneficial since system costs can be reduced.

Qualitative comparison of semiconductor losses

Considering the same chip area per semiconductor device and in total and assuming a relatively small clamping interval, with a full-bridge efficiencies tend to be higher than with a T-type circuit since the transformer voltage amplitude is doubled and the switch RMS currents divided by two for the same power operating point (this is due to the quadratic dependency of the conduction losses on the switch current, see **Tab. 4.2**). The use of a T-type circuit where the conduction interval of the clamping switch is relatively small is not favorable because the spent chip area for this switch could (or should) be distributed to the other two switches resulting in the end in the basic half-bridge circuit. Theoretically, the chip sizes of the switches can be optimized for minimum losses for an overall constant chip area as described in [137]. The chip area for devices with low losses is decreased whereas the one with high losses is increased. Since only chips with a discrete chip size are available for a hardware realization, the practical application of such an optimization is rather limited.

A simple comparison of the conduction and switching losses of DC-side DAB circuits is given in **Tab. 4.2** for R_s being the on-state re-

Table 4.2: Comparison of DC-side DAB circuit topologies in terms of conduction and switching losses for the same chip area per semiconductor device and in total (same total number of switches) at the same power operating point assuming full-block voltage operation without clamping. R_s represents the on-state resistance and $E_\mathrm{s} = E_\mathrm{on} + E_\mathrm{off}$ the switching loss energy of one semiconductor device rated for the full DC link voltage. The bidirectional clamping switch of the T-type circuit is not considered to be switched and conducting.

Circuit	**Switch resistance**[a]	**Switch current**[b]	**Conduction losses**	**Switching losses**
Half-bridge	$\frac{R_\mathrm{s}}{2}$	$2I_\mathrm{s}$	$2R_\mathrm{s}I_\mathrm{s}^2$	$4E_\mathrm{s}f_\mathrm{s}$
Full-bridge	$2R_\mathrm{s}$	I_s	$2R_\mathrm{s}I_\mathrm{s}^2$	$4E_\mathrm{s}f_\mathrm{s}$
T-type	R_s	$2I_\mathrm{s}$	$4R_\mathrm{s}I_\mathrm{s}^2$	$4E_\mathrm{s}f_\mathrm{s}$

---

[a] This corresponds to the total on-state resistance in the current path.

[b] This is the RMS switch current over a switching period (50 % on-state, 50 % off-state).

sistance and $E_\mathrm{s} = E_\mathrm{on} + E_\mathrm{off}$ being the switching loss energy of one semiconductor device rated for the full DC link voltage. In case of the T-type circuit, the losses are obviously higher since the spent chip area of the clamping switch is not used in full-block voltage operation. The half-bridge and the full-bridge circuits are comparable in terms of losses since the two switches of one leg of the full-bridge can be used for parallelization of two switches in the half-bridge circuit. For a simple comparison, the switching energy E_s is linearly scaled with the switch current which approximately models the device characteristic of an IGBT [137].

From the above discussion and with the requirement in degrees of freedom, the usage of a full-bridge as a DC-side DAB circuit is confirmed. Since commonly the clamping interval is minimized in order to reduce the circulating current and therefore the reactive power, the use of a full-bridge is more beneficial than using a T-type circuit.

4.2 Operating principle

For the explanation of the operating principle of the cascaded AC-DC DAB converter, a simple grid-side equivalent circuit as shown in **Fig. 4.3** can be drawn. There, the AC-DC modules are modeled by their capacitive voltage ports consisting of the series connection of two filter capacitors C_ac and a controlled current source $i_{\mathrm{mb}i}$ exemplarily for the module $i \in \{1, 2, ..., n\}$ in the phase string b. The DAB converter is modeled by the transformer leakage inductance L_σ and the AC- and DC-side applied MF voltages $v_{\mathrm{p,b}i}$, $v'_{\mathrm{s,b}i}$ (AC-side referred) at the transformer windings. The transformer magnetizing inductance L_m is assumed to be relatively large, so that the magnetizing current can be neglected for the analysis of the operating principle.

4.2.1 Module level

By adjusting the power transfer of the AC-DC DAB module, the current source $i_{\mathrm{mb}i}$ is controlled in order to regulate the AC-side module voltage $v_{\mathrm{b}i}$ and hence the grid current i_b. The current driven by the source can be written as

$$i_{\mathrm{mb}i} = i_\mathrm{b} - i_{\mathrm{Cb}i} \tag{4.1}$$

with $i_{\mathrm{Cb}i}$ being the current flowing through the AC-side capacitors.

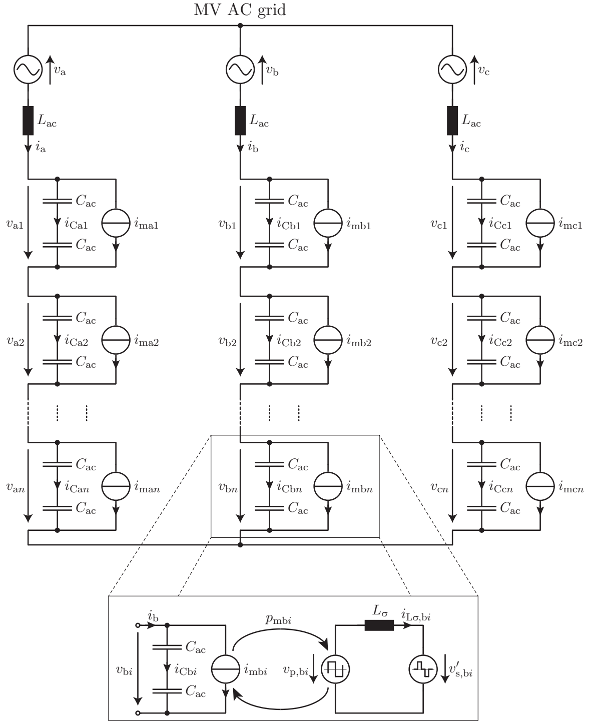

MV AC grid
v_{a}
v_{b}
v_{c}
L_{ac}
i_{a}
i_{b}
i_{c}
C_{ac}
v_{a1}
i_{Ca1}
i_{ma1}
v_{b1}
i_{Cb1}
i_{mb1}
v_{c1}
i_{Cc1}
i_{mc1}
v_{a2}
i_{Ca2}
i_{ma2}
v_{b2}
i_{Cb2}
i_{mb2}
v_{c2}
i_{Cc2}
i_{mc2}
$v_{\mathrm{a}n}$
$i_{\mathrm{Ca}n}$
$i_{\mathrm{ma}n}$
$v_{\mathrm{b}n}$
$i_{\mathrm{Cb}n}$
$i_{\mathrm{mb}n}$
$v_{\mathrm{c}n}$
$i_{\mathrm{Cc}n}$
$i_{\mathrm{mc}n}$
$p_{\mathrm{mb}i}$
L_σ
$i_{\mathrm{L}\sigma,\mathrm{b}i}$
$v_{\mathrm{b}i}$
$i_{\mathrm{Cb}i}$
$i_{\mathrm{mb}i}$
$v_{\mathrm{p,b}i}$
$v'_{\mathrm{s,b}i}$

Figure 4.3: Grid-side equivalent circuit of the cascaded AC-DC DAB converter shown in **Fig. 4.1**. The modules are modeled with their capacitive voltage ports consisting of the series connection of two filter capacitors C_{ac} and a controlled current source $i_{\mathrm{mb}i}$. By adjusting the power transfer of a DAB module, the current source is controlled in order to regulate the AC-side module voltage as well as the grid current. The DAB module is modeled by the transformer leakage inductance L_σ and the AC- and DC-side applied medium-frequency voltages $v_{\mathrm{p,b}i}$, $v'_{\mathrm{s,b}i}$ (AC-side referred) at the transformer windings.

The operating principle is comparable to a conventional CHB converter where a phase shift PWM is used to directly generate the grid-side module voltages [96, 97]. The major difference is, that the module voltage $v_{\mathrm{b}i}$ is indirectly controlled by the power transfer of the DAB converter which is given by

$$p_{\mathrm{mb}i} = v_{\mathrm{b}i} i_{\mathrm{mb}i} = v_{\mathrm{b}i} \left(i_{\mathrm{b}} - i_{\mathrm{Cb}i} \right). \tag{4.2}$$

The power coupling between the controlled current source $i_{\mathrm{mb}i}$ and the MF voltage source $v_{\mathrm{p,b}i}$ is represented by the two arrows shown in **Fig. 4.3**. The power transfer between the MF voltage sources $v_{\mathrm{p,b}i}$, $v'_{\mathrm{s,b}i}$ is dependent on the control variables of the employed modulation scheme such as the phase shift, the DC-side clamping interval and the switching frequency (see **Tab. 4.1**). The details of the modulation schemes are described in Section 4.3.

During one half-cycle of the grid-side AC voltage, two of the grid-side semiconductor devices in the bidirectional switches are constantly turned on. These are $S_{1\mathrm{b}}$ and $S_{2\mathrm{b}}$ for the positive and $S_{1\mathrm{a}}$ and $S_{2\mathrm{a}}$ for the negative half-wave (see **Fig. 4.1**).

4.2.2 System level

Controlling the AC-side module voltages in a phase string allows to apply the corresponding voltage across the grid filter inductor L_{ac} which leads to the required amplitude and phase of the grid current. For the battery energy storage system depicted in **Fig. 4.1**, purely active power in charging and discharging operation is considered with a power factor (PF) near unity. Moreover, since all modules in a phase string are connected in series, the power distribution among the modules can only be set by controlling the grid-side voltages of the modules as the module currents are equal.

By increasing the voltage of a module, the voltage of another module or the voltages of other modules in the same phase string have to be reduced, so that the voltage sum of all modules is not changed. In this way, only the power distribution among the modules is affected, but not the overall power flow between the grid and the batteries. The upper limit of the module power is basically given by the blocking voltage of the applied semiconductor devices.

At the grid side, each module can be simply represented by a voltage source (capacitive voltage port controlled by a current source as depicted in **Fig. 4.3**) where the voltage is controlled by the power transfer between the grid-side filter capacitors C_{ac} and the battery. To increase the module power, first the module voltage $v_{\mathrm{b}i}$ has to be increased which is done by reducing the power transfer to the battery. As soon as the module voltage rises, the power transfer can be increased again to reach its reference value. This is done by a module voltage controller as described in Section 4.4.5.

4.3 Module modulation schemes

A DAB converter is operated by actively applying square-wave voltages with or without clamping interval (zero voltage interval) across the windings of the transformer. The voltages can be seen as MF voltage sources which are decoupled by the leakage inductance of the transformer (see equivalent circuit of a DAB module in **Fig. 4.3**). By adjusting the phase shift between the square-wave voltages, the transformer leakage inductance current can be shaped in order to control the power flow and to allow beneficial conditions for the soft-switching of the semiconductor devices. Advanced modulation schemes not only use the phase shift, but also the clamping interval and/or the switching frequency as control variables (see **Tab. 4.1**).

For the theoretical analysis of the modulation schemes of a DAB module, the following assumptions are made:

- The magnetizing current is negligible small (means large magnetizing inductance L_m),
- the capacitors C_ac, C_dc are large enough so that the amplitudes of the generated square-wave voltages can be considered constant during one switching cycle,
- the switching frequency is well above the resonant frequency of the resonant tank formed by C_ac, C_dc and L_σ,
- the commutation intervals are negligible small in comparison to the switching cycle,
- the transformer turns ratio guarantees that the module is always operated in boost mode when the DC voltage is referred to the AC side.

Based on these, the transformer leakage inductance current is approximated by piecewise linear equations with no DC offset since the square-wave voltages applied to the transformer windings exhibit a zero voltage-second product over a switching cycle. This also guarantees that no DC flux appears in the transformer core.

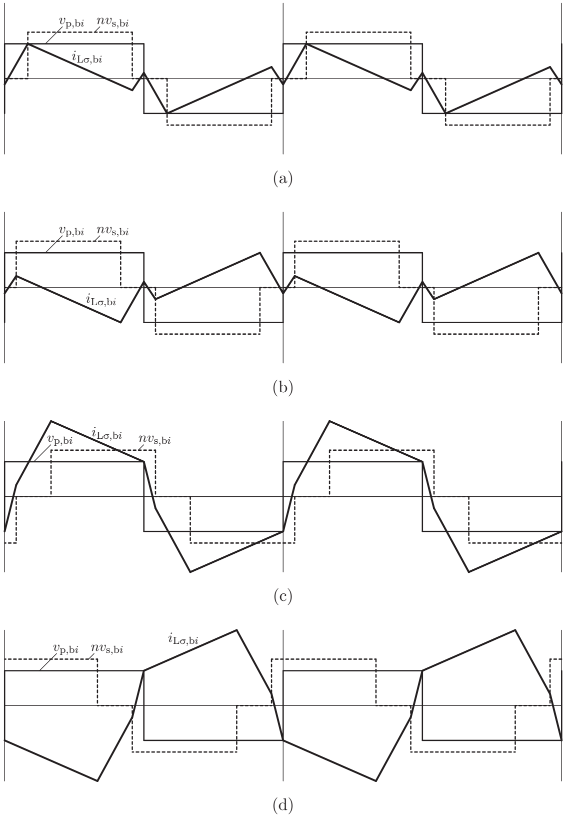


Figure 4.4: Possible and reasonable modulation schemes in boost mode for a DAB module with a grid-side half-bridge and a battery-side full-bridge with the transformer voltages $v_{\mathrm{p,b}i}$, $v_{\mathrm{s,b}i}$ applied to the AC-side and the DC-side winding of the module transformer with turns ratio n as well as the resulting leakage inductance current $i_{\mathrm{L}\sigma,\mathrm{b}i}$ referred to the AC side: (a) *inner mode* with a power transfer from the grid to the battery, (b) *inner mode* with a power transfer from the battery to the grid, (c) *lagging outer mode* with a power transfer from the grid to the battery, (d) *leading outer mode* with a power transfer from the battery to the grid.

The most prominent modulation scheme only uses the phase shift for controlling the power flow from the primary side to the secondary side of the transformer [73, 74]. Especially for a high power transfer and a square-wave voltage amplitude ratio close to unity (both voltages referred to the same side of the transformer), this modulation scheme is beneficial since soft-switching in terms of ZVS is possible and only a small amount of reactive power occurs (interval to change the sign of the current). For part load conditions, with two full-bridges, the clamping intervals can be used which leads to the trapezoidal and the triangular current mode modulation [138, 139].

For the AC-DC DAB module with an AC-side half-bridge and a DC-side full-bridge, the possible and reasonable modulation schemes in boost mode are depicted in **Fig. 4.4**. The modulation modes resulting from phase-shifting the battery-side voltage signal by 180° are not shown since these modes lead to high transformer peak currents and a high amount of reactive power (increased conduction losses). **Fig. 4.4(a)** and **Fig. 4.4(b)** show the *inner mode* where the DC-side voltage block lies completely inside the AC-side voltage block for the two power flow directions. In **Fig. 4.4(c)** the *lagging outer mode* with a power transfer from the grid to the battery is depicted and in **Fig. 4.4(d)** the *leading outer mode* with a power transfer from the battery to the grid is shown. The conventional phase shift modulation is inherently given by the *lagging outer mode* and the *leading outer mode* by setting the DC-side clamping interval to zero.

In the following, two modulation schemes are presented in detail - a first one which allows ZCS at the grid side with IGBTs and ZVS at the battery side with MOSFETs (presuming a constant switching frequency) and a second one which allows ZVS on both sides with MOSFETs (considering also switching frequency variation).

4.3.1 ZCS/ZVS modulation with fixed switching frequency

The *inner mode* as well as the *lagging outer mode* shown in **Fig. 4.4(a)** and **Fig. 4.4(c)** can be restricted such that the grid-side half-bridge switches always at zero current (ZCS). This is done by setting the current $i_{\mathrm{L}\sigma,\mathrm{b}i}$ at τ_0 and τ_3 to zero as shown in **Fig. 4.5** which leaves two degrees of freedom in control (see **Tab. 4.1**). At the switching instants τ_1, τ_2, τ_4 and τ_5 ZVS is possible as long as the transformer current exceeds the minimum commutation current needed for the resonant transition.

The resulting modulation schemes are a *low power mode* depicted in **Fig. 4.5(a)** and a *high power mode* in **Fig. 4.5(b)**. Since the power flow in *high power mode* cannot be substantially reduced (see (4.26) below) for the relatively low instantaneous power transfer required near the zero-crossing of the AC grid voltage (PFC operation assumed), the modulation has to be changed to the *low power mode* with a seamless transition in between. During the mode transition, ZVS cannot be maintained as the transformer current decreases below the minimum commutation current such that partly hard-switching occurs.

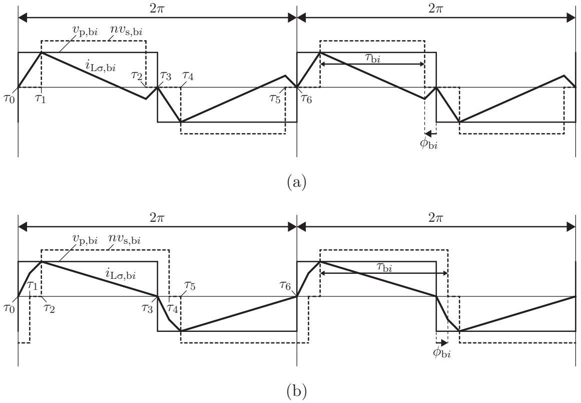


Figure 4.5: Medium-frequency voltages $v_{\mathrm{p,b}i}, nv_{\mathrm{s,b}i}$ applied to the transformer windings of a module and the resulting leakage inductance current $i_{\mathrm{L}\sigma,\mathrm{b}i}$ in *low power mode* (a) and *high power mode* (b) over a switching cycle $T_\mathrm{s} = \frac{2\pi}{\omega_\mathrm{s}}$ for a power transfer from the grid to the battery. The modulation scheme guarantees grid-side ZCS and battery-side ZVS, so that IGBTs can be used at the grid side and MOSFETs at the battery side.

Varying the switching frequency is not considered, as the mode change has to occur at a phase shift $\phi_{\mathrm{b}i}$ of zero (see **Fig. 4.5**) and a fixed switching frequency in order to guarantee continuous control variables over time. The switching frequency could be increased in *high power mode* to decrease the power transfer up to a certain limit where the modulation has to be changed to the *low power mode*. But this also requires that the phase shift is continuously decreased until this point is reached to allow a seamless transition between the modes. These transition constraints do not allow an independent optimization of the control variables for the two modes in order to minimize the transformer leakage inductance RMS current under the soft-switching constraints.

For the following mathematical analysis in grid-to-battery operation, the transformer turns ratio guarantees that $nv_{\mathrm{s,b}i} > v_{\mathrm{p,b}i}$ in every point of the AC module voltage $v_{\mathrm{b}i}$ (boost mode). The control variables for the power flow are the battery-side pulse width $\tau_{\mathrm{b}i} \in [0, \pi]$ and the phase shift $\phi_{\mathrm{b}i} \in [-\pi, \pi]$ in relation to the grid-side applied voltage $v_{\mathrm{p,b}i}$ as shown in **Fig. 4.5** both measured in rad. In *low power mode* $\phi_{\mathrm{b}i}$ is negative and in *high power mode* positive. The mode change occurs at $\phi_{\mathrm{b}i} = 0$. The derivation of the modulation in battery-to-grid operation is not given as it can be done analogously.

Low power mode

By using piecewise linear equations, the AC-side referred transformer leakage inductance current $i_{\mathrm{L}\sigma,\mathrm{b}i}$ in *low power mode* over a switching cycle $T_{\mathrm{s}} = \frac{2\pi}{\omega_{\mathrm{s}}}$ with the angular frequency ω_{s} is given by

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau) = \begin{cases} \dfrac{\frac{|v_{\mathrm{b}i}|}{2}}{\omega_{\mathrm{s}} L_\sigma}(\tau - \tau_0) + i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_0) & \tau_0 \le \tau \le \tau_1 \\ \dfrac{\frac{|v_{\mathrm{b}i}|}{2} - nv_{\mathrm{Bb}i}}{\omega_{\mathrm{s}} L_\sigma}(\tau - \tau_1) + i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_1) & \tau_1 \le \tau \le \tau_2 \\ \dfrac{\frac{|v_{\mathrm{b}i}|}{2}}{\omega_{\mathrm{s}} L_\sigma}(\tau - \tau_2) + i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_2) & \tau_2 \le \tau \le \tau_3 \\ \dfrac{-\frac{|v_{\mathrm{b}i}|}{2}}{\omega_{\mathrm{s}} L_\sigma}(\tau - \tau_3) + i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_3) & \tau_3 \le \tau \le \tau_4 \\ \dfrac{-\frac{|v_{\mathrm{b}i}|}{2} + nv_{\mathrm{Bb}i}}{\omega_{\mathrm{s}} L_\sigma}(\tau - \tau_4) + i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_4) & \tau_4 \le \tau \le \tau_5 \\ \dfrac{-\frac{|v_{\mathrm{b}i}|}{2}}{\omega_{\mathrm{s}} L_\sigma}(\tau - \tau_5) + i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_5) & \tau_5 \le \tau \le \tau_6 \end{cases} \tag{4.3}$$

with $\tau_0 = 0$, $\tau_6 = 2\pi$ and $|v_{\mathrm{b}i}|$ being the absolute value of the instantaneous AC module voltage and $v_{\mathrm{Bb}i}$ the battery voltage. The values of the transformer current at the switching instants are

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_0) = 0, \tag{4.4}$$

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_1) = \frac{\frac{|v_{\mathrm{b}i}|}{2}\left(\pi - \tau_{\mathrm{b}i} + \phi_{\mathrm{b}i}\right)}{\omega_{\mathrm{s}} L_\sigma}, \tag{4.5}$$

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_2) = \frac{\frac{|v_{\mathrm{b}i}|}{2}\left(\pi + \phi_{\mathrm{b}i}\right) - n v_{\mathrm{Bb}i}\tau_{\mathrm{b}i}}{\omega_{\mathrm{s}} L_\sigma}, \tag{4.6}$$

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_3) = 0, \tag{4.7}$$

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_4) = -\frac{\frac{|v_{\mathrm{b}i}|}{2}\left(\pi - \tau_{\mathrm{b}i} + \phi_{\mathrm{b}i}\right)}{\omega_{\mathrm{s}} L_\sigma}, \tag{4.8}$$

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_5) = -\frac{\frac{|v_{\mathrm{b}i}|}{2}\left(\pi + \phi_{\mathrm{b}i}\right) - n v_{\mathrm{Bb}i}\tau_{\mathrm{b}i}}{\omega_{\mathrm{s}} L_\sigma}. \tag{4.9}$$

The power $p_{\mathrm{mb}i}$ transferred from the AC to the DC side over a switching cycle is calculated by evaluating the integral

$$p_{\mathrm{mb}i} = \frac{1}{2\pi}\int_0^{2\pi} v_{\mathrm{p},\mathrm{b}i}(\tau) i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau)\ \mathrm{d}\tau \tag{4.10}$$

which leads to the power flow equation dependent on the control variables $\tau_{\mathrm{b}i}$ and $\phi_{\mathrm{b}i}$

$$p_{\mathrm{mb}i} = \frac{|v_{\mathrm{b}i}|\, n v_{\mathrm{Bb}i}\tau_{\mathrm{b}i}\left(\pi - \tau_{\mathrm{b}i} + 2\phi_{\mathrm{b}i}\right)}{4\pi\omega_{\mathrm{s}} L_\sigma}. \tag{4.11}$$

From the ZCS condition $i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_0) = i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_3) = 0$ for the AC-side half-bridge (see **Fig. 4.5**), the control variable $\tau_{\mathrm{b}i}$ is calculated as

$$\tau_{\mathrm{b}i} = \frac{|v_{\mathrm{b}i}|\,\pi}{2 n v_{\mathrm{Bb}i}}. \tag{4.12}$$

With the power flow equation (4.11) set to a reference power $p^*_{\mathrm{mb}i}$ and inserting $\tau_{\mathrm{b}i}$ from (4.12), the phase shift $\phi_{\mathrm{b}i}$ is given as

$$\phi_{\mathrm{b}i} = \frac{16\omega_{\mathrm{s}} L_\sigma n v_{\mathrm{Bb}i} p^*_{\mathrm{mb}i} - 2\pi n v_{\mathrm{Bb}i}\,|v_{\mathrm{b}i}|^2 + \pi\,|v_{\mathrm{b}i}|^3}{4 n v_{\mathrm{Bb}i}\,|v_{\mathrm{b}i}|^2}. \tag{4.13}$$

In *low power mode* the power transfer $p_{\mathrm{mb}i}$ can be reduced down to zero. The upper limit of the power transfer occurs at the mode boundary where $\phi_{\mathrm{b}i} = 0$ and is calculated as

$$p_{\mathrm{mb}i,\max} = \frac{\pi\,|v_{\mathrm{b}i}|^2\left(2 n v_{\mathrm{Bb}i} - |v_{\mathrm{b}i}|\right)}{16 n v_{\mathrm{Bb}i}\omega_{\mathrm{s}} L_\sigma}. \tag{4.14}$$

Fig. 4.6 shows the evaluated equations (4.12) and (4.13) for the control variables $\tau_{\mathrm{b}i}$ and $\phi_{\mathrm{b}i}$ over a 50 Hz grid half-cycle for one module design example. Moreover, the maximum power $p_{\mathrm{mb}i,\max}$ that can be transferred over the transformer in *low power mode* is drawn as a dashed line. It can be seen that the reference power $p^*_{\mathrm{mb}i}$ in *low power mode* is located close to the maximum $p_{\mathrm{mb}i,\max}$ whereas in *high power mode* much more power could be transferred until the maximum is reached. This is due to the fact that the peak current $i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_1)$ is only dependent on the AC module voltage $|v_{\mathrm{b}i}|$ at the maximum power flow (see **Fig. 4.5**). In *high power mode* the peak current $i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_2)$ can be drastically increased by setting a corresponding phase shift $\phi_{\mathrm{b}i}$ to increase the power.

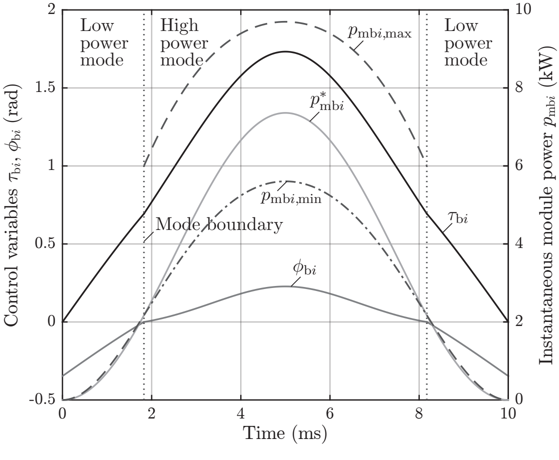


Figure 4.6: Control variables $\tau_{\mathrm{b}i}$, $\phi_{\mathrm{b}i}$ plotted over a 50 Hz grid half-cycle in *low power mode* as well as in *high power mode* for a module design example with the parameters $V_{\mathrm{b}i,\mathrm{rms}} = 230\,\mathrm{V}$, $V_{\mathrm{Bb}i} = 400\,\mathrm{V}$, $n = 1$, $L_\sigma = 35\,\mu\mathrm{H}$, $f_\mathrm{s} = 20\,\mathrm{kHz}$ and a reference grid current $I^*_{\mathrm{b,rms}} = 16\,\mathrm{A}$ neglecting the reactive power compensation of the filter capacitors C_ac (assuming $I_{\mathrm{Cb}i} = 0$). The dashed lines indicate the maximum power $p_{\mathrm{mb}i,\max}$ that can be transferred over the transformer at every time instant (for the specific AC module voltage) for the two modes. Moreover, the reference power $p^*_{\mathrm{mb}i}$ is given as well as the minimum power $p_{\mathrm{mb}i,\min}$ in *high power mode*.

High power mode

Similar to the *low power mode*, the AC-side referred transformer leakage inductance current $i_{\mathrm{L}\sigma,\mathrm{b}i}$ in *high power mode* over a switching cycle $T_\mathrm{s} = \frac{2\pi}{\omega_\mathrm{s}}$ with the angular frequency ω_s can be derived using piecewise linear equations as

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau) = \begin{cases} \dfrac{\frac{|v_{\mathrm{b}i}|}{2} + nv_{\mathrm{Bb}i}}{\omega_\mathrm{s} L_\sigma}(\tau - \tau_0) + i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_0) & \tau_0 \leq \tau \leq \tau_1 \\ \dfrac{\frac{|v_{\mathrm{b}i}|}{2}}{\omega_\mathrm{s} L_\sigma}(\tau - \tau_1) + i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_1) & \tau_1 \leq \tau \leq \tau_2 \\ \dfrac{\frac{|v_{\mathrm{b}i}|}{2} - nv_{\mathrm{Bb}i}}{\omega_\mathrm{s} L_\sigma}(\tau - \tau_2) + i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_2) & \tau_2 \leq \tau \leq \tau_3 \\ \dfrac{-\frac{|v_{\mathrm{b}i}|}{2} - nv_{\mathrm{Bb}i}}{\omega_\mathrm{s} L_\sigma}(\tau - \tau_3) + i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_3) & \tau_3 \leq \tau \leq \tau_4 \\ \dfrac{-\frac{|v_{\mathrm{b}i}|}{2}}{\omega_\mathrm{s} L_\sigma}(\tau - \tau_4) + i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_4) & \tau_4 \leq \tau \leq \tau_5 \\ \dfrac{-\frac{|v_{\mathrm{b}i}|}{2} + nv_{\mathrm{Bb}i}}{\omega_\mathrm{s} L_\sigma}(\tau - \tau_5) + i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_5) & \tau_5 \leq \tau \leq \tau_6 \end{cases} \tag{4.15}$$

with $\tau_0 = 0$, $\tau_6 = 2\pi$ and $|v_{\mathrm{b}i}|$ being the absolute value of the instantaneous AC module voltage and $v_{\mathrm{Bb}i}$ the battery voltage. The values of the transformer current at the switching instants are

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_0) = 0, \tag{4.16}$$

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_1) = \frac{\frac{|v_{\mathrm{b}i}|}{2}\phi_{\mathrm{b}i} + nv_{\mathrm{Bb}i}\phi_{\mathrm{b}i}}{\omega_\mathrm{s} L_\sigma}, \tag{4.17}$$

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_2) = \frac{\frac{|v_{\mathrm{b}i}|}{2}(\pi - \tau_{\mathrm{b}i} + \phi_{\mathrm{b}i}) + nv_{\mathrm{Bb}i}\phi_{\mathrm{b}i}}{\omega_\mathrm{s} L_\sigma}, \tag{4.18}$$

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_3) = 0, \tag{4.19}$$

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_4) = -\frac{\frac{|v_{\mathrm{b}i}|}{2}\phi_{\mathrm{b}i} + nv_{\mathrm{Bb}i}\phi_{\mathrm{b}i}}{\omega_\mathrm{s} L_\sigma}, \tag{4.20}$$

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_5) = -\frac{\frac{|v_{\mathrm{b}i}|}{2}(\pi - \tau_{\mathrm{b}i} + \phi_{\mathrm{b}i}) + nv_{\mathrm{Bb}i}\phi_{\mathrm{b}i}}{\omega_\mathrm{s} L_\sigma}. \tag{4.21}$$

The power $p_{\mathrm{mb}i}$ transferred from the AC to the DC side over a switching cycle is calculated with the integral (4.10) which leads to the power flow equation dependent on the control variables $\tau_{\mathrm{b}i}$ and $\phi_{\mathrm{b}i}$

$$p_{\mathrm{mb}i} = \frac{|v_{\mathrm{b}i}|\, n v_{\mathrm{Bb}i} \left(\tau_{\mathrm{b}i} \left(\pi - \tau_{\mathrm{b}i} + 2\phi_{\mathrm{b}i}\right) - 2\phi_{\mathrm{b}i}^2\right)}{4\pi\omega_{\mathrm{s}} L_\sigma}. \tag{4.22}$$

From the ZCS condition $i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_0) = i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_3) = 0$ for the AC-side half-bridge (see **Fig. 4.5**) the control variable $\tau_{\mathrm{b}i}$ is calculated as

$$\tau_{\mathrm{b}i} = \frac{|v_{\mathrm{b}i}|\,\pi + 4 n v_{\mathrm{Bb}i}\phi_{\mathrm{b}i}}{2 n v_{\mathrm{Bb}i}} \tag{4.23}$$

which shows a linear dependency on the phase shift $\phi_{\mathrm{b}i}$. With the power flow equation (4.22) set to a reference power $p_{\mathrm{mb}i}^*$ and inserting $\tau_{\mathrm{b}i}$ from (4.23), the phase shift $\phi_{\mathrm{b}i}$ is given as

$$\phi_{\mathrm{b}i} = \frac{2\pi n v_{\mathrm{Bb}i}\,|v_{\mathrm{b}i}| - \pi\,|v_{\mathrm{b}i}|^2 - \sqrt{\alpha}}{4 n v_{\mathrm{Bb}i}\,|v_{\mathrm{b}i}|} \tag{4.24}$$

where

$$\alpha = -32\pi\omega_{\mathrm{s}} L_\sigma n v_{\mathrm{Bb}i}\,|v_{\mathrm{b}i}|\, p_{\mathrm{mb}i}^* + 4\pi^2 n^2 v_{\mathrm{Bb}i}^2\,|v_{\mathrm{b}i}|^2 - \pi^2\,|v_{\mathrm{b}i}|^4. \tag{4.25}$$

In *high power mode* the minimum power transfer occurs at the mode boundary where $\phi_{\mathrm{b}i} = 0$ and is calculated as

$$p_{\mathrm{mb}i,\min} = \frac{\pi\,|v_{\mathrm{b}i}|^2 \left(2 n v_{\mathrm{Bb}i} - |v_{\mathrm{b}i}|\right)}{16 n v_{\mathrm{Bb}i}\omega_{\mathrm{s}} L_\sigma}. \tag{4.26}$$

The maximum power that can be transferred is obtained by setting the derivative of (4.22) with respect to $\phi_{\mathrm{b}i}$ to zero after inserting (4.23) for $\tau_{\mathrm{b}i}$. The resulting limit is given by

$$p_{\mathrm{mb}i,\max} = \frac{\pi\,|v_{\mathrm{b}i}| \left(4 n^2 v_{\mathrm{Bb}i}^2 - |v_{\mathrm{b}i}|^2\right)}{32 n v_{\mathrm{Bb}i}\omega_{\mathrm{s}} L_\sigma}. \tag{4.27}$$

Also for the *high power mode* **Fig. 4.6** depicts the evaluated equations (4.23) and (4.24) for the control variables $\tau_{\mathrm{b}i}$ and $\phi_{\mathrm{b}i}$. The maximum power $p_{\mathrm{mb}i,\max}$ that can be transferred over the transformer is shown by the dashed line, the minimum power $p_{\mathrm{mb}i,\min}$ in this mode by the dash-dot line.

ZCS/ZVS conditions

ZCS turn-on and turn-off of the grid-side switches are always maintained during the whole AC module voltage period in *low power mode* as well as in *high power mode* by the conditions

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_0) = 0, \tag{4.28}$$

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_3) = 0 \tag{4.29}$$

as presumed above. This is the case both for the low-frequency (switching at the zero-crossing of the AC module voltage) and the medium-frequency (with switching period $T_\mathrm{s} = \frac{2\pi}{\omega_\mathrm{s}}$) switched devices. At the low-frequency switching instants also ZVS is possible since the AC module voltage crosses zero. The application of ZCS is especially advantageous when IGBTs are used, so that the tail current at turn-off is substantially reduced as long as there is enough time for most of the minority carriers to be recombined [140].

ZVS turn-on in the *low power mode* is maintained as long as the conditions

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_1) > I_\mathrm{ZVS}, \tag{4.30}$$

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_2) < -I_\mathrm{ZVS} \tag{4.31}$$

are fulfilled for a minimum commutation current I_ZVS needed to simultaneously charge and discharge the output capacitances of the switches in a bridge-leg within the interlocking interval (resonant transition). At the switching instants $i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_4)$, $i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_5)$, ZVS is then inherently given by the symmetry of the transformer leakage inductance current shape. In *high power mode*, the ZVS conditions are stated as

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_1) > I_\mathrm{ZVS}, \tag{4.32}$$

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_2) > I_\mathrm{ZVS}. \tag{4.33}$$

The application of ZVS is especially beneficial when MOSFETs are used since these majority carrier devices offer a relatively fast turn-off at low losses and do not suffer from a tail current like IGBTs [140]. As soon as the MOSFET channel is completely blocked, a resonant transition of the drain-source voltage starts where the inductive load current charges the output capacitance of the turned-off MOSFET and simultaneously discharges the output capacitance of the to-be-turned-on MOSFET in the same bridge-leg until its antiparallel body diode starts to conduct. At this point the MOSFET can be turned on at (nearly) zero voltage.

The minimal turn-off current of a MOSFET required to achieve ZVS is in literature usually determined by current based, energy based or charge based ZVS conditions [103, 141]. Whereas the current based method only requires the drain-to-source current to be positive in the MOSFET initiating the commutation, the energy based approach ensures the energy stored in the leakage inductance of the transformer is sufficient enough to charge the energy equivalent linear capacitance of the parallel connection of two non-linear MOSFET output capacitances during the interlocking interval [142, 143]. Since the energy based conditions lead to a poor approximation of the leakage inductance current during the commutation interval, a charge based model is beneficial to use [103, 141].

Applying the model proposed in [141], the charge required to charge or discharge the output capacitance C_{oss} of a MOSFET in a DC-side bridge-leg is given by

$$Q_{\mathrm{C}} = q_{\mathrm{C}}(v_{\mathrm{Bb}i}) = \int_{0}^{v_{\mathrm{Bb}i}} C_{\mathrm{oss}}(v_{\mathrm{C}})\ \mathrm{d}v_{\mathrm{C}} \tag{4.34}$$

with $q_{\mathrm{C}}(v_{\mathrm{C}})$ being the charge function depending on the voltage v_{C} across the capacitance C_{oss} which is evaluated at the battery voltage $v_{\mathrm{Bb}i}$. To achieve ZVS, the transformer leakage inductance current $i_{\mathrm{L}\sigma,\mathrm{b}i}$ has to provide a total charge of $2Q_{\mathrm{C}}$. A simple capacitance model can be stated as

$$v_{\mathrm{C}}(q_{\mathrm{C}}) = \begin{cases} 0 & q_{\mathrm{C}} < Q_{\mathrm{C}} \\ \\ v_{\mathrm{Bb}i} & q_{\mathrm{C}} \geq Q_{\mathrm{C}} \end{cases} \tag{4.35}$$

by assuming a step voltage change of v_{C} across the parallel connection of two output capacitances $C_{\mathrm{oss}}||C_{\mathrm{oss}}$ at half of the required charge to complete the resonant transition. The charge requirement is formulated by the current integral

$$\int_{T_{\mathrm{c}}} |i_{\mathrm{L}\sigma,\mathrm{b}i}(t)|\ \mathrm{d}t \geq 2Q_{\mathrm{C}} \tag{4.36}$$

over the commutation interval T_{c}. By evaluating this integral for the specific commutation intervals following the switching instants τ_1, τ_2, the minimum commutation current I_{ZVS} can be determined. For obtaining simplified charge based ZVS conditions, the leakage inductance current $i_{\mathrm{L}\sigma,\mathrm{b}i}$ is considered to be constant during the commutation interval T_c what yields

$$I_\mathrm{ZVS} \geq \frac{2Q_\mathrm{C}}{T_\mathrm{c}}. \tag{4.37}$$

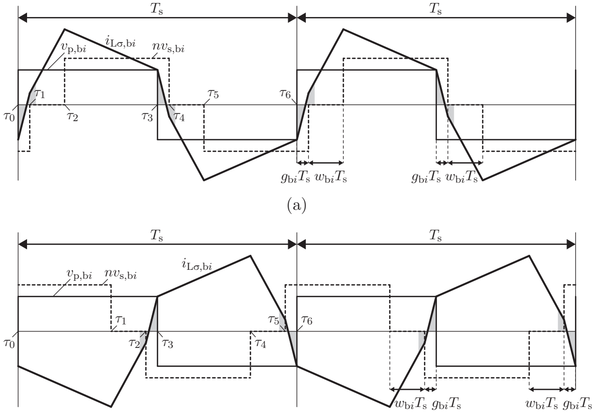
The minimum commutation current I_ZVS cannot be maintained around the zero-crossing of the phase shift $\phi_{\mathrm{b}i}$ where the mode change occurs as well as around the zero-crossing of the AC module voltage. In these regions, the commutation current is not sufficient to charge/discharge the output capacitances of the MOSFETs within the interlocking interval. Nevertheless, considering also the magnetizing current of the transformer, which has a positive contribution to the commutation current for the battery-side MOSFETs, ZVS can be achieved also around $\phi_{\mathrm{b}i} = 0$ except for a very small interval around it [144].

By using ZCS and/or ZVS, hard-switching in terms of a forced diode commutation by turning on a switching device while the antiparallel diode of the to-be-turned-off device in the same bridge-leg is conducting is avoided. Especially for silicon MOSFET devices, the reverse recovery losses caused by the body diode can be relatively high for devices with a blocking voltage capability higher than 500 V. Recent developments in the field of wide band gap semiconductor devices such as silicon carbide MOSFETs [145] or gallium nitride FETs [146] show a substantial reduction in the reverse recovery charge of the body diode, so that hard-switching operation at high switching frequencies gets possible.

4.3.2 ZVS modulation with variable switching frequency

The above presented ZCS/ZVS modulation guarantees ZCS over the whole AC module voltage but suffers from losing ZVS in the region of the mode change. Furthermore, the required mode change to lower the power transferred over the transformer around the zero-crossing of the AC module voltage (PFC operation assumed) induces transition constraints for the control variables, so that the two modes cannot be optimized independently.

To cope with these drawbacks, only the *lagging outer mode* and the *leading outer mode* for power direction reversal depicted in **Fig. 4.7(a)** and **Fig. 4.7(b)** are considered in the following. These modes allow AC- and DC-side ZVS at every switching instant as long as the minimum commutation current for the resonant transition is reached. Instead of changing the mode to lower the power transfer around the zero-crossing of the AC module voltage, the switching frequency is increased. The switching frequency is considered as an additional control variable which is restricted to a minimum and a maximum value. For the AC-DC DAB module, in total three degrees of freedom in control are available which are determined in an optimization procedure shown below to fulfill the ZVS conditions as well as the power transfer condition for a minimum transformer leakage inductance peak current.



(a)

(b)

Figure 4.7: Medium-frequency voltages $v_{\mathrm{p,b}i}, nv_{\mathrm{s,b}i}$ applied to the transformer windings of a module and the resulting leakage inductance current $i_{\mathrm{L}\sigma,\mathrm{b}i}$ in *lagging outer mode* for a power transfer from the grid to the battery (a) and *leading outer mode* for a power transfer from the battery to the grid (b) over a switching cycle $T_\mathrm{s} = \frac{1}{f_\mathrm{s}}$. The modulation scheme guarantees grid-side and battery-side ZVS, so that MOSFETs can be used both at the grid and the battery side.

For the following mathematical analysis, the control variables $g_{\mathrm{b}i} \in \left[0, \frac{1}{2}\right]$ and $w_{\mathrm{b}i} \in \left[0, \frac{1}{2}\right]$ are introduced which are normalized to the switching period T_s. The control variables represent the phase shift between the grid-side and the battery-side square-wave voltages as well as the width of the battery-side clamping interval (see **Fig. 4.7**). Due to the frequency variation, the description with normalized control variables to T_s is advantageous over the use of an angle-based analysis. The turns ratio of the transformer guarantees that $nv_{\mathrm{s,b}i} > v_{\mathrm{p,b}i}$ in every point of the AC module voltage $v_{\mathrm{b}i}$ (boost mode). Only the derivation of the modulation in grid-to-battery operation is given in the following. The derivation of the modulation in battery-to-grid operation can be done analogously.

Lagging outer mode

By using piecewise linear equations, the AC-side referred transformer leakage inductance current $i_{\mathrm{L}\sigma,\mathrm{b}i}$ in *lagging outer mode* over a switching cycle $T_\mathrm{s} = \frac{1}{f_\mathrm{s}}$ with the switching frequency f_s is given by

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau) = \begin{cases} \dfrac{\frac{|v_{\mathrm{b}i}|}{2} + nv_{\mathrm{Bb}i}}{L_\sigma}(\tau - \tau_0) + i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_0) & \tau_0 \leq \tau \leq \tau_1 \\ \dfrac{\frac{|v_{\mathrm{b}i}|}{2}}{L_\sigma}(\tau - \tau_1) + i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_1) & \tau_1 \leq \tau \leq \tau_2 \\ \dfrac{\frac{|v_{\mathrm{b}i}|}{2} - nv_{\mathrm{Bb}i}}{L_\sigma}(\tau - \tau_2) + i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_2) & \tau_2 \leq \tau \leq \tau_3 \\ \dfrac{-\frac{|v_{\mathrm{b}i}|}{2} - nv_{\mathrm{Bb}i}}{L_\sigma}(\tau - \tau_3) + i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_3) & \tau_3 \leq \tau \leq \tau_4 \\ \dfrac{-\frac{|v_{\mathrm{b}i}|}{2}}{L_\sigma}(\tau - \tau_4) + i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_4) & \tau_4 \leq \tau \leq \tau_5 \\ \dfrac{-\frac{|v_{\mathrm{b}i}|}{2} + nv_{\mathrm{Bb}i}}{L_\sigma}(\tau - \tau_5) + i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_5) & \tau_5 \leq \tau \leq \tau_6 \end{cases} \tag{4.38}$$

with $\tau_0 = 0$, $\tau_6 = T_\mathrm{s}$ and $|v_{\mathrm{b}i}|$ being the absolute value of the instantaneous AC module voltage and $v_{\mathrm{Bb}i}$ the battery voltage. The values of the transformer current at the switching instants are

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_0) = -\frac{\frac{|v_{\mathrm{b}i}|}{2} + nv_{\mathrm{Bb}i}\,(4g_{\mathrm{b}i} + 2w_{\mathrm{b}i} - 1)}{4f_\mathrm{s}L_\sigma}, \tag{4.39}$$

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_1) = \frac{\frac{|v_{\mathrm{b}i}|}{2}\,(4g_{\mathrm{b}i} - 1) - nv_{\mathrm{Bb}i}\,(2w_{\mathrm{b}i} - 1)}{4f_\mathrm{s}L_\sigma}, \tag{4.40}$$

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_2) = \frac{\frac{|v_{\mathrm{b}i}|}{2}\,(4g_{\mathrm{b}i} + 4w_{\mathrm{b}i} - 1) - nv_{\mathrm{Bb}i}\,(2w_{\mathrm{b}i} - 1)}{4f_\mathrm{s}L_\sigma}, \tag{4.41}$$

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_3) = \frac{\frac{|v_{\mathrm{b}i}|}{2} + nv_{\mathrm{Bb}i}\left(4g_{\mathrm{b}i} + 2w_{\mathrm{b}i} - 1\right)}{4f_{\mathrm{s}}L_{\sigma}}, \tag{4.42}$$

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_4) = -\frac{\frac{|v_{\mathrm{b}i}|}{2}\left(4g_{\mathrm{b}i} - 1\right) - nv_{\mathrm{Bb}i}\left(2w_{\mathrm{b}i} - 1\right)}{4f_{\mathrm{s}}L_{\sigma}}, \tag{4.43}$$

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_5) = -\frac{\frac{|v_{\mathrm{b}i}|}{2}\left(4g_{\mathrm{b}i} + 4w_{\mathrm{b}i} - 1\right) - nv_{\mathrm{Bb}i}\left(2w_{\mathrm{b}i} - 1\right)}{4f_{\mathrm{s}}L_{\sigma}}. \tag{4.44}$$

The power $p_{\mathrm{mb}i}$ transferred from the AC to the DC side over a switching cycle is calculated with the integral (4.10) which leads to the power flow equation depending on the control variables $g_{\mathrm{b}i}$, $w_{\mathrm{b}i}$ (and f_{s})

$$p_{\mathrm{mb}i} = \frac{|v_{\mathrm{b}i}|\, nv_{\mathrm{Bb}i}\left(2g_{\mathrm{b}i} - 4g_{\mathrm{b}i}^2 + w_{\mathrm{b}i} - 2w_{\mathrm{b}i}^2 - 4g_{\mathrm{b}i}w_{\mathrm{b}i}\right)}{4f_{\mathrm{s}}L_{\sigma}}. \tag{4.45}$$

In *lagging outer mode*, the power transfer $p_{\mathrm{mb}i}$ can be reduced down to zero. The upper limit of the power transfer is obtained by setting the derivatives of $p_{\mathrm{mb}i}$ with respect to $g_{\mathrm{b}i}$ and $w_{\mathrm{b}i}$ to zero what results in

$$p_{\mathrm{mb}i,\max} = \frac{|v_{\mathrm{b}i}|\, nv_{\mathrm{Bb}i}}{16f_{\mathrm{s}}L_{\sigma}} \tag{4.46}$$

at the control variables $g_{\mathrm{b}i} = \frac{1}{4}$ and $w_{\mathrm{b}i} = 0$.

ZVS conditions

For maintaining ZVS turn-on in the *lagging outer mode*, the conditions

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_0) < -I_{\mathrm{ZVS}}, \tag{4.47}$$

$$i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_1) > I_{\mathrm{ZVS}} \tag{4.48}$$

have to be fulfilled for a minimum commutation current I_{ZVS} needed to simultaneously charge and discharge the output capacitances of the switches in a bridge-leg within the interlocking interval (resonant transition). At the time instant τ_2, ZVS is inherently given as long as the condition at τ_1 is met, since $i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_2) \geq i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_1)$. At the switching instants $i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_3)$, $i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_4)$, $i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_5)$, ZVS is then inherently given by the symmetry of the transformer leakage inductance current shape. The minimal turn-off current I_{ZVS} can be obtained from the charge based model described above in Section 4.3.1 for the applied MOSFETs in a module design.

Optimal control variables

For determining the control variables in the *lagging outer mode* under ZVS conditions, a numerical optimization is performed with the corresponding flow chart shown in **Fig. 4.8**. The solutions of the control variables are given numerically which can be stored in a lookup table (LUT). No closed-form analytical solutions are derived.

The objective of the optimization is to minimize the absolute value of the transformer leakage inductance current $|i_{\mathrm{L}\sigma,\mathrm{b}i}|$ at the time instants τ_0 and τ_1 for a minimal commutation current while maintaining the ZVS conditions and simultaneously guarantee the corresponding power flow over a switching cycle which leads to a sinusoidal AC module current. In this way, the reactive power (shaded areas in **Fig. 4.7**), that is required for ZVS, is kept minimal what in turn leads to minimal transformer leakage inductance peak currents.

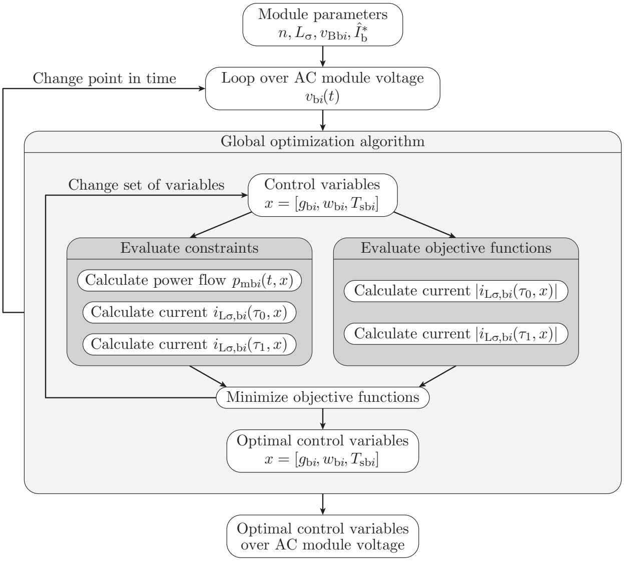

Module parameters
$n, L_\sigma, v_{\mathrm{Bb}i}, \hat{I}_\mathrm{b}^*$
Change point in time
Loop over AC module voltage
$v_{\mathrm{b}i}(t)$
Global optimization algorithm
Change set of variables
Control variables
$x = [g_{\mathrm{b}i}, w_{\mathrm{b}i}, T_{\mathrm{sb}i}]$
Evaluate constraints
Calculate power flow $p_{\mathrm{mb}i}(t, x)$
Calculate current $i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_0, x)$
Calculate current $i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_1, x)$
Evaluate objective functions
Calculate current $|i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_0, x)|$
Calculate current $|i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_1, x)|$
Minimize objective functions
Optimal control variables
$x = [g_{\mathrm{b}i}, w_{\mathrm{b}i}, T_{\mathrm{sb}i}]$
Optimal control variables
over AC module voltage

Figure 4.8: Flow chart of the optimization algorithm to derive optimal control variables $g_{\mathrm{b}i}$, $w_{\mathrm{b}i}$, $T_{\mathrm{sb}i}$ for ZVS conditions for a given set of module parameters $n, L_\sigma, v_{\mathrm{Bb}i}$ and a reference current amplitude $\hat{I}_\mathrm{b}^*$. The optimization is carried out in every point $v_{\mathrm{b}i}(t)$ of the AC module voltage applying a corresponding discretization.

The minimization of the leakage inductance peak current in every switching cycle leads to the maximum module efficiency as shown in **Fig. 4.9** for different parameterizations with the switching frequency $f_{\mathrm{sb}i}$ and the module power $p_{\mathrm{mb}i}$. There, the efficiencies at the peak AC module voltage $v_{\mathrm{b}i} = 325\,\mathrm{V}$ and the DC voltage $v_{\mathrm{Bb}i} = 350\,\mathrm{V}$ of a module prototype system described below in Section 4.5 are evaluated by iterating over the phase shift $g_{\mathrm{b}i} \in \left[0, \frac{1}{2}\right]$ for a constant switching frequency $f_{\mathrm{sb}i}$ and a given power operating point $p_{\mathrm{mb}i}$. With an increasing phase shift $g_{\mathrm{b}i}$, the clamping interval $w_{\mathrm{b}i}$ is decreased to keep the module power $p_{\mathrm{mb}i}$ constant. As the phase shift increases, also the leakage inductance peak current $i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_2)$ (see **Fig. 4.7(a)**) increases and the module efficiency drops. The starting point of the phase shift, where the efficiency exhibits its maximum, guarantees that $i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_0) < 0$ as well as $i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_1) > 0$.

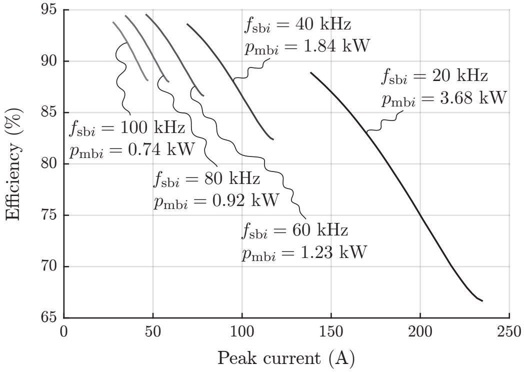


Figure 4.9: Module efficiencies for a module prototype system described in Section 4.5 depending on the transformer leakage inductance peak current $i_{\mathrm{L}\sigma,\mathrm{b}i}(\tau_2)$ for different parameterizations with the switching frequency $f_{\mathrm{sb}i}$ and the module power $p_{\mathrm{mb}i}$. The efficiencies are given at the peak AC module voltage $v_{\mathrm{b}i} = 325\,\mathrm{V}$ and the DC voltage $v_{\mathrm{Bb}i} = 350\,\mathrm{V}$ at a given power operating point $p_{\mathrm{mb}i}$.

For the ZVS modulation with variable switching frequency, there are three degrees of freedom in the modulation scheme. These are the phase shift $g_{\mathrm{b}i}$, the length of the clamping interval $w_{\mathrm{b}i}$ and the switching period $T_{\mathrm{sb}i}$. At each point of the AC module voltage, the optimization problem is formulated as

$$\min_{x} \left(\left| i_{\mathrm{L}\sigma}(\tau_0, x) \right|, \left| i_{\mathrm{L}\sigma}(\tau_1, x) \right| \right) \tag{4.49}$$

with respect to

$$x = \begin{bmatrix} g_{\mathrm{b}i} \\ w_{\mathrm{b}i} \\ T_{\mathrm{sb}i} \end{bmatrix} \text{ with } x_{\mathrm{lb}} = \begin{bmatrix} 0 \\ 0 \\ T_{\mathrm{sb}i,\mathrm{min}} \end{bmatrix},\ x_{\mathrm{ub}} = \begin{bmatrix} \frac{1}{2} \\ \frac{1}{2} - g_{\mathrm{b}i} \\ T_{\mathrm{sb}i,\mathrm{max}} \end{bmatrix} \tag{4.50}$$

where x denotes the vector of control variables which is restricted to lower and upper bounds x_{lb}, x_{ub} respectively. The first constraint is given by the power equality constraint

$$p_{\mathrm{mb}i}(t, x) = p^*_{\mathrm{mb}i}(t) \tag{4.51}$$

with the reference of the instantaneous power $p^*_{\mathrm{mb}i}(t)$ for a given input current amplitude $\hat{I}^*_{\mathrm{b}}$

$$p^*_{\mathrm{mb}i}(t) = \hat{V}_{\mathrm{b}i} \hat{I}^*_{\mathrm{b}} \sin^2(\omega t) \tag{4.52}$$

for the simplified case and

$$p^*_{\mathrm{mb}i}(t) = \hat{V}_{\mathrm{b}i} \hat{I}^*_{\mathrm{b}} \sin^2(\omega t) - \frac{\omega C_{\mathrm{ac}}}{2} \hat{V}^2_{\mathrm{b}i} \sin(\omega t) \cos(\omega t) \tag{4.53}$$

for considering also the compensation of the reactive power of the input capacitors C_{ac}. Further constraints are given by the minimum commutation current I_{ZVS} for ZVS as

$$\left| i_{\mathrm{L}\sigma}(\tau_0, x) \right| \geq I_{\mathrm{ZVS}}, \tag{4.54}$$

$$\left| i_{\mathrm{L}\sigma}(\tau_1, x) \right| \geq I_{\mathrm{ZVS}}. \tag{4.55}$$

Fig. 4.10 shows the obtained control variables $g_{\mathrm{b}i}$, $w_{\mathrm{b}i}$ and $f_{\mathrm{sb}i} = \frac{1}{T_{\mathrm{sb}i}}$ over a 50 Hz grid half-cycle for one module design example. Around the zero-crossing of the AC module voltage, the switching frequency $f_{\mathrm{sb}i}$ is increased to lower the output power and reaches its maximum which is set to 120 kHz. Similar, the phase shift $g_{\mathrm{b}i}$ is increased with lower output power which guarantees a triangular-like transformer leakage inductance current that is required to maintain ZVS also around the zero-crossing of the AC module voltage. For a high power transfer at

2 ms up to 8 ms (see **Fig. 4.10**), $w_{\mathrm{b}i}$ stays rather constant and the power is controlled mainly by the phase shift $g_{\mathrm{b}i}$ and the switching frequency $f_{\mathrm{sb}i}$.

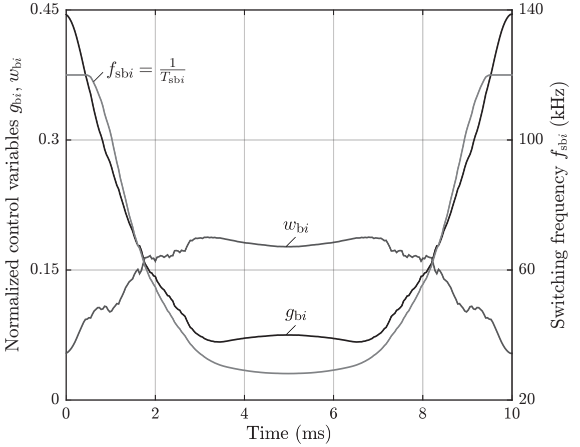


Figure 4.10: Control variables $g_{\mathrm{b}i}$, $w_{\mathrm{b}i}$, $f_{\mathrm{sb}i} = \frac{1}{T_{\mathrm{sb}i}}$ obtained by the optimization process depicted in **Fig. 4.8** plotted over a 50 Hz grid half-cycle in *lagging outer mode* for a module design example with the parameters $V_{\mathrm{b}i,\mathrm{rms}} = 230\,\mathrm{V}$, $V_{\mathrm{Bb}i} = 350\,\mathrm{V}$, $n = 10/13$, $L_\sigma = 20\,\mu\mathrm{H}$, $f_{\mathrm{sb}i,\mathrm{min}} = 20\,\mathrm{kHz}$, $f_{\mathrm{sb}i,\mathrm{max}} = 120\,\mathrm{kHz}$ and a reference grid current $I^*_{\mathrm{b,rms}} = 16\,\mathrm{A}$ neglecting the reactive power compensation of the filter capacitors C_{ac} (assuming $I_{\mathrm{Cb}i} = 0$).

4.4 Converter control

The control of the cascaded AC-DC DAB converter with an integrated battery energy storage system is divided into a top-level and a module-level control as shown in **Fig. 4.11**. The objectives of the top-level control are obtaining the grid and phase angles by means of phase-locked loops (PLLs), controlling the grid current in the dq-frame and balancing the average state of charge (SOC) values of the storage batteries over the three phases. On the module level, the SOCs of the batteries in one phase are balanced and the grid-side module voltages are controlled.

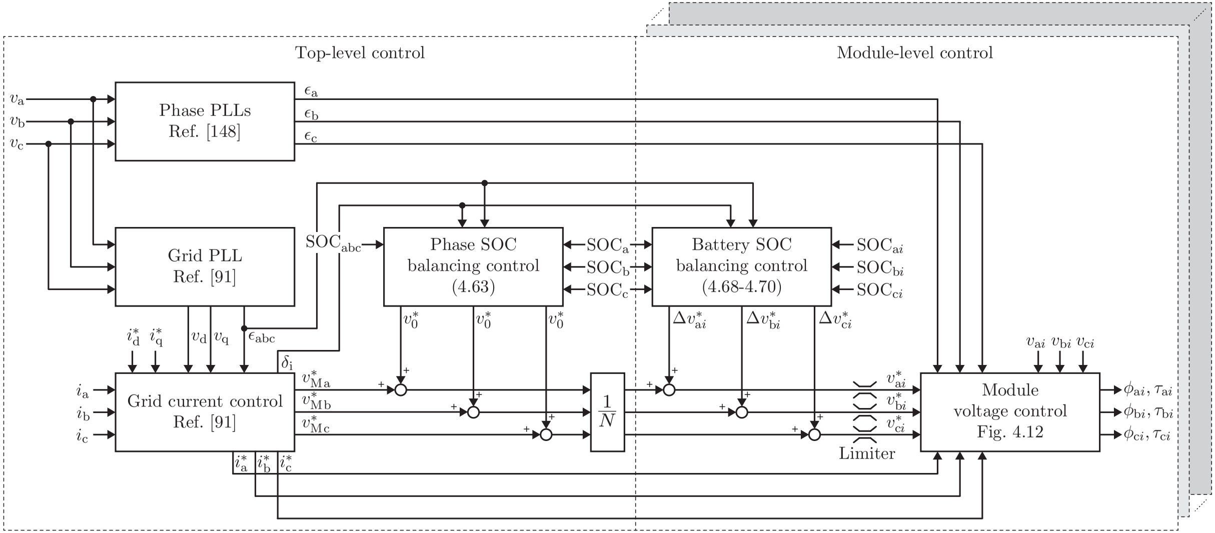

Top-level control
Module-level control
v_a
v_b
v_c
Phase PLLs
Ref. [148]
ϵ_a
ϵ_b
ϵ_c
Grid PLL
Ref. [91]
$\mathrm{SOC}_\mathrm{abc}$
Phase SOC
balancing control
(4.63)
SOC_a
SOC_b
SOC_c
Battery SOC
balancing control
(4.68-4.70)
$\mathrm{SOC}_{\mathrm{a}i}$
$\mathrm{SOC}_{\mathrm{b}i}$
$\mathrm{SOC}_{\mathrm{c}i}$
i^*_d i^*_q
v_d v_q
ϵ_abc
δ_i
v^*_0
v^*_0
v^*_0
$\Delta v^*_{\mathrm{a}i}$
$\Delta v^*_{\mathrm{b}i}$
$\Delta v^*_{\mathrm{c}i}$
$v_{\mathrm{a}i}$ $v_{\mathrm{b}i}$ $v_{\mathrm{c}i}$
i_a
i_b
i_c
Grid current control
Ref. [91]
v^*_Ma
v^*_Mb
v^*_Mc
+
$\frac{1}{N}$
$v^*_{\mathrm{a}i}$
$v^*_{\mathrm{b}i}$
$v^*_{\mathrm{c}i}$
Limiter
Module
voltage control
Fig. 4.12
$\phi_{\mathrm{a}i}, \tau_{\mathrm{a}i}$
$\phi_{\mathrm{b}i}, \tau_{\mathrm{b}i}$
$\phi_{\mathrm{c}i}, \tau_{\mathrm{c}i}$
i^*_a i^*_b i^*_c

Figure 4.11: Overview of the control system of the cascaded AC-DC DAB converter with an integrated battery energy storage system depicted in **Fig. 4.1**.

For the modulation scheme with fixed switching frequency, the modules in the same phase are interleaved at the grid side by shifting their phase shift references by multiples of $\frac{2\pi}{N}$ in order to reduce the ripple of the grid current and to keep the grid filter inductance values L_{ac} low.

4.4.1 Grid and phase PLLs

For the grid current control in the dq-frame, the grid PLL in **Fig. 4.11** obtains the grid angle ϵ_{abc} of the three-phase grid. Moreover, for the module-level voltage control in dq-coordinates, the angles ϵ_{a}, ϵ_{b}, ϵ_{c} of the phase voltages are required which are obtained by the phase PLLs (see **Fig. 4.11**). A separate grid PLL is implemented because during unbalanced grid voltage conditions the angle ϵ_{abc} differs from ϵ_{a}. Furthermore, deriving ϵ_{abc} from the phase angles ϵ_{a}, ϵ_{b}, ϵ_{c} would require the measurement of the peak phase voltages at a reasonable sampling rate.

For a single-phase PLL, only the α-component is available, the β-component has to be constructed. This is done by using an orthogonal system generator (OSG) implemented with a second order generalized integrator (SOGI) structure as proposed in [147, 148]. The OSG-SOGI structure filters the measured input voltage and delivers two clean orthogonal voltage waveforms [148].

4.4.2 Grid current control

The grid current control in dq-coordinates depicted in **Fig. 4.11** takes the grid currents i_{d}^{*}, i_{q}^{*} as reference values and outputs the reference voltages in the time domain v_{Ma}^{*}, v_{Mb}^{*}, v_{Mc}^{*} of all series-connected modules in a phase leg [91]. These reference values are adjusted by the phase SOC balancing control as described below, then divided by the number of modules N in a phase and passed to the module-level control of each module. The current controllers for d- and q-axis have both a proportional and integral part.

4.4.3 Phase SOC balancing

The objective of the phase SOC balancing control as part of the top-level control is to equalize the average SOC values among the phase legs by means of zero-sequence voltage injection as described in [51]. By adding the zero-sequence voltage v_{0}^{*} to the phase reference voltages

v_{Ma}^*, v_{Mb}^*, v_{Mc}^* as shown in **Fig. 4.11**, an unequal active power can be drawn in each phase without drawing negative-sequence current at the grid side.

The average SOC values in the three phases are given by

$$\mathrm{SOC_a} = \frac{1}{N}\sum_{i=1}^{N}\mathrm{SOC}_{\mathrm{a}i}, \tag{4.56}$$

$$\mathrm{SOC_b} = \frac{1}{N}\sum_{i=1}^{N}\mathrm{SOC}_{\mathrm{b}i}, \tag{4.57}$$

$$\mathrm{SOC_c} = \frac{1}{N}\sum_{i=1}^{N}\mathrm{SOC}_{\mathrm{c}i} \tag{4.58}$$

whereas the reference SOC in a phase leg is the average value of the SOCs of all batteries in the system calculated as

$$\mathrm{SOC_{abc}} = \frac{1}{3}\left(\mathrm{SOC_a} + \mathrm{SOC_b} + \mathrm{SOC_c}\right). \tag{4.59}$$

The deviations from the reference values in each phase can then be written as

$$\Delta\mathrm{SOC_a} = \mathrm{SOC_{abc}} - \mathrm{SOC_a}, \tag{4.60}$$

$$\Delta\mathrm{SOC_b} = \mathrm{SOC_{abc}} - \mathrm{SOC_b}, \tag{4.61}$$

$$\Delta\mathrm{SOC_c} = \mathrm{SOC_{abc}} - \mathrm{SOC_c} \tag{4.62}$$

which are transformed to αβ-coordinates to form a deviation vector $\Delta\mathrm{SOC_{v0}} \cdot e^{j\delta_{\mathrm{v0}}}$. For compensating the phase SOC deviations, the zero-sequence voltage according to

$$v_0^* = K_0 \cdot \Delta\mathrm{SOC_{v0}} \cdot \cos(\epsilon_{\mathrm{abc}} + \delta_{\mathrm{i}} - \delta_{\mathrm{v0}}) \tag{4.63}$$

with

$$\delta_{\mathrm{i}} = \arctan\left(\frac{i_{\mathrm{q}}}{i_{\mathrm{d}}}\right) \tag{4.64}$$

is added to the phase reference voltages as depicted in **Fig. 4.11**, where K_0 defines a proportional gain, ϵ_{abc} corresponds to the grid voltage angle obtained by the grid PLL and δ_{i} represents the angle of the grid current space vector. The overall three-phase power transfer is not affected by the zero-sequence voltage injection since the sum of the three phase currents i_{a}, i_{b}, i_{c} is zero due to the open star point.

4.4.4 Battery SOC balancing

The battery SOC balancing control acts as a part of the module-level control to ensure balancing the SOCs among the batteries in the same phase leg. For the cascaded AC-DC DAB converter, this is done by adjusting the module voltage references (see **Fig. 4.11**) to draw the specific amount of active power in each module needed to balance the SOCs.

With the measured battery $\mathrm{SOC}_{\mathrm{a}i}$, $\mathrm{SOC}_{\mathrm{b}i}$, $\mathrm{SOC}_{\mathrm{c}i}$, the deviation of the SOC of a battery i from the average phase SOC value is calculated. The deviations for phases a, b, c are given by

$$\Delta\mathrm{SOC}_{\mathrm{a}i} = \mathrm{SOC}_{\mathrm{a}} - \mathrm{SOC}_{\mathrm{a}i}, \tag{4.65}$$

$$\Delta\mathrm{SOC}_{\mathrm{b}i} = \mathrm{SOC}_{\mathrm{b}} - \mathrm{SOC}_{\mathrm{b}i}, \tag{4.66}$$

$$\Delta\mathrm{SOC}_{\mathrm{c}i} = \mathrm{SOC}_{\mathrm{c}} - \mathrm{SOC}_{\mathrm{c}i}. \tag{4.67}$$

To equalize the SOCs among the batteries in one phase, the control adds the voltages $\Delta v_{\mathrm{a}i}^{*}$, $\Delta v_{\mathrm{b}i}^{*}$, $\Delta v_{\mathrm{c}i}^{*}$ according to the control laws

$$\Delta v_{\mathrm{a}i}^{*} = K_1 \cdot \Delta\mathrm{SOC}_{\mathrm{a}i} \cdot \cos\left(\epsilon_{\mathrm{abc}} + \delta_{\mathrm{i}}\right), \tag{4.68}$$

$$\Delta v_{\mathrm{b}i}^{*} = K_1 \cdot \Delta\mathrm{SOC}_{\mathrm{b}i} \cdot \cos\left(\epsilon_{\mathrm{abc}} - \frac{2\pi}{3} + \delta_{\mathrm{i}}\right), \tag{4.69}$$

$$\Delta v_{\mathrm{c}i}^{*} = K_1 \cdot \Delta\mathrm{SOC}_{\mathrm{c}i} \cdot \cos\left(\epsilon_{\mathrm{abc}} - \frac{4\pi}{3} + \delta_{\mathrm{i}}\right) \tag{4.70}$$

as depicted in **Fig. 4.11**, where δ_{i} corresponds to the angle of the grid current space vector. For positive $\Delta\mathrm{SOC}_{\mathrm{a}i}$, $\Delta\mathrm{SOC}_{\mathrm{b}i}$, $\Delta\mathrm{SOC}_{\mathrm{c}i}$, the power flowing into the batteries has to be increased which is done by increasing the grid-side module voltages. Accordingly, negative SOC deviations lead to a decrease of the module voltages. The upper limit of the grid-side module voltage is defined by the blocking voltage rating of the applied switching devices considering common safety margins. The limiters are shown in **Fig. 4.11** which output the reference voltages $v_{\mathrm{a}i}^{*}$, $v_{\mathrm{b}i}^{*}$, $v_{\mathrm{c}i}^{*}$ for the module-level voltage controllers.

4.4.5 Module voltage control

In order to enable balancing the SOCs of the batteries, the power distribution among the modules has to be varied. This can be done only by controlling the grid-side voltages of the series-connected modules in a phase leg while maintaining the sum of all module voltages equal to the reference voltage of the grid current control. This approach is similar to the conventional CHB converter where the balancing control of the DC-side capacitors or batteries is based on varying the amplitudes of the PWM generated sinusoidal voltages of an H-bridge module [51, 91, 93, 96]. Nevertheless, in the cascaded AC-DC DAB converter, the module voltage cannot directly be controlled, rather it is controlled indirectly via the power flow over the module transformer.

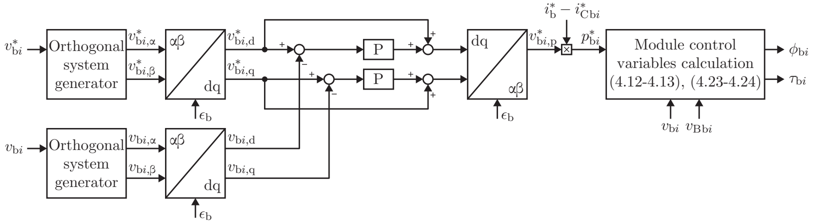

$v^*_{\mathrm{b}i}$
Orthogonal system generator
$v^*_{\mathrm{b}i,\alpha}$
$v^*_{\mathrm{b}i,\beta}$
αβ
dq
ϵ_b
$v^*_{\mathrm{b}i,\mathrm{d}}$
$v^*_{\mathrm{b}i,\mathrm{q}}$
+
−
P
P
+
+
dq
αβ
ϵ_b
$i^*_\mathrm{b} - i^*_{\mathrm{C}\mathrm{b}i}$
$v^*_{\mathrm{b}i,\mathrm{p}}$
$p^*_{\mathrm{b}i}$
Module control variables calculation (4.12-4.13), (4.23-4.24)
$\phi_{\mathrm{b}i}$
$\tau_{\mathrm{b}i}$
$v_{\mathrm{b}i}$
$v_{\mathrm{B}\mathrm{b}i}$
$v_{\mathrm{b}i}$
Orthogonal system generator
$v_{\mathrm{b}i,\alpha}$
$v_{\mathrm{b}i,\beta}$
αβ
dq
ϵ_b
$v_{\mathrm{b}i,\mathrm{d}}$
$v_{\mathrm{b}i,\mathrm{q}}$

Figure 4.12: Overview of the module voltage control at the grid side in the dq-frame, exemplarily shown for a module i in phase b applying the ZCS/ZVS modulation with fixed switching frequency described in Section 4.3.1. In case of the ZVS modulation with variable switching frequency, the module control variables calculation is replaced by a LUT to store the control variables obtained by the numerical optimization (see Section 4.3.2).

The voltage control is performed in the dq-frame of the respective phase as exemplarily shown in **Fig. 4.12** for phase b and the ZCS/ZVS modulation with fixed switching frequency described in Section 4.3.1. The transformation angles ϵ_a, ϵ_b, ϵ_c are obtained from the corresponding phase PLLs. The calculation of the αβ-components of the measured module voltage $v_{\mathrm{b}i}$ and the reference $v^*_{\mathrm{b}i}$ is done by using the same OSG-SOGI structure [148] as for the single-phase PLLs described above.

Two proportional controllers with feed-forward of the voltage reference values $v^*_{\mathrm{b}i,\mathrm{d}}$, $v^*_{\mathrm{b}i,\mathrm{q}}$ are used to generate a voltage reference signal $v^*_{\mathrm{b}i,\mathrm{p}}$ in the time domain which is multiplied by the phase current reference i^*_b to get the desired module transfer power $p^*_{\mathrm{b}i}$ (assuming $i^*_{\mathrm{Cb}i} = 0$).

For the ZCS/ZVS modulation with fixed switching frequency, the control variables $\phi_{\mathrm{b}i}$, $\tau_{\mathrm{b}i}$ can be calculated using (4.12), (4.13), (4.23) and (4.24) taking also the measured battery voltage $v_{\mathrm{Bb}i}$ into account. In the case of the ZVS modulation with variable switching frequency presented in Section 4.3.2, the control variables $g_{\mathrm{b}i}$, $w_{\mathrm{b}i}$, $T_{\mathrm{sb}i}$ are obtained by the numerical optimization shown in **Fig. 4.8** and stored in a LUT.

4.5 Module design

For validating the ZVS modulation with variable switching frequency presented in Section 4.3.2, a 3.3 kW AC-DC DAB module to connect to a 230 V AC voltage and a DC-side storage battery pack with a voltage range of 280 V up to 420 V is designed and built. The converter system is not only a module in the cascaded AC-DC converter, in fact it can be also used as a stand-alone single-phase bidirectional isolated AC-DC converter with PFC for instance for electric vehicle battery chargers for lithium-ion batteries. The parameters of the module prototype system

Table 4.3: Parameters of the AC-DC DAB module prototype system.

Mains voltage	$V_{\mathrm{b}i}$	230 V
Mains frequency	$f_\mathrm{g} = 1/T_\mathrm{g}$	50 Hz
Battery voltage	$V_{\mathrm{Bb}i}$	280 V...420 V
Nominal output power	$P_{\mathrm{mb}i}$	3.3 kW
Switching frequency	$f_{\mathrm{sb}i}$	20 kHz...120 kHz
Transformer turns ratio	n	10/13
Transformer leakage inductance	L_σ	20 µH
Transformer magnetizing inductance	L_m	11 mH
Inductors	L_ac, L_dc	100 µH
Capacitors	C_ac	10 µF
Capacitor	C_dc	20 µF

are given in **Tab. 4.3** and are thoroughly discussed based on the selected components and the applied loss models in the following.

4.5.1 Power components

In order to evaluate the AC-DC DAB module efficiencies at different operating points, the module components with their applied loss models are discussed. **Tab. 4.4** summarizes the components of the module prototype system.

Power MOSFETs

Since the applied modulation scheme guarantees ZVS at every switching instant, MOSFET devices with a comparable low on-state resistance are chosen. The used device is a 650 V MOSFET with an on-state resistance of 14 mΩ at 25 °C from STMicroelectronics [149]. The hardware prototype applies two MOSFETs in parallel for all switches.

The MOSFET loss model is based on data sheet parameters and described in Section B.1.2. The gate drive losses are modeled according to Section B.1.3.

Transformer

For the ZVS modulation with variable switching frequency, the transformer turns ratio has to guarantee

$$n v_{\mathrm{B b} i} > \frac{\hat{V}_{\mathrm{b} i}}{2} \tag{4.71}$$

at the lowest battery voltage of 280 V with the battery voltage $v'_{\mathrm{Bb}i} = n v_{\mathrm{Bb}i}$ referred to the AC side of the transformer.

Furthermore, the leakage inductance L_σ is designed such that the peak of the instantaneous power $\hat{P}_{\mathrm{mb}i} = \hat{V}_{\mathrm{b}i} \hat{I}^*_{\mathrm{b}}$ (neglecting the reactive power term in (4.53)) at full input power of 3.68 kW can be transferred at the lowest switching frequency of $f_{\mathrm{sb}i,\mathrm{min}} = 20\,\mathrm{kHz}$ and the lowest battery voltage of $v_{\mathrm{Bb}i,\mathrm{min}} = 280\,\mathrm{V}$. Using (4.46) and solving for L_σ leads to the design equation

$$L_\sigma = \frac{\hat{V}_{\mathrm{b}i} n v_{\mathrm{Bb}i,\mathrm{min}}}{16 f_{\mathrm{sb}i,\mathrm{min}} \hat{P}_{\mathrm{mb}i}}. \tag{4.72}$$

Table 4.4: Components of the AC-DC DAB module prototype system.

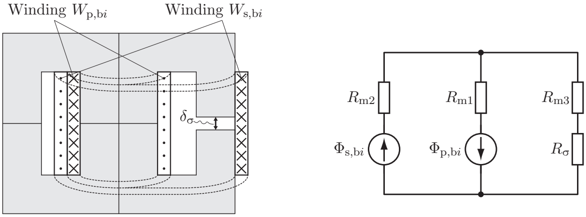
MOSFETs $S_{1a}, S_{1b}, S_{2a}, S_{2b}$	2x STY139N65M5, 650 V, 14 mΩ
MOSFETs S_3, S_4, S_5, S_6	2x STY139N65M5, 650 V, 14 mΩ
Transformer	2x 2x AMCC-4 VITROPERM 500F 10 primary turns, 120 µm copper foil 13 secondary turns, 120 µm copper foil
Inductors L_{ac}, L_{dc}	2x Kool Mu E 4317 26u, 27 turns Litz wire, 20 strands, 0.355 mm
Capacitors C_{ac}	18x Syfer 1825J500564KX, 560 nF
Capacitor C_{dc}	36x Syfer 1825J500564KX, 560 nF

The transformer is built of two AMCC-4 C-cores [150] made of nanocrystalline VITROPERM 500F [151] material forming an E-core. To increase the core area, two of them are stacked. The AC-side winding is wound around the center leg and the DC-side winding around the center and an outer stray leg as shown in **Fig. 4.13(a)** [152]. In **Fig. 4.13(b)**, also the reluctance model of the transformer is given. An air gap of length δ_σ is inserted in the stray leg to adjust the desired leakage inductance which is approximately given by

$$L_\sigma = \frac{N_\mathrm{p}^2}{R_\sigma} = \frac{N_\mathrm{p}^2 \mu_0 \mu_\mathrm{r} A_\mathrm{e}}{\delta_\sigma} \tag{4.73}$$

assuming that the air gap contributes to the main part of the stored energy of the stray magnetic field and that the fringing field is negligible small for a small δ_σ. A practical realization of the transformer ideally uses a distributed air gap to keep the fringing field low [152]. N_p is the AC-side number of turns and A_e denotes the core cross section area. The reluctance R_{m3} in the stray leg (also contributing to the leakage inductance, see **Fig. 4.13(b)**) can be neglected as with a relative permeability of around $\mu_\mathrm{r} = 20\,000$ of the VITROPERM 500F material [151] it is several orders of magnitude smaller than the leakage reluctance R_σ. In the loss model, the core losses are calculated by applying the improved generalized Steinmetz equation (iGSE) as described in Section B.2.2.

For the AC- and DC-side windings, copper foil is used where the optimal foil thickness is calculated according to [153] which gives a minimum value of effective AC resistance. These values are 132 µm and 116 µm. For the hardware prototype, 120 µm copper foil is chosen with 10 primary and 13 secondary turns. The skin and proximity effect losses in the foil conductors for each current harmonic are calculated with the loss models given in Section B.2.1 considering a 1D magnetic field approximation.



(a) (b)

Figure 4.13: 2D drawing of the transformer consisting of four C-cores with the AC-side winding $W_{\mathrm{p,b}i}$ wound around the inner leg and the DC-side winding $W_{\mathrm{s,b}i}$ wound around the inner and the right-hand sided stray leg (a). By inserting an air gap of length δ_σ in the stray leg, the leakage inductance L_σ is adjusted. In (b) the reluctance model is depicted with the flux sources $\Phi_{\mathrm{p,b}i}$ and $\Phi_{\mathrm{s,b}i}$.

Inductors

For the AC- and DC-side inductors L_{ac}, L_{dc}, two stacked E-cores of type Kool Mu 4317 with material 26u from Magnetics [154] are used with the winding placed around the center leg. Powder cores are ideally suited for the hardware prototype because they offer a distributed air gap and a high saturation flux density. This is advantageous over a ferrite core with a large air gap exhibiting considerable fringing magnetic field. Both inductors are wound with litz wire with 20 strands of diameter 0.355 mm and a number of turns of 27, so that a minimum inductance value of 100 µH is guaranteed at the highest peak current.

Again, the core losses are calculated by using the iGSE as given in Section B.2.2, the Steinmetz parameters are obtained from the material curves provided by the manufacturer [155]. The skin and proximity effect losses in the litz wire for each current harmonic are calculated according to Section B.2.1 with a 1D magnetic field approximation.

Capacitors

For the AC- and DC-side capacitors C_{ac}, C_{dc}, paralleled 560 nF, 500 V ceramic capacitors with dielectric X7R from Syfer [156] are used. For achieving high power densities, multilayer ceramic capacitors are ideally suited because they offer comparable high energy densities and allow high current ripples. The applied loss model by considering the equivalent series resistance (ESR) from the manufacturers data sheet is discussed in Section B.3.

Auxiliary losses

Besides the load-dependent losses shown in the previous sections, a constant loss share of 6 W for the pre-charging relay, the FPGA control board, the sensing and the fans is considered. Furthermore, the EMI filter losses are approximated by an equivalent resistance of 4 mΩ.

Cooling system

The number of semiconductors basically defines the base plate size of the heat sink as 80 mm × 65 mm for the AC- and DC-side switching devices, so that a double-sided heat sink can be used. Two 40 mm × 40 mm fans of type San Ace 40 are applied for forced convection cooling. After optimizing the cooling system as described in [157] considering a minimum fin thickness of 1 mm and a minimum fin spacing of 2 mm, a thermal sink to ambient resistance of $R_{\mathrm{th,s\text{-}a}} = 0.32\,\mathrm{K/W}$ results which in turn leads to a cooling system performance index (CSPI) of 9.86.

4.5.2 Efficiency calculations

For the previously described module design with its components and loss models, the efficiencies over the output power range are calculated for battery voltages of 280 V, 350 V and 420 V. The results are shown in **Fig. 4.14**. Additionally, the efficiency curve applying the phase shift modulation for an output voltage of 350 V is shown where the MOSFETs are partly operated under hard-switching conditions so that the reachable efficiency is comparably low. For low output power, the efficiency curves diverge because of the high transformer leakage inductance peak currents occurring at high output voltages. In low power mode, mainly a triangular-like leakage inductance current occurs at the maximum switching frequency of 120 kHz where the peak current is directly proportional to the output voltage. With the presented design of the AC-DC DAB module and the application of the described loss models, a maximum theoretical efficiency of 97 % at an output power of 2.5 kW and the lowest battery voltage of 280 V is predicted.

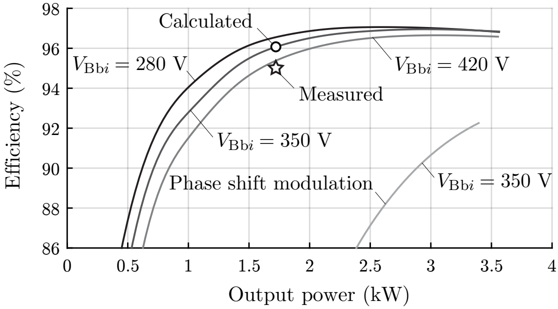


Figure 4.14: Calculated efficiencies of the AC-DC DAB module applying the ZVS modulation with variable switching frequency (see Section 4.3.2) over the output power range for the battery voltages 280 V, 350 V and 420 V. The hardware prototype discussed in Section 4.5.3 exhibits an efficiency of around 95 % at an output voltage of 350 V. Additionally, the efficiency curve applying the phase shift modulation at an output voltage of 350 V is shown.

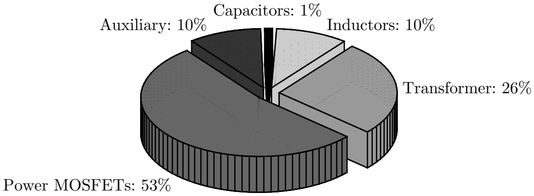


Figure 4.15: Calculated loss distribution between the AC-DC DAB module components at the maximum output power of 3.56 kW and a battery voltage of 350 V applying the ZVS modulation with variable switching frequency (see Section 4.3.2).

The loss distribution between the module components at the maximum output power of 3.58 kW and a battery voltage of 350 V is depicted in **Fig. 4.15**. The major parts of the losses represent the MOSFET losses with a percentage of 53 % and the transformer losses with a percentage of 26 %. The remaining percentage accounts for the losses occurring in the AC- and DC-side filter inductors and capacitors as well as the auxiliary losses for the sensing, the control and the cooling.

4.5.3 Hardware prototype

For validating the theoretical analysis of the ZVS modulation with variable switching frequency, the above discussed AC-DC DAB module design is realized as an electric vehicle battery charger for lithium-ion batteries with a 3.3 kW nominal output power to connect to the single-phase AC mains. A photograph is shown in **Fig. 4.16**. The parameters of the hardware prototype are given above in **Tab. 4.3** with the previously presented components listed in **Tab. 4.4**.

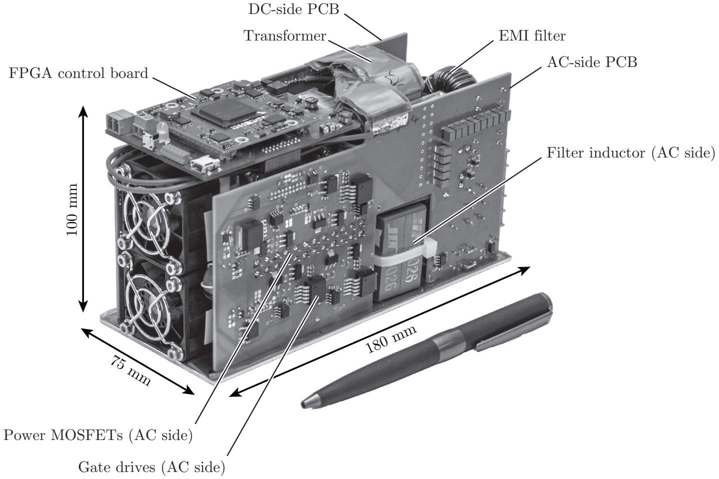

DC-side PCB
Transformer
EMI filter
AC-side PCB
FPGA control board
Filter inductor (AC side)
100 mm
75 mm
180 mm
Power MOSFETs (AC side)
Gate drives (AC side)

Figure 4.16: Photograph of the hardware prototype system for experimental verification of the ZVS modulation with variable switching frequency (see Section 4.3.2).

The control of the DAB module is based on a PLL for the synchronization to the AC mains voltage $v_{\mathrm{b}i}$, a LUT to store the optimal control variables $g_{\mathrm{b}i}$, $w_{\mathrm{b}i}$, $T_{\mathrm{sb}i}$ obtained from the numerical optimization shown in **Fig. 4.8** as well as a PI controller for adjusting the switching period $T_{\mathrm{sb}i}$ to shape the AC input current i_{b}. An overview of the control is depicted in **Fig. 4.17** with the details discussed in the following.

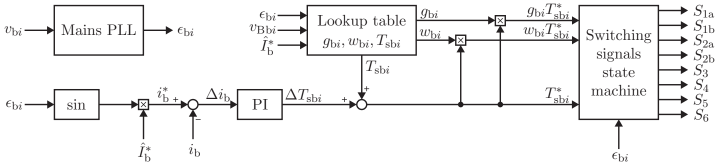

$v_{\mathrm{b}i}$
Mains PLL
$\epsilon_{\mathrm{b}i}$
$\epsilon_{\mathrm{b}i}$
sin
i_{b}^{*}
$\hat{I}_{\mathrm{b}}^{*}$
Δi_{b}
i_{b}
PI
$\Delta T_{\mathrm{sb}i}$
$\epsilon_{\mathrm{b}i}$
$v_{\mathrm{Bb}i}$
$\hat{I}_{\mathrm{b}}^{*}$
Lookup table
$g_{\mathrm{b}i}, w_{\mathrm{b}i}, T_{\mathrm{sb}i}$
$T_{\mathrm{sb}i}$
$g_{\mathrm{b}i}$
$w_{\mathrm{b}i}$
$g_{\mathrm{b}i}T_{\mathrm{sb}i}^{*}$
$w_{\mathrm{b}i}T_{\mathrm{sb}i}^{*}$
$T_{\mathrm{sb}i}^{*}$
Switching signals state machine
$\epsilon_{\mathrm{b}i}$
$S_{1\mathrm{a}}$
$S_{1\mathrm{b}}$
$S_{2\mathrm{a}}$
$S_{2\mathrm{b}}$
S_{3}
S_{4}
S_{5}
S_{6}

Figure 4.17: Overview of the AC-DC DAB module control including the mains PLL to determine the mains angle $\epsilon_{\mathrm{b}i}$, a LUT to store the optimal control variables $g_{\mathrm{b}i}$, $w_{\mathrm{b}i}$, $T_{\mathrm{sb}i}$ as well as a PI controller for adjusting the switching period $T_{\mathrm{sb}i}$ to shape the AC input current i_{b}.

Mains PLL

The mains PLL includes an orthogonal system generator (OSG) implemented with a second order generalized integrator (SOGI) structure as proposed in [147, 148]. With the OSG-SOGI structure, two clean orthogonal voltage waveforms v_{α}, v_{β} are constructed. These are then transformed into rotating dq-coordinates and v_{d} is controlled to zero (synchronization to a sinusoidal waveform) to derive the mains angle $\epsilon_{\mathrm{b}i}$.

Lookup table (LUT)

The LUT stores the optimal control variables $g_{\mathrm{b}i}$, $w_{\mathrm{b}i}$, $T_{\mathrm{sb}i}$ for an AC mains half-wave dependent on the mains angle $\epsilon_{\mathrm{b}i}$ and parameterized with the battery voltage $v_{\mathrm{Bb}i}$ and the reference current amplitude $\hat{I}_{\mathrm{b}}^{*}$. The output of the switching period $T_{\mathrm{sb}i}$ serves as a feed-forward value for the PI controller that adds a $\Delta T_{\mathrm{sb}i}$ to it as shown in **Fig. 4.17**. The resulting $T_{\mathrm{sb}i}^{*}$ gets then multiplied by $g_{\mathrm{b}i}$ and $w_{\mathrm{b}i}$.

Switching signals state machine

The switching signals state machine generates the gate signals for the switches $S_{1\mathrm{a}}$, $S_{1\mathrm{b}}$, $S_{2\mathrm{a}}$, $S_{2\mathrm{b}}$, S_{3}, S_{4}, S_{5}, S_{6} from $g_{\mathrm{b}i}T_{\mathrm{sb}i}^{*}$, $w_{\mathrm{b}i}T_{\mathrm{sb}i}^{*}$, $T_{\mathrm{sb}i}^{*}$

according to **Fig. 4.18**. There, only the gating signals for the power flow from the AC mains to the battery side for the ZVS modulation with variable switching frequency are shown (the modulation corresponds to the *lagging outer mode* depicted in **Fig. 4.7(a)**). The interlocking interval is set to a fixed time t_i depending on the switching speed of the used MOSFETs and the commutation paths (parasitic inductances) of the PCB layout.

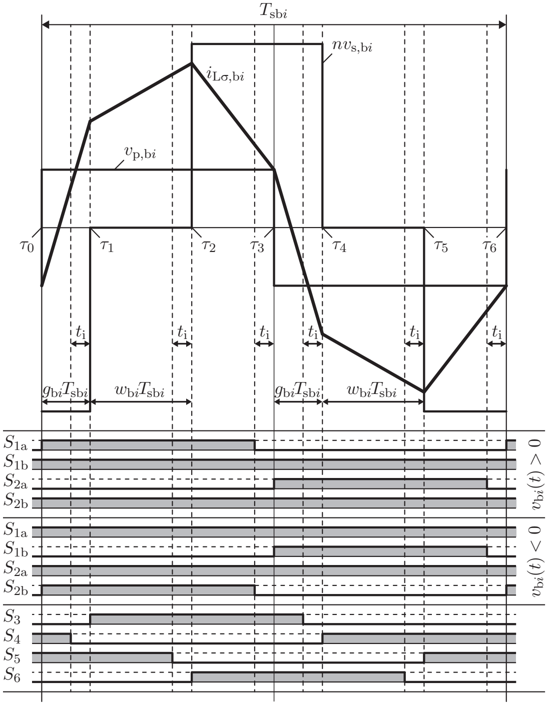

$T_{\mathrm{sb}i}$
$nv_{\mathrm{s,b}i}$
$i_{\mathrm{L}\sigma,\mathrm{b}i}$
$v_{\mathrm{p,b}i}$
τ_0
τ_1
τ_2
τ_3
τ_4
τ_5
τ_6
t_i
$g_{\mathrm{b}i}T_{\mathrm{sb}i}$
$w_{\mathrm{b}i}T_{\mathrm{sb}i}$
$S_{1\mathrm{a}}$
$S_{1\mathrm{b}}$
$S_{2\mathrm{a}}$
$S_{2\mathrm{b}}$
$v_{\mathrm{b}i}(t) > 0$
$v_{\mathrm{b}i}(t) < 0$
S_3
S_4
S_5
S_6

Figure 4.18: Switching states of the switches $S_{1\mathrm{a}}$, $S_{1\mathrm{b}}$, $S_{2\mathrm{a}}$, $S_{2\mathrm{b}}$, S_3, S_4, S_5, S_6 of the AC-DC DAB module during a switching cycle $T_{\mathrm{sb}i}$ for the ZVS modulation with variable switching frequency (see Section 4.3.2). t_i denotes the interlocking time which is set to a constant value over the whole 50 Hz grid cycle, despite the variable switching frequency. During the positive half-cycle of the module voltage $v_{\mathrm{b}i}$, the switches $S_{1\mathrm{b}}$ and $S_{2\mathrm{b}}$ are constantly on whereas for the negative half-cycle $S_{1\mathrm{a}}$ and $S_{2\mathrm{a}}$ are constantly on.

PI controller

For the PI controller design, the small-signal transfer function from $\Delta T_{\mathrm{sb}i}$ to Δi_{b} is derived from (4.45) and given as

$$G_{\mathrm{p}} = \frac{\Delta i_{\mathrm{b}}}{\Delta T_{\mathrm{sb}i}} = \frac{n v_{\mathrm{Bb}i}\left(2g_{\mathrm{b}i} - 4g_{\mathrm{b}i}^2 + w_{\mathrm{b}i} - 2w_{\mathrm{b}i}^2 - 4g_{\mathrm{b}i}w_{\mathrm{b}i}\right)}{4L_{\sigma}}. \tag{4.74}$$

Since the AC-DC DAB module is not operated near the resonant frequency of the resonant tank formed by the capacitors C_{ac}, C_{dc} and the leakage inductance L_{σ}, the dynamics of these passive elements can be neglected what has been also a prerequisite for describing $i_{\mathrm{L}\sigma,\mathrm{b}i}$ with linear equations. The transfer function G_{p} is mainly dependent on the mains angle $\epsilon_{\mathrm{b}i}$ (indirectly via the control variables $g_{\mathrm{b}i}(\epsilon_{\mathrm{b}i}), w_{\mathrm{b}i}(\epsilon_{\mathrm{b}i})$) and the battery voltage $v_{\mathrm{Bb}i}$. To compensate the voltage dependencies, the proportional and integral gain of the PI controller are scaled by

$$K = \frac{1}{G_{\mathrm{p}}} = \frac{4L_{\sigma}}{n v_{\mathrm{Bb}i}\left(2g_{\mathrm{b}i} - 4g_{\mathrm{b}i}^2 + w_{\mathrm{b}i} - 2w_{\mathrm{b}i}^2 - 4g_{\mathrm{b}i}w_{\mathrm{b}i}\right)} \tag{4.75}$$

such that

$$K_{\mathrm{P}} = K\widetilde{K}_{\mathrm{P}}, \tag{4.76}$$

$$K_{\mathrm{I}} = K\widetilde{K}_{\mathrm{I}} \tag{4.77}$$

where $\widetilde{K}_{\mathrm{P}}$, $\widetilde{K}_{\mathrm{I}}$ are the constant gains and K_{P}, K_{I} the effective and adaptive ones. The closed-loop transfer function can be written as

$$G_{\mathrm{cl}} = \frac{G_{\mathrm{PI}}G_{\mathrm{p}}}{1 + G_{\mathrm{PI}}G_{\mathrm{p}}} = \frac{\widetilde{K}_{\mathrm{I}} + \widetilde{K}_{\mathrm{P}}s}{\widetilde{K}_{\mathrm{I}} + (1 + \widetilde{K}_{\mathrm{P}})s} \tag{4.78}$$

with G_{PI} being the transfer function of the PI controller

$$G_{\mathrm{PI}} = K_{\mathrm{P}} + \frac{K_{\mathrm{I}}}{s} = K\left(\widetilde{K}_{\mathrm{P}} + \frac{\widetilde{K}_{\mathrm{I}}}{s}\right). \tag{4.79}$$

By setting $\widetilde{K}_{\mathrm{P}} = 0$, the closed-loop transfer function can be simplified to a first-order system

$$G_{\mathrm{cl}} = \frac{1}{1 + \frac{1}{\widetilde{K}_{\mathrm{I}}}s} \tag{4.80}$$

where the rise time from 10 % to 90 % of the steady-state value in the step response is given by

$$t_{\mathrm{r}} = \frac{2.2}{\widetilde{K}_{\mathrm{I}}}. \tag{4.81}$$

Since the controller tracks a sinusoidal waveform, the rise time should be kept small in the magnitude of a few switching periods $T_{\mathrm{sb}i,\mathrm{max}}$ at the lowest switching frequency. With a rise time of $t_{\mathrm{r}} = 100\,\mu\mathrm{s}$, the controller gains are determined to be $\widetilde{K}_{\mathrm{P}} = 0$ and $\widetilde{K}_{\mathrm{I}} = 22'000$ for the hardware prototype.

4.5.4 Experimental verification

For conducting experiments at the hardware prototype, the control of the DAB module (see **Fig. 4.17**) is implemented in VHDL on an Altera Cyclone IV [158] FPGA device. The optimization of the control variables is done offline with the results stored in LUTs on the FPGA. The interlocking time for the used switching devices is set to 500 ns. For each parallel connection of two MOSFETs, a 10 nF ceramic capacitor is placed in parallel in order to limit the $\mathrm{d}i_{\mathrm{ds}}/\mathrm{d}t$ and therefore the ringing of the drain-source voltage v_{ds} at the end of the resonant transition. Under these circumstances, a minimum commutation current I_{ZVS} of 5 A per device is found to be sufficient for achieving ZVS over the whole AC mains cycle.

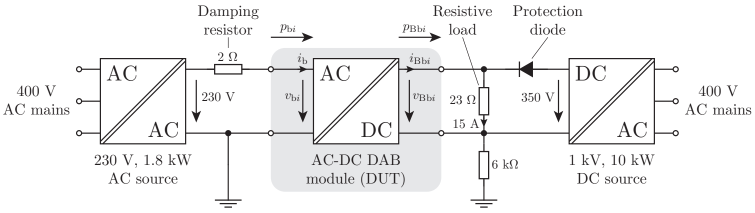

Damping resistor
$p_{\mathrm{b}i}$
$p_{\mathrm{Bb}i}$
Resistive load
Protection diode
2 Ω
i_{b}
$i_{\mathrm{Bb}i}$
400 V AC mains
AC
AC
230 V
$v_{\mathrm{b}i}$
AC
DC
$v_{\mathrm{Bb}i}$
23 Ω
15 A
350 V
DC
AC
400 V AC mains
230 V, 1.8 kW AC source
AC-DC DAB module (DUT)
6 kΩ
1 kV, 10 kW DC source

Figure 4.19: Overview of the measurement setup to conduct experiments at the AC-DC DAB module (device under test - DUT). The storage battery is simulated by a 1 kV, 10 kW DC source operated in constant voltage mode at 350 V. A resistive load is connected via a series protection diode to draw a current of 15 A from the DC source when the DAB module is switched off. In this way, the power can flow from the AC to the DC side of the DAB module.

The experiments are conducted by using an AC source capable of delivering 8 A at 230 V connected to the input of the hardware prototype and a 1 kV, 10 kW DC source connected to the output of the hardware prototype to simulate a battery voltage of 350 V (see **Fig. 4.19**). A resistive load draws 15 A via a series protection diode from the DC source when the DAB module is switched off. In this way, the power can flow from the AC input of the module to the DC output preventing power flowing back into the DC supply. Furthermore, the over-voltage protection of the DAB module monitors the DC link voltage v_{dc} and trips in case of a rapid voltage rise. Additionally, a damping resistor in series to the AC input is inserted to prevent oscillations between the AC source and the input filter of the DAB module.

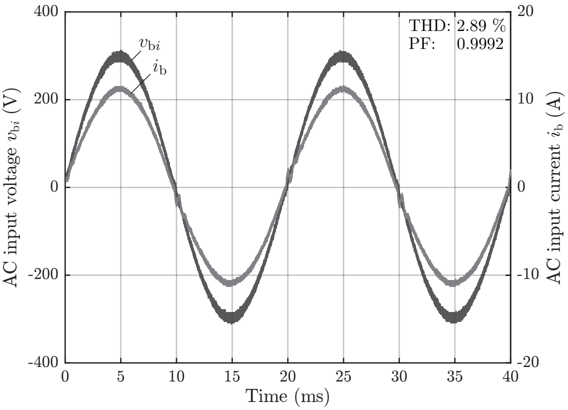


Figure 4.20: Measured AC input current i_{b} and AC input voltage $v_{\mathrm{b}i}$ for an input current reference $\hat{I}_{\mathrm{b}}^{*} = \sqrt{2} \cdot 8\,\mathrm{A}$ and a DC output voltage of 350 V in AC-to-DC operation for a mains voltage of 230 V.

For the measurements, the AC current controller described above is enabled and its reference set to 8 A. **Fig. 4.20** shows the measured AC input current i_{b} together with the AC input voltage $v_{\mathrm{b}i}$ whereas **Fig. 4.21** depicts the measured DC output current $i_{\mathrm{Bb}i}$ and the DC link voltage v_{dc} across the capacitor C_{dc}.

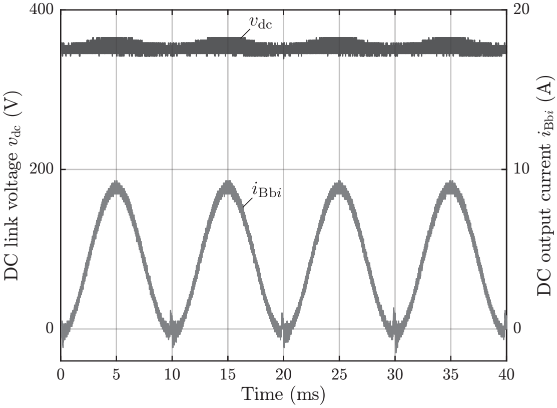


Figure 4.21: Measured DC output current $i_{\mathrm{Bb}i}$ and DC link voltage v_{dc} for an input current reference $\hat{I}_{\mathrm{b}}^{*} = \sqrt{2} \cdot 8\,\mathrm{A}$ and a DC output voltage of 350 V in AC-to-DC operation for a mains voltage of 230 V.

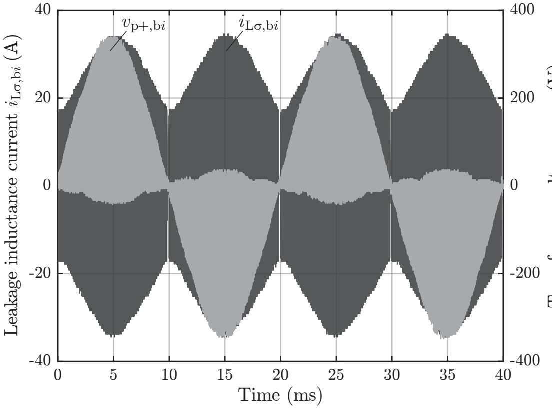


Figure 4.22: Measured transformer leakage inductance current $i_{\mathrm{L}\sigma,\mathrm{b}i}$ and transformer voltage $v_{\mathrm{p+,b}i}$ (transformer connection p+ to negative AC input rail) for an input current reference $\hat{I}_{\mathrm{b}}^{*} = \sqrt{2} \cdot 8\,\mathrm{A}$ and a DC output voltage of 350 V in AC-to-DC operation for a mains voltage of 230 V.

During the zero-crossing of the AC voltage, all MOSFETs are opened for a short time period, so that i_b starts to ring when the switching operation is started again. Oscillations can also be seen in the DC output current $i_{\mathrm{Bb}i}$ when it touches the zero-line.

The measurements of the voltages and the currents at the transformer are given in **Fig. 4.22** and **Fig. 4.23**. The transformer leakage inductance current $i_{\mathrm{L}\sigma,\mathrm{b}i}$ exhibits the typical envelope with twice the AC input voltage frequency. The transformer voltage $v_{\mathrm{p+,b}i}$ measured from point p+ to the negative AC input rail shows square-wave voltages with amplitudes following the AC input voltage. During the first half-wave of the input voltage, the amplitudes are positive, during the second half-wave they are negative. The transformer voltages $v_{\mathrm{s+,b}i}$, $v_{\mathrm{s-,b}i}$ are measured from points s+, s− to the negative DC output rail and show square-wave voltages with a constant amplitude of the DC output voltage.

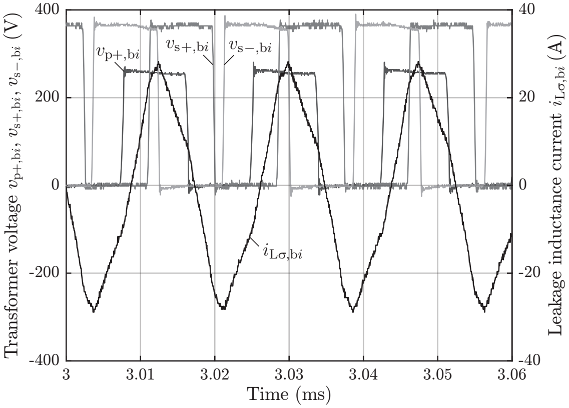


Figure 4.23: Measured transformer leakage inductance current $i_{\mathrm{L}\sigma,\mathrm{b}i}$ and transformer voltages $v_{\mathrm{p+,b}i}$, $v_{\mathrm{s+,b}i}$, $v_{\mathrm{s-,b}i}$ (transformer connection p+ to negative AC input rail, transformer connections s+, s− to negative DC output rail) for an input current reference $\hat{I}_\mathrm{b}^* = \sqrt{2}\cdot 8\,\mathrm{A}$ and a DC output voltage of 350 V in AC-to-DC operation for a mains voltage of 230 V.

The postprocessing of the waveforms i_b, $v_{\mathrm{b}i}$ from **Fig. 4.20** leads to a total harmonic distortion (THD) of 2.89 % and a power factor (PF) of 0.9992 at the given operating point. The AC input current harmonics compared to the IEC 61000-3-2 class A standard are given in **Fig. 4.24**. It can be seen, that the proposed ZVS modulation scheme with variable switching frequency guarantees full compliance of the AC-DC DAB module with the IEC standard.

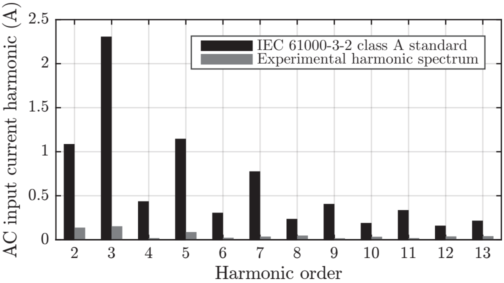


Figure 4.24: Experimental AC input current harmonics compared to the IEC 61000-3-2 class A standard for an input current reference $\hat{I}_{\mathrm{b}}^{*} = \sqrt{2} \cdot 8\,\mathrm{A}$ and an output voltage of 350 V in AC-to-DC operation for a mains voltage of 230 V.

Besides the oscilloscope measurements presented above for validating the developed ZVS modulation scheme with variable switching frequency, the instantaneous input power $p_{\mathrm{b}i}$ as well as the instantaneous output power $p_{\mathrm{Bb}i}$ of the AC-DC DAB module are measured as depicted in **Fig. 4.19**. With the power analyzer LMG670 from ZES ZIMMER [159], the power curves shown in **Fig. 4.25** are obtained. The power curves exhibit the typical sinusoidal waveform with twice the AC mains frequency. The ringing of the DC output current $i_{\mathrm{Bb}i}$ during the zero-crossing of the mains voltage $v_{\mathrm{b}i}$, when the switching operation is started again after a small dead time (see **Fig. 4.21**), leads also to oscillations seen in the output power curve $p_{\mathrm{Bb}i}$. The DC output voltage $v_{\mathrm{Bb}i}$ during that time stays constant without any oscillations observed.

The measured efficiency is determined to be 95 % for an AC mains voltage of 230 V, a DC output voltage of 350 V and an input current reference of 8 A. The power density is around 2.5 kW/L. The measurement at 1.7 kW output power is compared to the calculated efficiency curves in **Fig. 4.14**. From the calculation with the applied loss models presented in Section 4.5.1 an efficiency of around 96 % is obtained. The difference in losses is mainly due to the assumption of relatively small switching losses of the MOSFETs under ZVS conditions. The applied device STY139N65M5 [149] exhibits a relatively small on-state resistance but a large output capacitance which demands a corresponding commutation current for the resonant transition during the interlocking interval. Increased minimal currents at the switching instants in combination with a slow turn-off of the MOSFET have a substantial impact on the semiconductor losses. By using devices with an improved switching behavior as for example from the 650 V CoolMOS$^{\mathrm{TM}}$ C7 series [160], the efficiency of the hardware prototype could be further increased.

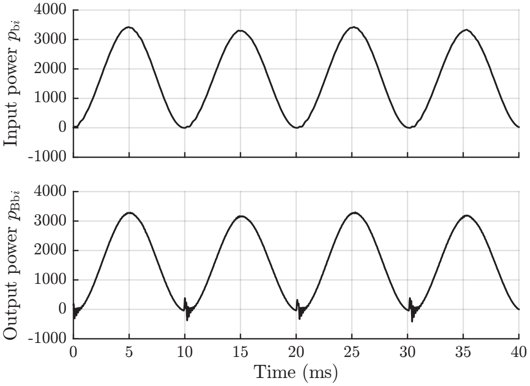


Figure 4.25: Measured input power $p_{\mathrm{b}i}$ and output power $p_{\mathrm{Bb}i}$ of the AC-DC DAB module (see **Fig. 4.19**) for an input current reference $\hat{I}_{\mathrm{b}}^{*} = \sqrt{2} \cdot 8\,\mathrm{A}$ and a DC output voltage of 350 V in AC-to-DC operation for a mains voltage of 230 V.

4.6 System simulation

The cascaded AC-DC DAB converter is simulated in GeckoCIRCUITS [161] with a simulation model according to **Fig. 4.1** of a 45 kW battery energy storage system connected to a 2.4 kV AC grid. The simulation model applies three AC-DC DAB modules per phase leg with an input voltage of 460 V ± 30 % and a nominal output power of 5 kW. Each module is connected to a storage battery pack modeled as a constant voltage source of 350 V with an energy capacity of 3.33 Wh. The energy capacity is chosen to be small to limit the simulation time to just a few hours. **Tab. 4.5** summarizes the parameters for the simulations performed.

Table 4.5: Parameters of the cascaded AC-DC converter with integrated battery energy storage system for simulation purposes.

Cascaded AC-DC DAB converter		
AC grid voltage (RMS line-to-line)	V_{abc}	2.4 kV
AC grid frequency	f_{abc}	50 Hz
Nominal system power	P_{abc}	45 kW
Total energy storage capacity	E_{abc}	30 Wh
Grid-side filter inductors	L_{ac}	100 µH
Number of modules per phase leg	N	3

AC-DC DAB module		
Input voltage (RMS)	$V_{\mathrm{b}i}$	460 V ± 30 %
Nominal output power	$P_{\mathrm{Bb}i}$	5 kW
Switching frequency	f_{s}	20 kHz
Transformer turns ratio	n	14/9
Transformer leakage inductance	L_{σ}	47 µH
Transformer magnetizing inductance	L_{m}	neglected
Grid-side capacitors	C_{ac}	20 µF
Battery-side inductors	L_{dc}	100 µH
Battery-side capacitors	C_{dc}	60 µF

Storage battery		
Battery voltage	$V_{\mathrm{Bb}i}$	350 V
Energy storage capacity	$E_{\mathrm{Bb}i}$	3.33 Wh

For validating the control concept discussed in Section 4.4, the top-level as well as the module-level control are implemented in Java. Each AC-DC DAB module applies the ZCS/ZVS modulation with fixed switching frequency (see Section 4.3.1). The input current reference is set to $I^{*}_{\mathrm{abc}} = 10\,\mathrm{A}$ for charging operation. Initially, the SOCs of the batteries are in an unbalanced state.

Fig. 4.26 shows the simulated grid currents i_a, i_b, i_c together with the grid voltages v_a, v_b, v_c. The currents are controlled to the reference amplitudes and in phase to the grid voltages (PFC operation).

In **Fig. 4.27**, the module input voltages $v_{\mathrm{a}i}$, $v_{\mathrm{b}i}$, $v_{\mathrm{c}i}$ and the battery currents $i_{\mathrm{Ba}i}$, $i_{\mathrm{Bb}i}$, $i_{\mathrm{Bc}i}$ are depicted. It can be seen, that the module voltage controller adjusts the module input voltages according to the reference given by the top-level control and the battery SOC balancing control. The overall power flow into the batteries is accordingly divided as can be seen from the battery currents.

From **Fig. 4.28**, the balancing of the battery SOCs by the phase SOC and the battery SOC balancing control can be seen. The initial SOC imbalance gets smaller during the charging operation of the batteries. The changes of the battery currents over time show the different power requirements of the batteries to finally end up in a balanced state where the battery currents converge to the same values.

In **Fig. 4.29**, the phase SOC deviations (4.60), (4.61), (4.62) as well as the battery SOC deviations (4.65), (4.66), (4.67) are depicted. Due to the charging with pulsating currents, the SOCs exhibit small ripples with double the grid frequency.

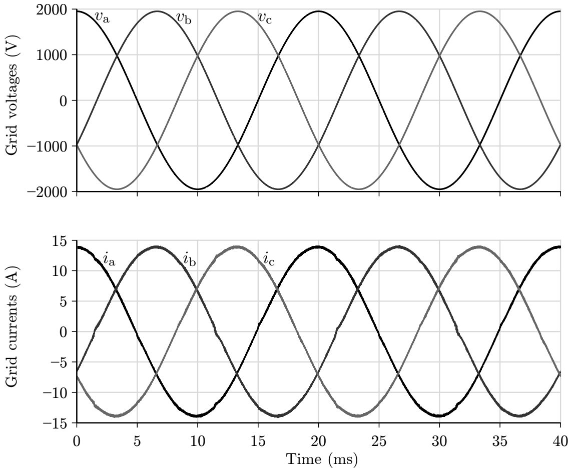


Figure 4.26: Simulated grid currents of the cascaded AC-DC DAB converter with parameters given in **Tab. 4.5** for $I^*_\mathrm{abc} = 10\,\mathrm{A}$ in charging operation.

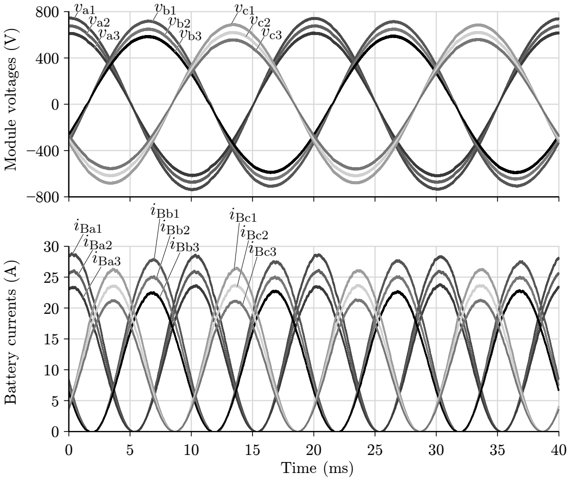


Figure 4.27: Simulated module voltages and battery currents of the cascaded AC-DC DAB converter with parameters given in **Tab. 4.5** for $I^*_{\mathrm{abc}} = 10\,\mathrm{A}$ in charging operation.

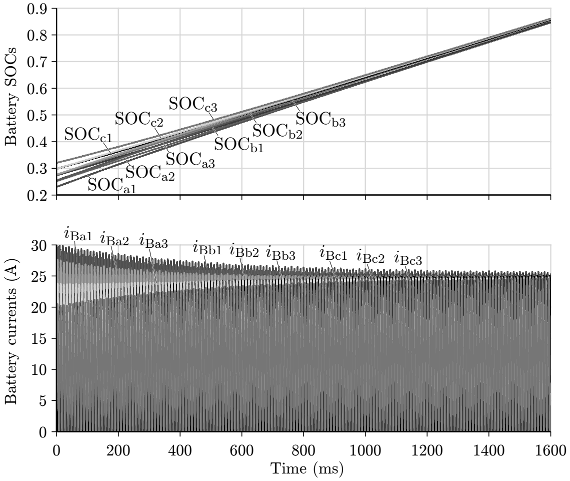


Figure 4.28: Simulated battery SOCs and currents of the cascaded AC-DC DAB converter with parameters given in **Tab. 4.5** for $I^*_{\mathrm{abc}} = 10\,\mathrm{A}$ in charging operation.

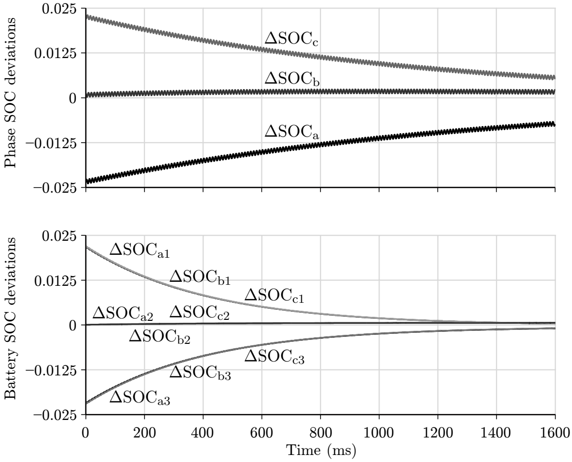


Figure 4.29: Simulated phase SOC and battery SOC deviations of the cascaded AC-DC DAB converter with parameters given in **Tab. 4.5** for $I^*_{\mathrm{abc}} = 10\,\mathrm{A}$ in charging operation.

4.7 Summary and conclusion

In this chapter, a new cascaded AC-DC DAB converter for battery energy storage systems is developed. The topology is derived from a state-of-the-art CHB converter and integrates module-level galvanic isolation using series-connected single-stage bidirectional isolated AC-DC converter modules.

Possible AC-DC DAB module topologies are discussed considering their degrees of freedom in control and performing a qualitative comparison of the semiconductor losses. The topology with an AC-side half-bridge and a DC-side full-bridge is identified as the most suitable one since the hardware control effort as well as the system costs can be significantly reduced compared to a standard full-bridge/full-bridge DAB. By taking the switching frequency into consideration for control, an additional degree of freedom for optimizing the transformer peak and/or RMS currents becomes available. From the semiconductor losses point of view, the AC-side half-bridge is comparable to an AC-side full-bridge assuming full-block voltage operation without clamping. At the DC side, for the same degrees of freedom in control, the use of a full-bridge is more beneficial than using a T-type circuit since commonly the clamping interval is minimized in order to reduce the circulating current and therefore the reactive power.

Furthermore, the operating principle on module as well as on system level is presented. The AC-DC DAB modules are modeled by their capacitive voltage ports consisting of the series connection of two filter capacitors and a controlled current source in parallel. By adjusting the power transfer of a DAB module, the current source is controlled in order to regulate the AC-side module voltage and therefore the grid current. By controlling the module voltage, also the power distribution among the modules is set since all modules in a phase string are connected in series and exhibit the same module current.

For the AC-DC DAB module, two different modulation schemes are developed. A first one which allows ZCS at the grid side with IGBTs and ZVS at the battery side with MOSFETs presuming a constant switching frequency and a second one which allows ZVS on both sides with MOSFETs considering also the variation of the switching frequency. The mathematical analysis of the transformer leakage inductance current by using piecewise linear equations is given to derive the power flow equations including their borders for the minimum and the maximum power transfer. For the ZVS modulation with variable switching frequency, the optimal control variables are determined by a numerical optimization to minimize the transformer leakage inductance peak currents.

The overall control of the cascaded AC-DC DAB converter with an integrated battery energy storage system is described with a top-level as well as a module-level control. The objectives of the top-level control are obtaining the grid and phase angles by means of PLLs, controlling the grid current in the dq-frame and balancing the average SOC values of the storage batteries over the three phases. On the module level, the SOCs of the batteries in one phase are balanced and the grid-side module voltages are controlled.

For validating the theoretical aspects of the new ZVS modulation including switching frequency variation, an AC-DC DAB module is designed and a 3.3 kW hardware prototype built. For conducting experiments, the control of the DAB module is implemented in VHDL on an FPGA device. The measurements at the hardware prototype conform to the developed mathematical models and the harmonics of the AC module current fully comply with the IEC 61000-3-2 class A standard.

The measured efficiency of the prototype at 1.7 kW output power is 95 % whereas the reached power density is around 2.5 kW/L.

Finally, a 45 kW cascaded AC-DC DAB converter with an integrated battery energy storage system connected to a 2.4 kV AC grid is simulated to validate the aspects of the developed control structure on system and module level. The simulation model applies three AC-DC DAB modules per phase leg with an input voltage of 460 V ± 30 % and a nominal output power of 5 kW. Each module is connected to a storage battery pack modeled as a constant voltage source of 350 V. The simulation curves verify the effectiveness of the discussed control methods to balance the SOCs between the phase legs as well as between the single batteries in a phase leg while maintaining sinusoidal grid currents in phase with the grid voltages (PFC operation).

5

Cascaded AC-DC Multi-Port Converter

This chapter proposes a new cascaded AC-DC multi-port converter for battery energy storage systems. The topology is derived from state-of-the-art DC-DC multi-port converters in order to integrate module-level galvanic isolation and to provide bidirectional power flow capability. For a three-phase AC-DC multi-port converter module, a new modeling approach for the power flows at the AC and the DC ports is presented and suitable modulation schemes are developed to shape the AC currents while maintaining soft-switching conditions over the full AC grid cycle. A module prototype is designed as well as its components and losses modeled to evaluate the efficiency of the proposed converter module. Finally, the converter module is simulated to validate the theoretical analysis of the power flows and the introduced modulation schemes.

5.1 Introduction to multi-port converters

Multi-port converters allow the coupling of several power sources and loads/sinks by the use of a single power electronic converter system. Most of the multi-port converters discussed in literature offer galvanically isolated ports and bidirectional power flow capability between the ports. The galvanic isolation is realized by magnetically coupling the ports with a multi-winding transformer.

The main application area of multi-port converters are future energy distribution systems where so-called solid state transformers (SST) interface with local generation like wind or solar power, energy storage systems, electric vehicles (EVs), utility AC or DC grids or in general AC and DC loads. With the upcoming integration of distributed generation, intelligent multi-port converter systems can substantially enhance the reliability of the distribution system by providing reactive power compensation to the grid as well as current limiting and energy storage management functions.

Research has mainly focused on DC-DC multi-port converter topologies. The most prominent example is the bidirectional isolated three-port DC-DC converter based on the single-phase DAB converter [108–113] or on the three-phase DAB converter [114]. Further publications describe concepts of a general N-port DC-DC converter with the focus on deriving the mathematical models of the power flows [116, 117].

Isolated multi-port converters with combined AC and DC ports (see **Fig. 3.10**) have been rarely discussed in literature. Publications have mainly focused on three-phase isolated rectifier topologies based on a multi-port topology. In this chapter, the well-known DC-DC multi-port converter is extended to a multi-port converter with combined AC and DC ports. For an AC-DC multi-port module in a battery energy storage system, a comprehensive investigation of the topology, the power flow modeling and suitable modulation schemes is given.

5.2 Converter topology

Similar to the derivation of the cascaded AC-DC DAB converter in the preceding chapter, the cascaded AC-DC multi-port converter topology for battery energy storage systems depicted in **Fig. 5.1** is based on a conventional cascaded H-bridge (CHB) converter [48, 89] in star connection. The main difference is, that each converter module consists of three AC ports for the phases a, b and c and one DC port to attach a storage battery pack. Each converter module represents a bidirectional isolated AC-DC multi-port converter where the three AC ports belonging to the three different phases and the DC port are magnetically coupled through a four-winding transformer providing the galvanic isolation. The converter system consists of three phase strings/legs which are tied together at a common star point. In a phase string, several AC-DC multi-port converter modules are connected in series at their respective AC ports together with a filter inductor L_{ac}.

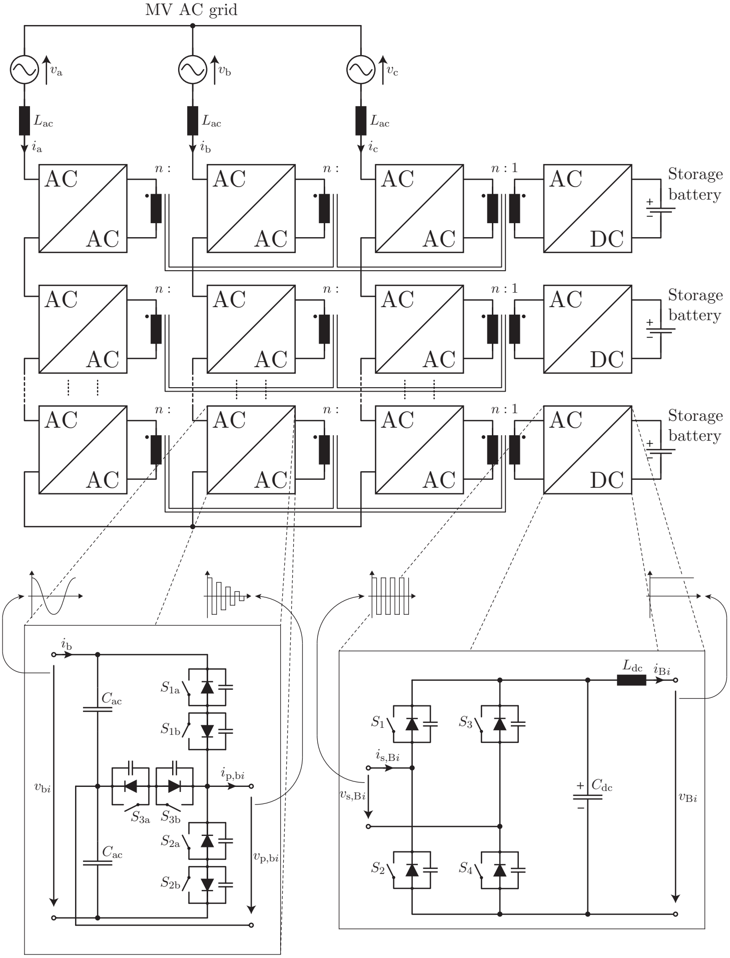

MV AC grid
v_{a}
v_{b}
v_{c}
L_{ac}
L_{ac}
L_{ac}
i_{a}
i_{b}
i_{c}
AC
AC
AC
DC
$n:$
$n:1$
Storage battery
+
−
i_{b}
C_{ac}
$S_{1\mathrm{a}}$
$S_{1\mathrm{b}}$
$i_{\mathrm{p,b}i}$
$v_{\mathrm{b}i}$
$S_{3\mathrm{a}}$
$S_{3\mathrm{b}}$
$S_{2\mathrm{a}}$
C_{ac}
$v_{\mathrm{p,b}i}$
$S_{2\mathrm{b}}$
L_{dc}
$i_{\mathrm{B}i}$
S_1
S_3
$i_{\mathrm{s,B}i}$
$v_{\mathrm{s,B}i}$
C_{dc}
$v_{\mathrm{B}i}$
S_2
S_4

Figure 5.1: Cascaded AC-DC multi-port converter in star connection for battery energy storage systems with series-connected AC-DC multi-port modules applying grid-side T-type blocks with bidirectional switches, battery-side full-bridges with unidirectional switches and four-winding medium-frequency transformers providing galvanic isolation. Each module is connected to a storage battery at the DC side. The module input voltages $v_{\mathrm{a}i}$, $v_{\mathrm{b}i}$, $v_{\mathrm{c}i}$ correspond to sinusoidal voltage waveforms with the grid frequency.

5.2.1 Module topology

Each of the modules exhibit three grid-side low-frequency (LF) AC voltage ports (with capacitors C_{ac}) and a DC voltage port (with capacitor C_{dc}) as shown in **Fig. 5.2** exemplarily for a module i. The DC voltage port is connected through a filter inductor L_{dc} to a storage battery.

The module topology applies grid-side T-type blocks with bidirectional switches and a battery-side full-bridge with unidirectional switches. The four-winding medium-frequency (MF) transformer provides the galvanic isolation between the medium voltage (MV) grid and the storage battery and serves as an energy transfer node where the windings of the three AC ports and the DC port are magnetically coupled.

Since each of the three AC ports inherently exhibits a wide voltage range (from zero up to the peak value), the AC-side windings are electrically connected in series to allow a summation of the winding voltages $v_{\mathrm{p,a}i}$, $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$ (see **Fig. 5.2**). In this way, a three-phase AC port is formed by the series connection of the AC ports belonging to the three different phases.

In a three-phase AC grid, the absolute values of the phase voltages add up to an *approximately constant* sum over a grid cycle. Hence, an *approximately constant* sum of the half-cycle voltage-second products applied to the AC-side windings becomes available for control. The three-phase AC port can be therefore seen as one DC port with an *approximately constant* voltage. The term *approximately constant* in this context does not mean negligible ripple. In case of a symmetrical three-phase AC grid, the sum of the absolute phase voltages with an amplitude $\hat{V}_{\mathrm{abc}}$ corresponds to a six-pulse waveform with a constant average value of $\frac{6\hat{V}_{\mathrm{abc}}}{\pi}$ over the AC grid cycle exhibiting a $2(\frac{\pi}{3}-1)\,\% = 9.4\,\%$ peak-to-peak voltage ripple.

As discussed in the previous chapter in Section 4.1.2, a full-bridge and a T-type circuit exhibit the same amount of degrees of freedom in control. Nevertheless, when it comes to a qualitative comparison of the semiconductor losses, the full-bridge circuit performs better as long as the clamping interval is substantially small. Due to the series connection of the AC port windings, the length of the clamping intervals strongly depend on the instantaneous phase current/power and can therefore vary in a wide range.

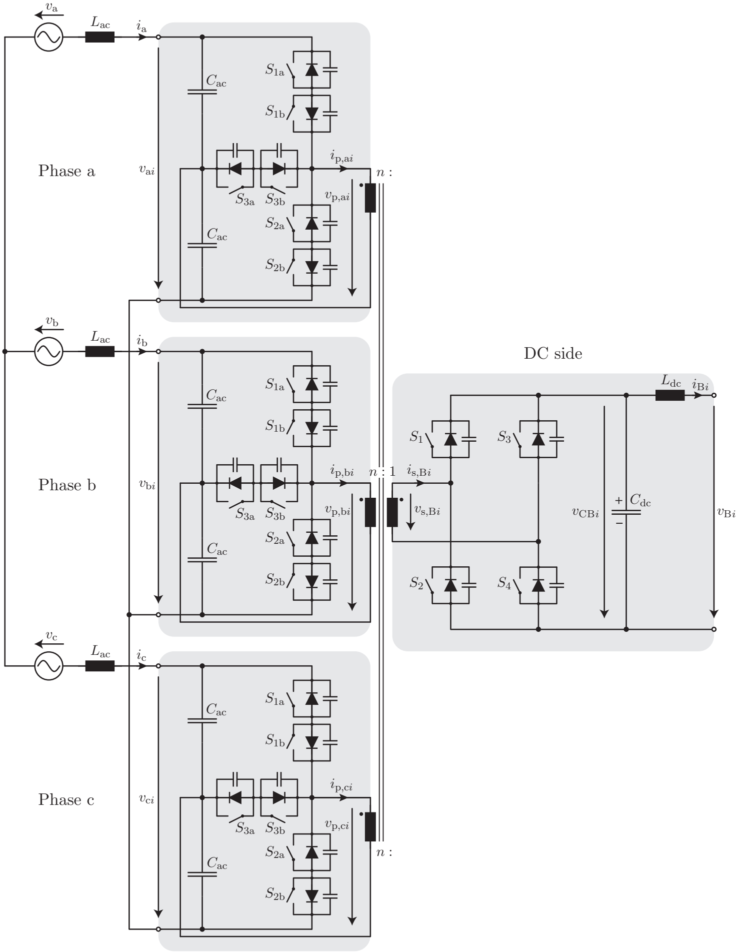

v_a
L_{ac}
i_a
C_{ac}
S_{1a}
S_{1b}
Phase a
v_{ai}
$i_{p,ai}$
$n:$
S_{3a}
S_{3b}
$v_{p,ai}$
S_{2a}
S_{2b}
v_b
i_b
Phase b
v_{bi}
$i_{p,bi}$
$n:1$
$i_{s,Bi}$
$v_{p,bi}$
$v_{s,Bi}$
DC side
L_{dc}
i_{Bi}
S_1
S_2
S_3
S_4
v_{CBi}
C_{dc}
v_{Bi}
v_c
i_c
Phase c
v_{ci}
$i_{p,ci}$
$v_{p,ci}$

Figure 5.2: AC-DC multi-port converter module applying grid-side T-type blocks with bidirectional switches, a battery-side full-bridge with unidirectional switches and a four-winding medium-frequency transformer providing the galvanic isolation.

Thus, the use of a T-type block at the AC side is advantageous since the conduction losses caused by the circulating current flowing through all ports (three AC and one DC port) can be reduced. This is due to the fact that the semiconductor devices of the clamping switch in a T-type block require only to be rated for half of the blocking voltage compared to the devices of the half-bridge. The application of semiconductor devices with lower voltage rating leads in turn to lower on-state resistance and finally to lower conduction losses.

5.2.2 Transformer arrangements

The formation of a three-phase AC port from three single-phase AC ports as described above requires the summation of the winding voltages $v_{\mathrm{p,a}i}$, $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$ through a suitable transformer arrangement. Then, for controlling the AC-DC multi-port module, an *approximately constant* sum of the half-cycle voltage-second products applied to the AC-side windings becomes available.

Electrically adding the winding voltages directly transforms to magnetically adding the winding fluxes through the transformer core. Thus, in general, there are two possibilities of transformer arrangements for the summation of the AC-side winding voltages: Firstly, the use of three two-winding transformers with independent magnetic cores where the AC-side winding voltages are added through an electric series connection of the DC-side windings. Secondly, the use of a four-winding transformer with a single magnetic core where the AC-side winding fluxes are added through a magnetic parallel connection of the AC-side windings.

Two-winding transformers

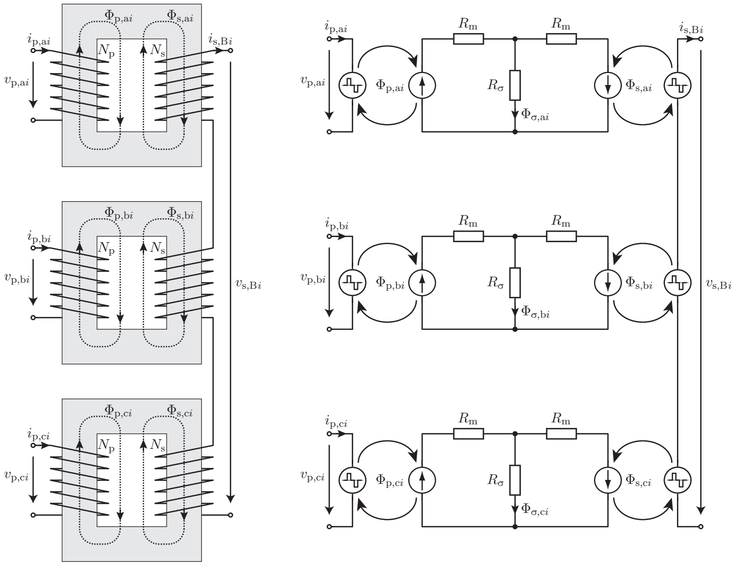
The first transformer arrangement applying three two-winding transformers with the DC-side windings electrically connected in series is shown in **Fig. 5.3**. Besides one possible assembly of the three transformers consisting of two C-cores with the windings on the right leg and the left leg, also the corresponding reluctance models are depicted. By applying MF square-wave voltages with clamping intervals to the transformer windings, the associated winding fluxes in the magnetic core are impressed. The generation of the winding fluxes through the applied voltages is modeled by flux sources in the reluctance model. The magnetic core is modeled by the reluctances R_m and the leakage layer/area by the reluctance R_σ (see **Fig. 5.3(b)**).

The impressed winding fluxes through the voltages $v_{\mathrm{p,a}i}$, $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$ at the AC side of the two-winding transformers can be written as

$$\Phi_{\mathrm{p,a}i}(t) = \Phi_{\mathrm{p,a}i}(0) + \frac{1}{N_\mathrm{p}} \int_0^t v_{\mathrm{p,a}i}(\tau)\ \mathrm{d}\tau, \tag{5.1}$$

$$\Phi_{\mathrm{p,b}i}(t) = \Phi_{\mathrm{p,b}i}(0) + \frac{1}{N_\mathrm{p}} \int_0^t v_{\mathrm{p,b}i}(\tau)\ \mathrm{d}\tau, \tag{5.2}$$

$$\Phi_{\mathrm{p,c}i}(t) = \Phi_{\mathrm{p,c}i}(0) + \frac{1}{N_\mathrm{p}} \int_0^t v_{\mathrm{p,c}i}(\tau)\ \mathrm{d}\tau. \tag{5.3}$$


$\Phi_{\mathrm{p,a}i}$
$\Phi_{\mathrm{s,a}i}$
$i_{\mathrm{p,a}i}$
$i_{\mathrm{s,B}i}$
N_p
N_s
$v_{\mathrm{p,a}i}$
$\Phi_{\mathrm{p,b}i}$
$\Phi_{\mathrm{s,b}i}$
$i_{\mathrm{p,b}i}$
$v_{\mathrm{p,b}i}$
$v_{\mathrm{s,B}i}$
$\Phi_{\mathrm{p,c}i}$
$\Phi_{\mathrm{s,c}i}$
$i_{\mathrm{p,c}i}$
$v_{\mathrm{p,c}i}$
R_m
R_σ
$\Phi_{\sigma,\mathrm{a}i}$
$\Phi_{\sigma,\mathrm{b}i}$
$\Phi_{\sigma,\mathrm{c}i}$

(a) (b)

Figure 5.3: Transformer arrangement consisting of three two-winding transformers whose secondary windings are connected in series for the use in the AC-DC multi-port module depicted in **Fig. 5.2**: (a) possible assembly of the transformer arrangement with voltage, current and winding flux directions and (b) the corresponding reluctance models including the couplings to the electric circuits. The applied voltages to the transformer windings are modeled by MF square-wave voltage sources with clamping intervals.

Assuming equal impedances of the DC-side windings of the two-winding transformers, the voltage $v_{\mathrm{s,B}i}$ is equally split between the windings, so that the impressed winding fluxes at the DC side are given by

$$\Phi_{\mathrm{s,a}i}(t) = \Phi_{\mathrm{s,a}i}(0) + \frac{1}{N_\mathrm{s}} \int_0^t \frac{1}{3} v_{\mathrm{s,B}i}(\tau)\ \mathrm{d}\tau, \tag{5.4}$$

$$\Phi_{\mathrm{s,b}i}(t) = \Phi_{\mathrm{s,b}i}(0) + \frac{1}{N_\mathrm{s}} \int_0^t \frac{1}{3} v_{\mathrm{s,B}i}(\tau)\ \mathrm{d}\tau, \tag{5.5}$$

$$\Phi_{\mathrm{s,c}i}(t) = \Phi_{\mathrm{s,c}i}(0) + \frac{1}{N_\mathrm{s}} \int_0^t \frac{1}{3} v_{\mathrm{s,B}i}(\tau)\ \mathrm{d}\tau. \tag{5.6}$$

The difference of the AC- and the DC-side impressed winding fluxes represents the leakage flux which is flowing through the leakage reluctance R_σ as shown in **Fig. 5.3(b)**. The resulting leakage fluxes in the three transformers are thus determined as

$$\Phi_{\sigma,\mathrm{a}i}(t) = \Phi_{\mathrm{p,a}i}(t) - \Phi_{\mathrm{s,a}i}(t), \tag{5.7}$$

$$\Phi_{\sigma,\mathrm{b}i}(t) = \Phi_{\mathrm{p,b}i}(t) - \Phi_{\mathrm{s,b}i}(t), \tag{5.8}$$

$$\Phi_{\sigma,\mathrm{c}i}(t) = \Phi_{\mathrm{p,c}i}(t) - \Phi_{\mathrm{s,c}i}(t). \tag{5.9}$$

From the reluctance models depicted in **Fig. 5.3(b)**, the AC-side referred leakage inductance of the three two-winding transformers can be calculated as

$$L_{\sigma,\mathrm{a}i} = L_{\sigma,\mathrm{b}i} = L_{\sigma,\mathrm{c}i} = \frac{N_\mathrm{p}^2}{R_\sigma}. \tag{5.10}$$

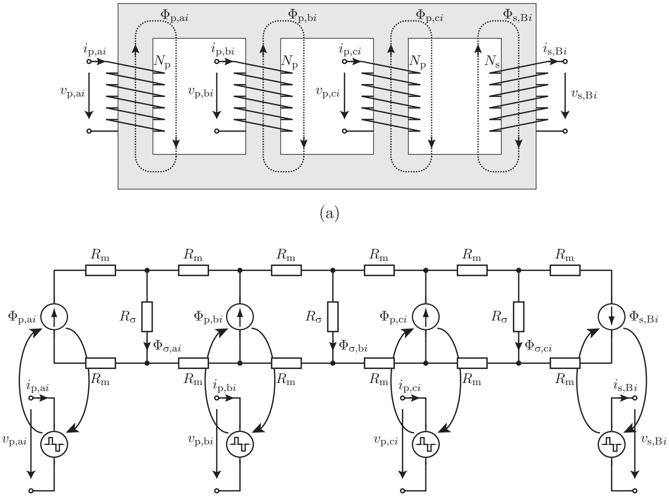
The AC-side referred total leakage inductance relevant for controlling the AC-DC multi-port module is then given as the series connection of the leakage inductances of the single transformers

$$L_\sigma = L_{\sigma,\mathrm{a}i} + L_{\sigma,\mathrm{b}i} + L_{\sigma,\mathrm{c}i} = 3\frac{N_\mathrm{p}^2}{R_\sigma}. \tag{5.11}$$

This is due to the fact that all (AC- and DC-side) ports are electrically connected in series through the utilized transformer arrangement.

Four-winding transformer

The second transformer arrangement applying one four-winding transformer with the AC-side windings magnetically connected in parallel is shown in **Fig. 5.4**. A possible assembly consists of six C-cores with a winding on each of the four legs in parallel (see **Fig. 5.4(a)**). The corresponding reluctance model is depicted in **Fig. 5.4(b)** where the impressed winding fluxes through the applied winding voltages are modeled as flux sources. The magnetic core is modeled by the reluctances R_m and the leakage layer/area by the reluctances R_σ.



$\Phi_{\mathrm{p,a}i}$
$\Phi_{\mathrm{p,b}i}$
$\Phi_{\mathrm{p,c}i}$
$\Phi_{\mathrm{s,B}i}$
$i_{\mathrm{p,a}i}$
$i_{\mathrm{p,b}i}$
$i_{\mathrm{p,c}i}$
$i_{\mathrm{s,B}i}$
N_p
N_p
N_p
N_s
$v_{\mathrm{p,a}i}$
$v_{\mathrm{p,b}i}$
$v_{\mathrm{p,c}i}$
$v_{\mathrm{s,B}i}$
R_m
R_σ
$\Phi_{\sigma,\mathrm{a}i}$
$\Phi_{\sigma,\mathrm{b}i}$
$\Phi_{\sigma,\mathrm{c}i}$

(a)

(b)

Figure 5.4: Transformer arrangement consisting of a four-winding transformer where the windings are magnetically connected in parallel for the use in the AC-DC multi-port module depicted in **Fig. 5.2**: (a) possible assembly of the transformer arrangement with voltage, current and winding flux directions and (b) the corresponding reluctance model including the couplings to the electric circuits. The applied voltages to the transformer windings are modeled by MF square-wave voltage sources with clamping intervals.

The impressed winding fluxes through the voltages $v_{\mathrm{p,a}i}$, $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$ at the AC-side windings of the four-winding transformer do not differ from the two-winding transformer case and are given by (5.1), (5.2) and (5.3). At the DC side, the voltage $v_{\mathrm{s,B}i}$ is applied to one single DC winding such that the DC-side flux

$$\Phi_{\mathrm{s,B}i}(t) = \Phi_{\mathrm{s,B}i}(0) + \frac{1}{N_{\mathrm{s}}} \int_0^t v_{\mathrm{s,B}i}(\tau)\ \mathrm{d}\tau \tag{5.12}$$

is impressed.

The difference of the AC-side winding flux sum and the DC-side winding flux represents the total leakage flux which is flowing through the leakage reluctances R_σ as shown in **Fig. 5.4(b)**. The resulting leakage fluxes in the three leakage layers/areas modeled in the reluctance model are calculated as

$$\Phi_{\sigma,\mathrm{a}i}(t) = \alpha_1\Phi_{\mathrm{p,a}i}(t) + \alpha_2\Phi_{\mathrm{p,b}i}(t) + \alpha_3\Phi_{\mathrm{p,c}i}(t) - \alpha_4\Phi_{\mathrm{s,B}i}(t), \tag{5.13}$$

$$\Phi_{\sigma,\mathrm{b}i}(t) = \beta_1\Phi_{\mathrm{p,a}i}(t) + \beta_2\Phi_{\mathrm{p,b}i}(t) + \beta_3\Phi_{\mathrm{p,c}i}(t) - \beta_4\Phi_{\mathrm{s,B}i}(t), \tag{5.14}$$

$$\Phi_{\sigma,\mathrm{c}i}(t) = \gamma_1\Phi_{\mathrm{p,a}i}(t) + \gamma_2\Phi_{\mathrm{p,b}i}(t) + \gamma_3\Phi_{\mathrm{p,c}i}(t) - \gamma_4\Phi_{\mathrm{s,B}i}(t) \tag{5.15}$$

with the coefficients

$$\alpha_1 = \gamma_4 = \frac{16R_{\mathrm{m}}^2 + 12R_{\mathrm{m}}R_\sigma + R_\sigma^2}{(4R_{\mathrm{m}} + 3R_\sigma)(4R_{\mathrm{m}} + R_\sigma)}, \tag{5.16}$$

$$\alpha_2 = \gamma_3 = \frac{8R_{\mathrm{m}}^2 + 8R_{\mathrm{m}}R_\sigma + R_\sigma^2}{(4R_{\mathrm{m}} + 3R_\sigma)(4R_{\mathrm{m}} + R_\sigma)}, \tag{5.17}$$

$$\alpha_3 = \gamma_2 = \frac{R_\sigma(2R_{\mathrm{m}} + R_\sigma)}{(4R_{\mathrm{m}} + 3R_\sigma)(4R_{\mathrm{m}} + R_\sigma)}, \tag{5.18}$$

$$\alpha_4 = \gamma_1 = \frac{R_\sigma^2}{(4R_{\mathrm{m}} + 3R_\sigma)(4R_{\mathrm{m}} + R_\sigma)}, \tag{5.19}$$

$$\beta_1 = \beta_4 = \frac{R_\sigma}{4R_{\mathrm{m}} + 3R_\sigma}, \tag{5.20}$$

$$\beta_2 = \beta_3 = \frac{2R_{\mathrm{m}} + R_\sigma}{4R_{\mathrm{m}} + 3R_\sigma}. \tag{5.21}$$

The total leakage flux is then given by adding the leakage fluxes $\Phi_{\sigma,\mathrm{a}i}$, $\Phi_{\sigma,\mathrm{b}i}$ and $\Phi_{\sigma,\mathrm{c}i}$ which leads to

$$\Phi_{\sigma}(t) = \Phi_{\mathrm{p,a}i}(t) + \Phi_{\mathrm{p,b}i}(t) + \Phi_{\mathrm{p,c}i}(t) - \Phi_{\mathrm{s,B}i}(t). \tag{5.22}$$

From the reluctance model depicted in **Fig. 5.4(b)**, the AC-side referred total leakage inductance of the four-winding transformer can be calculated by the magnetic parallel connection of the leakage reluctances R_{σ} as

$$L_{\sigma} = 3\frac{N_{\mathrm{p}}^{2}}{R_{\sigma}}. \tag{5.23}$$

5.3 Operating principle

As in the case of the cascaded AC-DC DAB converter, a grid-side equivalent circuit of the cascaded AC-DC multi-port converter can be drawn which is shown in **Fig. 5.5**. The AC-DC modules are modeled by their capacitive voltage ports consisting of the series connection of two filter capacitors C_{ac} and the controlled current sources $i_{\mathrm{ma}i}$, $i_{\mathrm{mb}i}$, $i_{\mathrm{mc}i}$ exemplarily for the module $i \in \{1, 2, ..., n\}$. The AC-DC multi-port module is modeled by the total transformer leakage inductance L_{σ} of the transformer arrangement (see **Fig. 5.3** and **Fig. 5.4**) and the AC- and DC-side applied MF voltages $v_{\mathrm{p,a}i}$, $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$, $v'_{\mathrm{s,B}i}$ (AC-side referred) at the transformer windings. The transformer magnetizing inductance(s) L_{m} is/are assumed to be relatively large, so that magnetizing currents can be neglected for the analysis of the operating principle.

5.3.1 Module level

Like the three-port DC-DC converters discussed in [109–111], the proposed AC-DC multi-port module depicted in **Fig. 5.2** is operated by phase shift control where the MF square-wave voltages applied to the transformer windings exhibit a phase displacement with regard to each other to control the power flow at the ports. The total leakage inductance L_{σ} of the transformer arrangement acts as decoupling and energy transfer element between the ports. **Fig. 5.5** shows the equivalent circuit of the multi-port module where the AC-side T-type blocks and the DC-side full-bridge are modeled as controlled current sources coupled to MF square-wave voltage sources with clamping intervals.

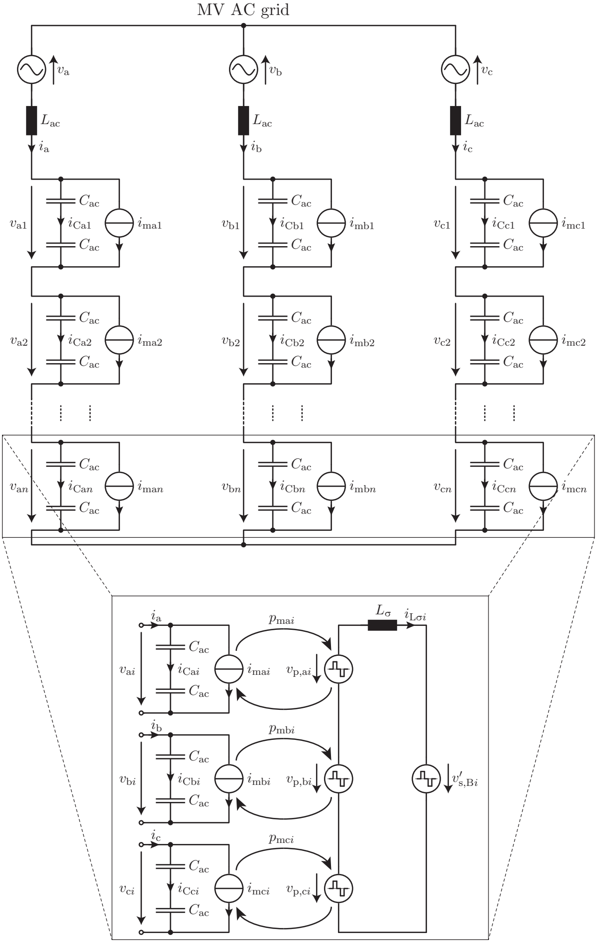

MV AC grid
v_{a}
v_{b}
v_{c}
L_{ac}
i_{a}
i_{b}
i_{c}
C_{ac}
v_{a1}
i_{Ca1}
i_{ma1}
v_{b1}
i_{Cb1}
i_{mb1}
v_{c1}
i_{Cc1}
i_{mc1}
v_{a2}
i_{Ca2}
i_{ma2}
v_{b2}
i_{Cb2}
i_{mb2}
v_{c2}
i_{Cc2}
i_{mc2}
$v_{\mathrm{a}n}$
$i_{\mathrm{Ca}n}$
$i_{\mathrm{ma}n}$
$v_{\mathrm{b}n}$
$i_{\mathrm{Cb}n}$
$i_{\mathrm{mb}n}$
$v_{\mathrm{c}n}$
$i_{\mathrm{Cc}n}$
$i_{\mathrm{mc}n}$
L_σ
$i_{\mathrm{L}\sigma i}$
$p_{\mathrm{ma}i}$
$v_{\mathrm{a}i}$
$i_{\mathrm{Ca}i}$
$i_{\mathrm{ma}i}$
$v_{\mathrm{p,a}i}$
$p_{\mathrm{mb}i}$
$v_{\mathrm{b}i}$
$i_{\mathrm{Cb}i}$
$i_{\mathrm{mb}i}$
$v_{\mathrm{p,b}i}$
$v'_{\mathrm{s,B}i}$
$p_{\mathrm{mc}i}$
$v_{\mathrm{c}i}$
$i_{\mathrm{Cc}i}$
$i_{\mathrm{mc}i}$
$v_{\mathrm{p,c}i}$

Figure 5.5: Grid-side equivalent circuit of the cascaded AC-DC multi-port converter shown in **Fig. 5.1**. The modules are modeled with their capacitive voltage ports consisting of the series connection of two filter capacitors C_{ac} and the controlled current sources $i_{\mathrm{ma}i}$, $i_{\mathrm{mb}i}$, $i_{\mathrm{mc}i}$. By adjusting the power transfer at the AC ports of a multi-port module, the current sources are controlled in order to regulate the AC-side module voltages as well as the grid currents. The multi-port module is modeled by the total transformer leakage inductance L_σ and the AC- and DC-side applied MF voltages $v_{\mathrm{p,a}i}$, $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$, $v'_{\mathrm{s,B}i}$ (AC-side referred) at the transformer windings.

With the modulation schemes described in Section 5.5, the power transfer from the AC ports to the DC port is controlled. The power flows $p_{\mathrm{ma}i}$, $p_{\mathrm{mb}i}$, $p_{\mathrm{mc}i}$ represent the couplings of the grid-side current sources $i_{\mathrm{ma}i}$, $i_{\mathrm{mb}i}$, $i_{\mathrm{mc}i}$ and the corresponding MF voltage sources $v_{\mathrm{p,a}i}$, $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$ (represented by the two arrows for each coupling shown in **Fig. 5.5**) and are given by

$$p_{\mathrm{ma}i} = v_{\mathrm{a}i} i_{\mathrm{ma}i} = v_{\mathrm{a}i} \left(i_{\mathrm{a}} - i_{\mathrm{Ca}i} \right), \tag{5.24}$$

$$p_{\mathrm{mb}i} = v_{\mathrm{b}i} i_{\mathrm{mb}i} = v_{\mathrm{b}i} \left(i_{\mathrm{b}} - i_{\mathrm{Cb}i} \right), \tag{5.25}$$

$$p_{\mathrm{mc}i} = v_{\mathrm{c}i} i_{\mathrm{mc}i} = v_{\mathrm{c}i} \left(i_{\mathrm{c}} - i_{\mathrm{Cc}i} \right). \tag{5.26}$$

By adjusting the power flows through the modulation scheme, the current sources $i_{\mathrm{ma}i}$, $i_{\mathrm{mb}i}$, $i_{\mathrm{mc}i}$ are controlled in order to regulate the AC-side module voltages $v_{\mathrm{a}i}$, $v_{\mathrm{b}i}$, $v_{\mathrm{c}i}$ and hence the grid currents i_{a}, i_{b}, i_{c}.

During one half-cycle of the grid-side AC voltage, two of the grid-side semiconductor devices in the bidirectional switches of the AC ports are constantly turned on. These are $S_{1\mathrm{b}}$ and $S_{2\mathrm{b}}$ for the positive and $S_{1\mathrm{a}}$ and $S_{2\mathrm{a}}$ for the negative half-wave (see **Fig. 5.2**).

5.3.2 System level

The grid current in terms of amplitude and phase is controlled by the AC-side module voltages in a phase string by applying the corresponding voltage across the grid filter inductor L_{ac}. For the battery energy storage system depicted in **Fig. 5.1**, purely active power in charging and discharging operation is considered with a power factor (PF) near unity. Moreover, since the module voltage ports in the same phase string are connected in series, the power distribution among the module ports can only be set by controlling the grid-side voltages of the modules as the module currents are equal.

By increasing the voltage of a module port, the voltage of another module port or the voltages of other module ports in the same phase string have to be reduced, so that the voltage sum of all module ports is not changed. In this way, only the power distribution among the module ports is affected, but not the overall power flow between the grid and the batteries. The upper limit of the module power is basically given by the blocking voltage of the applied semiconductor devices.

At the grid side, each module can be simply represented by a voltage source (capacitive voltage port controlled by a current source as depicted in **Fig. 5.5**) where the voltage is controlled by the power transfer between the grid-side filter capacitors C_{ac} and the battery. To increase the module port power, first the module port voltage $v_{\mathrm{a}i}$, $v_{\mathrm{b}i}$ or $v_{\mathrm{c}i}$ has to be increased which is done by reducing the power transfer to the battery. As soon as the module voltage rises, the power transfer can be increased again to reach its reference value. A corresponding voltage controller was previously described in Section 4.4.5 for the cascaded AC-DC DAB converter.

5.4 Modeling of power flows

For designing and controlling a multi-port converter system, the mathematical description of the power flows depending on the control variables is essential. The optimization procedure to derive optimal control variables as shown later in Section 5.5.2 requires the calculation of the power flows $p_{\mathrm{ma}i}$, $p_{\mathrm{mb}i}$, $p_{\mathrm{mc}i}$ (see **Fig. 5.5**) for evaluating the power equality constraints.

The well-known approach uses piecewise linear equations for the transformer leakage inductance current where several mathematical cases depending on the phase shifts and the clamping intervals have to be distinguished. Due to the mathematical complexity, especially for high port numbers in multi-port converters, the following analysis uses basic superposition principles to find general analytical formulas for the power flows. With this approach, there is no need for a mathematical distinction of cases.

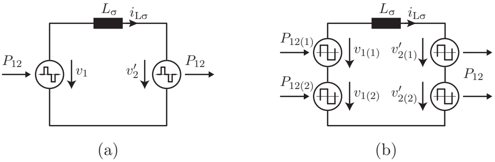
The mathematical analysis of the power flows at the AC ports and the DC port is based on the AC-side referred equivalent circuit of the multi-port converter topology shown in **Fig. 5.5**. The T-type circuits and the full-bridge are modeled by MF square-wave voltage sources $v_{\mathrm{p,a}i}$, $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$, $v'_{\mathrm{s,B}i}$ with clamping intervals. For the analytical description of the power flow at an AC port, first the power flow between two ports applying square-wave voltages with clamping intervals is modeled (see **Fig. 5.6(a)**).

5.4.1 Power flow between two ports

The power flow over one switching cycle $T_\mathrm{s} = \frac{2\pi}{\omega_\mathrm{s}}$ between two ports (from a first port 1 to a second port 2) applying square-wave voltages with clamping intervals as shown in **Fig. 5.6(a)** is based on the well-known power flow equation [116] (power from a primary port p to a secondary port s)

$$P_\mathrm{ps} = \frac{V_\mathrm{p} n V_\mathrm{s}}{\omega_\mathrm{s} L_\sigma} (\phi_\mathrm{p} - \phi_\mathrm{s}) \left(1 - \frac{|\phi_\mathrm{p} - \phi_\mathrm{s}|}{\pi}\right). \tag{5.27}$$

There, two square-wave voltages with 50 % duty cycles, amplitudes V_p, V_s and phases $\phi_\mathrm{p}, \phi_\mathrm{s} \in \{-\pi, \pi\}$ are applied across the windings of a two-winding transformer with the primary referred leakage inductance L_σ, a negligible large magnetizing inductance and the turns ratio $n = \frac{N_\mathrm{p}}{N_\mathrm{s}}$. The phase angles are measured against a given reference, a positive angle defines a leading signal and a negative angle a lagging signal with respect to the reference.



(a) (b)

Figure 5.6: Simplified circuit of a two-port converter applying square-wave voltages with clamping intervals (a) and the equivalent four-port circuit applying square-wave voltages without clamping intervals at the ports (b).

The two-port circuit with clamping intervals drawn in **Fig. 5.6(a)** can be modeled by an equivalent four-port circuit which is shown in **Fig. 5.6(b)** where only square-wave voltages without clamping intervals and duty cycles of 50 % occur. This is done by splitting up the voltage v_1 with clamping interval into a sum $v_{1(1)} + v_{1(2)}$ of two voltages with 50 % duty cycles, no clamping intervals and a phase shift of $2\delta_1$ against each other as depicted in **Fig. 5.7**. Analogously, this is done for the voltage v_2.

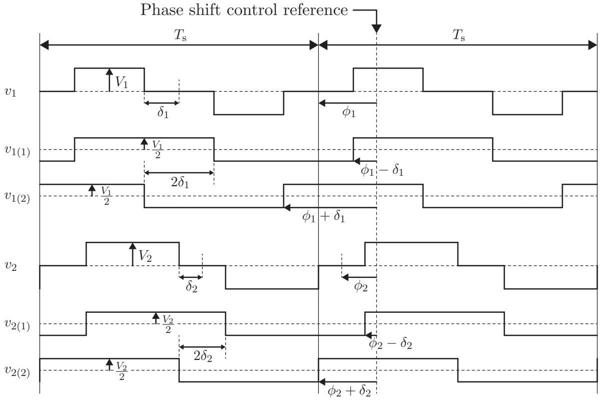

Phase shift control reference
T_s
T_s
v_1
V_1
δ_1
ϕ_1
$v_{1(1)}$
$\frac{V_1}{2}$
$2\delta_1$
$\phi_1 - \delta_1$
$v_{1(2)}$
$\frac{V_1}{2}$
$\phi_1 + \delta_1$
v_2
V_2
δ_2
ϕ_2
$v_{2(1)}$
$\frac{V_2}{2}$
$2\delta_2$
$\phi_2 - \delta_2$
$v_{2(2)}$
$\frac{V_2}{2}$
$\phi_2 + \delta_2$

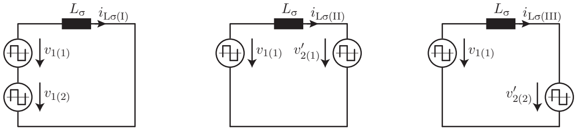
Figure 5.7: Square-wave voltages v_1, v_2 with clamping intervals $2\delta_1$, $2\delta_2$ and the underlying square-wave voltages $v_{1(1)}$, $v_{1(2)}$, $v_{2(1)}$, $v_{2(2)}$ without clamping intervals and duty cycles 50 % which add up to v_1 and v_2 respectively.

The power transferred from port 1 to port 2 is then given by

$$P_{12} = \underbrace{\frac{1}{T_\mathrm{s}} \int_0^{T_\mathrm{s}} v_{1(1)} i_{\mathrm{L}\sigma} \,\mathrm{d}\tau}_{P_{12(1)}} + \underbrace{\frac{1}{T_\mathrm{s}} \int_0^{T_\mathrm{s}} v_{1(2)} i_{\mathrm{L}\sigma} \,\mathrm{d}\tau}_{P_{12(2)}} \tag{5.28}$$

with the two power shares $P_{12(1)}$, $P_{12(2)}$ of the voltage sources $v_{1(1)}$, $v_{1(2)}$ (see **Fig. 5.6(b)**).

Since the voltage-second product of each source in **Fig. 5.6(b)** over a switching cycle T_s is zero, a single source only delivers reactive power to the leakage inductance L_σ. Therefore, the calculation of the power share $P_{12(1)}$ can be done by splitting up the leakage inductance current $i_{\mathrm{L}\sigma}$ into three parts $i_{\mathrm{L}\sigma(\mathrm{I})}$, $i_{\mathrm{L}\sigma(\mathrm{II})}$, $i_{\mathrm{L}\sigma(\mathrm{III})}$ which are obtained by applying the superposition principle as shown in **Fig. 5.8** by selectively short-circuiting voltage sources. In this way, the active power exchange of the source $v_{1(1)}$ with the sources $v_{1(2)}$, $v'_{2(1)}$, $v'_{2(2)}$ is described. Although the source $v_{1(1)}$ contributes three times to the current $i_{\mathrm{L}\sigma}$ by applying the proposed superposition, this current part cancels out in the active power calculation, as it only describes reactive power delivered from $v_{1(1)}$ to L_σ. Compared to conventional superposition, the current driven by $v_{1(1)}$ is increased by a factor of 3, nevertheless it does not contribute to the active power calculation.


L_σ
$i_{\mathrm{L}\sigma(\mathrm{I})}$
$v_{1(1)}$
$v_{1(2)}$
L_σ
$i_{\mathrm{L}\sigma(\mathrm{II})}$
$v_{1(1)}$
$v'_{2(1)}$
L_σ
$i_{\mathrm{L}\sigma(\mathrm{III})}$
$v_{1(1)}$
$v'_{2(2)}$

(a) (b) (c)

Figure 5.8: Leakage inductance current obtained for the power calculation by applying the superposition principle with three parts (a), (b), (c) by selectively short-circuiting voltage sources: $i_{\mathrm{L}\sigma} = i_{\mathrm{L}\sigma(\mathrm{I})} + i_{\mathrm{L}\sigma(\mathrm{II})} + i_{\mathrm{L}\sigma(\mathrm{III})}$.

The power share $P_{12(1)}$ in (5.28) can then be written as

$$\begin{aligned} P_{12(1)} = & \underbrace{\frac{1}{T_\mathrm{s}} \int_0^{T_\mathrm{s}} v_{1(1)} i_{\mathrm{L}\sigma(\mathrm{I})} \, \mathrm{d}\tau}_{P_{12(1)(\mathrm{I})}} + \underbrace{\frac{1}{T_\mathrm{s}} \int_0^{T_\mathrm{s}} v_{1(1)} i_{\mathrm{L}\sigma(\mathrm{II})} \, \mathrm{d}\tau}_{P_{12(1)(\mathrm{II})}} \\ & + \underbrace{\frac{1}{T_\mathrm{s}} \int_0^{T_\mathrm{s}} v_{1(1)} i_{\mathrm{L}\sigma(\mathrm{III})} \, \mathrm{d}\tau}_{P_{12(1)(\mathrm{III})}} . \end{aligned} \tag{5.29}$$

Analogously, the second power share $P_{12(2)}$ is described. From **Fig. 5.8** and (5.29) it is concluded, that the power shares $P_{12(1)(\mathrm{I})}$, $P_{12(1)(\mathrm{II})}$, $P_{12(1)(\mathrm{III})}$ are given by (5.27). This is also the case for the power shares $P_{12(2)(\mathrm{I})}$, $P_{12(2)(\mathrm{II})}$, $P_{12(2)(\mathrm{III})}$. By summing up all the power shares, the resulting power transferred per switching cycle from port 1 to port 2 applying square-wave voltages v_1, v_2 with clamping intervals $2\delta_1$, $2\delta_2$ and phases ϕ_1, ϕ_2 as shown in **Fig. 5.7** is thus given as

$$\begin{aligned} P_{12} = \frac{V_1 n V_2}{4 \omega_\mathrm{s} L_\sigma} \Bigg[& ((\phi_1 - \delta_1) - (\phi_2 - \delta_2)) \left(1 - \frac{|(\phi_1 - \delta_1) - (\phi_2 - \delta_2)|}{\pi} \right) \\ & + ((\phi_1 - \delta_1) - (\phi_2 + \delta_2)) \left(1 - \frac{|(\phi_1 - \delta_1) - (\phi_2 + \delta_2)|}{\pi} \right) \end{aligned}$$

$$+\left((\phi_1+\delta_1)-(\phi_2-\delta_2)\right)\left(1-\frac{|(\phi_1+\delta_1)-(\phi_2-\delta_2)|}{\pi}\right)$$
$$+\left((\phi_1+\delta_1)-(\phi_2+\delta_2)\right)\left(1-\frac{|(\phi_1+\delta_1)-(\phi_2+\delta_2)|}{\pi}\right)\Bigg]. \tag{5.30}$$

This analytical power flow equation represents the basis for modeling the power flows at the AC ports as functions of the control variables in the three-phase AC-DC multi-port converter.

5.4.2 Power flow at AC ports

With the general power flow equation (5.30), in a next step, the analytical formulas for the power flows at the AC ports are derived. This is exemplarily done for phase a. The same derivation applies to the phases b and c. Looking at **Fig. 5.5**, the previously mentioned superposition principle is also applicable. For phase a, the voltage source $v_{\mathrm{p,a}i}$ exchanges power with all the other sources $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$, $v'_{\mathrm{s,B}i}$ which leads to the power flow

$$p_{\mathrm{ma}i} = \underbrace{\frac{1}{T_\mathrm{s}}\int_0^{T_\mathrm{s}} v_{\mathrm{p,a}i}\, i_{\mathrm{L}\sigma i(1)}\,\mathrm{d}\tau}_{p_{\mathrm{ma}i(1)}} + \underbrace{\frac{1}{T_\mathrm{s}}\int_0^{T_\mathrm{s}} v_{\mathrm{p,a}i}\, i_{\mathrm{L}\sigma i(2)}\,\mathrm{d}\tau}_{p_{\mathrm{ma}i(2)}}$$
$$+\underbrace{\frac{1}{T_\mathrm{s}}\int_0^{T_\mathrm{s}} v_{\mathrm{p,a}i}\, i_{\mathrm{L}\sigma i(3)}\,\mathrm{d}\tau}_{p_{\mathrm{ma}i(3)}} \tag{5.31}$$

from the AC port a to all other ports. The leakage inductance current is split up into three parts $i_{\mathrm{L}\sigma i(1)}$, $i_{\mathrm{L}\sigma i(2)}$, $i_{\mathrm{L}\sigma i(3)}$. The power shares are then formulated by means of (5.30) and given by

$$p_{\mathrm{ma}i(1)} = P_{12}\Bigg(V_1 = \frac{v_{\mathrm{a}i}}{2}, nV_2 = -\frac{v_{\mathrm{b}i}}{2},$$
$$\delta_1 = \delta_{\mathrm{a}i}, \phi_1 = \phi_{\mathrm{a}i}, \delta_2 = \delta_{\mathrm{b}i}, \phi_2 = \phi_{\mathrm{b}i}\Bigg), \tag{5.32}$$

$$p_{\mathrm{ma}i(2)} = P_{12}\Bigg(V_1 = \frac{v_{\mathrm{a}i}}{2}, nV_2 = -\frac{v_{\mathrm{c}i}}{2}, \\ \delta_1 = \delta_{\mathrm{a}i}, \phi_1 = \phi_{\mathrm{a}i}, \delta_2 = \delta_{\mathrm{c}i}, \phi_2 = \phi_{\mathrm{c}i}\Bigg), \tag{5.33}$$

$$p_{\mathrm{ma}i(3)} = P_{12}\Bigg(V_1 = \frac{v_{\mathrm{a}i}}{2}, V_2 = v_{\mathrm{B}i}, \\ \delta_1 = \delta_{\mathrm{a}i}, \phi_1 = \phi_{\mathrm{a}i}, \delta_2 = \delta_{\mathrm{B}i}, \phi_2 = \phi_{\mathrm{B}i}\Bigg). \tag{5.34}$$

The equations for the power flows $p_{\mathrm{ma}i}$, $p_{\mathrm{mb}i}$, $p_{\mathrm{mc}i}$ are used later in Section 5.5.2 in an optimization procedure for numerically deriving optimal control variables.

5.5 Module modulation schemes

Like DAB converters, the presented multi-port converter module depicted in **Fig. 5.2** is operated by actively applying square-wave voltages with clamping interval (zero voltage interval) across the windings of the two-winding transformers or the four-winding transformer respectively. The winding voltages can be modeled as MF voltage sources which are decoupled by the total leakage inductance of the transformer arrangement (see equivalent circuit of a multi-port module in **Fig. 5.5**). By adjusting the phase shifts between the square-wave voltages as well as the length of the clamping intervals, the transformer leakage inductance current can be shaped in order to control the power flows at the AC ports and the DC port and additionally allow beneficial conditions for soft-switching of the semiconductor devices.

Similar to Section 4.3, for the theoretical analysis of the modulation schemes of a multi-port module, the following assumptions are made:

- The magnetizing current(s) is/are negligible small (means large magnetizing inductance(s) L_{m}),
- the capacitors C_{ac}, C_{dc} are large enough so that the amplitudes of the generated square-wave voltages can be considered constant during one switching cycle,
- the switching frequency is well above the resonant frequency of the resonant tank formed by C_{ac}, C_{dc} and L_σ,

- the commutation intervals are negligible small in comparison to the switching cycle,
- the transformer turns ratio guarantees that the module is always operated in boost mode when the DC voltage is referred to the AC side.

Based on these, the transformer leakage inductance current is approximated by piecewise linear equations with no DC offset since the square-wave voltages applied to the transformer windings exhibit a zero voltage-second product over a switching cycle. This also guarantees that no DC flux appears in the transformer core(s).

Due to the electric series connection of the ports, the transformer leakage inductance current $i_{\mathrm{L}\sigma i}$ flows through all of the equivalent voltage sources $v_{\mathrm{p,a}i}$, $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$, $v'_{\mathrm{s,B}i}$ as shown in **Fig. 5.5** and hence defines, together with the port voltages, the instantaneous power which has to be delivered to or drawn from the corresponding port. The coupling of the AC ports and the DC port leads to a certain degree of complexity in deriving suitable modulation schemes.

In the following, two approaches are presented: In a first step, a modulation scheme based only on a fundamental wave model is developed to achieve sinusoidal AC port currents with phase displacements of 120° without considering soft-switching conditions (suitable for the use with IGBTs). In a second step, based on the above derived general power flow equations at the ports, optimal control variables are numerically determined while considering also soft-switching conditions in terms of ZVS in order to use MOSFETs.

5.5.1 Fundamental phasor modulation

A simple modulation scheme for the AC-DC multi-port module depicted in **Fig. 5.2** can be developed by only considering the fundamental waves of the MF square-wave voltages applied to the transformer windings as for instance shown in [109] for a three-port DC-DC converter. The MF square-wave voltage sources $v_{\mathrm{p,a}i}$, $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$, $v'_{\mathrm{s,B}i}$ depicted in **Fig. 5.9(b)** are reduced to their fundamental component in order to derive analytical solutions for the control variables in terms of phase shifts and clamping intervals. The phase angles $\phi_{\mathrm{a}i}$, $\phi_{\mathrm{b}i}$, $\phi_{\mathrm{c}i}$ of the AC-side applied square-wave voltages in relation to the DC-side applied square-wave voltage as well as the AC-side clamping interval

$2\delta_{\mathrm{abc}i}$ and the DC-side clamping interval $2\delta_{\mathrm{B}i}$ are introduced as unknowns as can be seen in **Fig. 5.10**. The introduction of a common clamping interval at the AC side leads to a symmetrical three-phase current system as shown later.

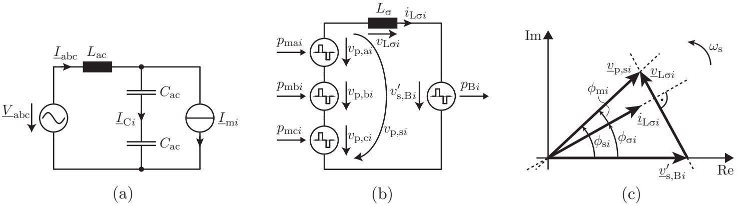

$\underline{I}_{\mathrm{abc}}$
L_{ac}
C_{ac}
$\underline{V}_{\mathrm{abc}}$
$\underline{I}_{\mathrm{C}i}$
$\underline{I}_{\mathrm{m}i}$
C_{ac}
(a)
L_σ
$i_{\mathrm{L}\sigma i}$
$p_{\mathrm{ma}i}$
$v_{\mathrm{p,a}i}$
$v_{\mathrm{L}\sigma i}$
$p_{\mathrm{mb}i}$
$v_{\mathrm{p,b}i}$
$v'_{\mathrm{s,B}i}$
$p_{\mathrm{B}i}$
$p_{\mathrm{mc}i}$
$v_{\mathrm{p,c}i}$
$v_{\mathrm{p,s}i}$
(b)
Im
ω_{s}
$\underline{v}_{\mathrm{p,s}i}$
$\underline{v}_{\mathrm{L}\sigma i}$
$\phi_{\mathrm{m}i}$
$\underline{i}_{\mathrm{L}\sigma i}$
$\phi_{\mathrm{s}i}$
$\phi_{\sigma i}$
$\underline{v}'_{\mathrm{s,B}i}$
Re
(c)

Figure 5.9: Single-phase grid-side equivalent circuit of the multi-port module in (a) where the current source $\underline{I}_{\mathrm{m}i}$ is controlled such that the desired phase current $\underline{I}_{\mathrm{abc}}$ results. (b) depicts the equivalent circuit of the multi-port module for describing the fundamental phasor modulation scheme with the transformer winding voltages modeled as MF voltage sources $v_{\mathrm{p,a}i}$, $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$, $v'_{\mathrm{s,B}i}$ and the AC-side referred total leakage inductance L_σ. Additionally, (c) shows a general phasor diagram for the MF fundamental model in case of capacitive AC port currents ($\phi_{\mathrm{m}i} > 0$).

Medium-frequency (MF) square-wave voltage summation

The transformer arrangements depicted in **Fig. 5.3** and **Fig. 5.4** sum up the MF square-wave voltages $v_{\mathrm{p,a}i}$, $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$ which are generated by the AC-side T-type circuits shown in **Fig. 5.2**. The phase displacements in relation to the DC-side applied voltage $v_{\mathrm{s,B}i}$, which is chosen as the phase shift control reference, are described by the angles $\phi_{\mathrm{a}i}$, $\phi_{\mathrm{b}i}$, $\phi_{\mathrm{c}i}$ as depicted in **Fig. 5.10**. There, also the resulting voltage sum $v_{\mathrm{p,s}i} = v_{\mathrm{p,a}i} + v_{\mathrm{p,b}i} + v_{\mathrm{p,c}i}$ and the transformer leakage inductance current $i_{\mathrm{L}\sigma i}$ referred to the AC side over two switching periods T_{s} are drawn.

The adaptation of the phase angles $\phi_{\mathrm{a}i}$, $\phi_{\mathrm{b}i}$, $\phi_{\mathrm{c}i}$ within the period of the AC grid enables keeping the half-cycle voltage-second product (shaded area in **Fig. 5.10**) and therefore also the amplitude of the MF fundamental wave of the voltage sum $v_{\mathrm{p,s}i}$ at an approximately constant value.

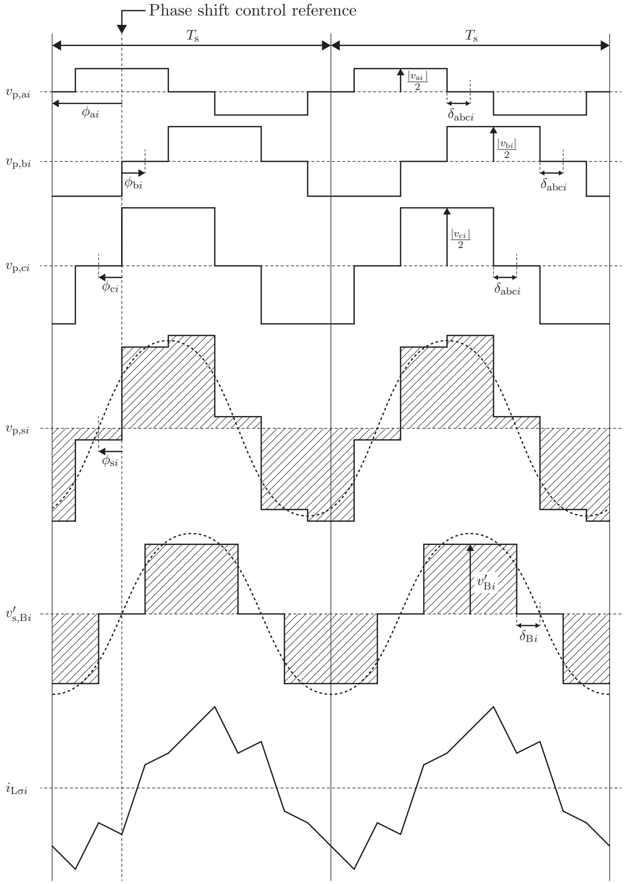

Phase shift control reference
T_s
T_s
$v_{\mathrm{p,a}i}$
$\phi_{\mathrm{a}i}$
$\frac{|v_{\mathrm{a}i}|}{2}$
$\delta_{\mathrm{abc}i}$
$v_{\mathrm{p,b}i}$
$\phi_{\mathrm{b}i}$
$\frac{|v_{\mathrm{b}i}|}{2}$
$\delta_{\mathrm{abc}i}$
$v_{\mathrm{p,c}i}$
$\phi_{\mathrm{c}i}$
$\frac{|v_{\mathrm{c}i}|}{2}$
$\delta_{\mathrm{abc}i}$
$v_{\mathrm{p,s}i}$
$\phi_{\mathrm{s}i}$
$v'_{\mathrm{s,B}i}$
$v'_{\mathrm{B}i}$
$\delta_{\mathrm{B}i}$
$i_{\mathrm{L}\sigma i}$

Figure 5.10: Square-wave voltages $v_{\mathrm{p,a}i}$, $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$ applied to the AC-side windings, the resulting voltage sum $v_{\mathrm{p,s}i}$, the AC-side referred square-wave voltage $v'_{\mathrm{s,B}i}$ applied to the series connection of the DC-side windings (or the single DC winding in case of a four-winding transformer) and the transformer leakage inductance current $i_{\mathrm{L}\sigma i}$ for the case $v_{\mathrm{b}i} > v_{\mathrm{a}i} > v_{\mathrm{c}i}$ in AC-to-DC operation over two switching cycles T_s.

This in turn leads to an almost constant ratio between the half-cycle voltage-second product of the voltage sum $v_{\mathrm{p,s}i}$ and the voltage $v_{\mathrm{s,B}i}$ generated by the DC-side full-bridge. In other words, the amplitude ratio of the MF fundamental waves of $v_{\mathrm{p,s}i}$ and $v_{\mathrm{s,B}i}$ becomes time-independent.

Medium-frequency (MF) fundamental model

For simple analytical calculations, a MF fundamental model of the multi-port module is considered where higher order harmonics of the MF square-wave voltages applied to the transformer windings are neglected. The MF voltages considering the clamping intervals $2\delta_{\mathrm{abc}i}$, $2\delta_{\mathrm{B}i}$ (see **Fig. 5.10**) and the resulting leakage inductance current are then described as complex MF phasors which are given by

$$\underline{v}_{\mathrm{p,a}i} = \frac{2v_{\mathrm{a}}\cos\left(\delta_{\mathrm{abc}i}\right)}{\pi} e^{j\phi_{\mathrm{a}i}}, \tag{5.35}$$

$$\underline{v}_{\mathrm{p,b}i} = \frac{2v_{\mathrm{b}}\cos\left(\delta_{\mathrm{abc}i}\right)}{\pi} e^{j\phi_{\mathrm{b}i}}, \tag{5.36}$$

$$\underline{v}_{\mathrm{p,c}i} = \frac{2v_{\mathrm{c}}\cos\left(\delta_{\mathrm{abc}i}\right)}{\pi} e^{j\phi_{\mathrm{c}i}}, \tag{5.37}$$

$$\underline{v}'_{\mathrm{s,B}i} = \frac{4nv_{\mathrm{B}i}\cos\left(\delta_{\mathrm{B}i}\right)}{\pi} e^{j\phi_{\mathrm{B}i}}, \tag{5.38}$$

$$\underline{i}_{\mathrm{L}\sigma i} = \hat{i}_{\mathrm{L}\sigma i} e^{j\phi_{\sigma i}} = \frac{\underline{v}_{\mathrm{p,a}i} + \underline{v}_{\mathrm{p,b}i} + \underline{v}_{\mathrm{p,c}i} - \underline{v}'_{\mathrm{s,B}i}}{j\omega_{\mathrm{s}} L_{\sigma}}. \tag{5.39}$$

The MF phasors rotate with the angular frequency $\omega_{\mathrm{s}} = 2\pi f_{\mathrm{s}}$. Additionally, $\underline{v}_{\mathrm{p,a}i}$, $\underline{v}_{\mathrm{p,b}i}$, $\underline{v}_{\mathrm{p,c}i}$ show a time-dependent amplitude caused by the AC grid voltage waveforms and a time-dependent phase caused by the time-varying phase shift control.

The square-wave voltage $v_{\mathrm{s,B}i}$ is chosen to be the reference for the phase shift control as shown in **Fig. 5.10** and its phasor is placed on the real axis of the complex coordinate system ($\phi_{\mathrm{B}i} = 0$) as depicted in the phasor diagram in **Fig. 5.9(c)**.

At the AC side, a common clamping interval $2\delta_{\mathrm{abc}i}$ is introduced such that the phase currents exhibit the same amplitudes for the case of a symmetrical three-phase current system. Nevertheless, the current amplitudes could be varied independently by introducing separate clamping intervals as control variables.

Modulation and control strategy

For the multi-port module, a time-varying phase shift control is applied where the phase angles $\phi_{\mathrm{a}i}$, $\phi_{\mathrm{b}i}$, $\phi_{\mathrm{c}i}$ appearing in (5.35)-(5.37) represent the control functions whose waveforms have to assure sinusoidal phase currents i_{a}, i_{b}, i_{c} with a given amplitude $\hat{I}_{\mathrm{abc}}$ and a given phase shift ϕ_{abc} towards the phase voltages

$$v_{\mathrm{a}} = \hat{V}_{\mathrm{abc}} \cos\left(\omega_{\mathrm{abc}} t\right), \tag{5.40}$$

$$v_{\mathrm{b}} = \hat{V}_{\mathrm{abc}} \cos\left(\omega_{\mathrm{abc}} t - \frac{2\pi}{3}\right), \tag{5.41}$$

$$v_{\mathrm{c}} = \hat{V}_{\mathrm{abc}} \cos\left(\omega_{\mathrm{abc}} t - \frac{4\pi}{3}\right) \tag{5.42}$$

where $\omega_{\mathrm{abc}} = 2\pi f_{\mathrm{abc}}$ describes the angular grid frequency.

To get the required phase currents, the control functions are chosen in such a way that the corresponding instantaneous power $p_{\mathrm{ma}i}$, $p_{\mathrm{mb}i}$, $p_{\mathrm{mc}i}$ is drawn from or delivered to the port which in turn is modeled by the equivalent MF voltage source (see **Fig. 5.9(b)**). The average active power flowing out or into the equivalent sources over one switching cycle T_{s} can be determined with the MF fundamental model according to

$$p_{\mathrm{ma}i} = \mathrm{Re}\left\{\frac{1}{2}\underline{v}_{\mathrm{p,a}i}\overline{\underline{i}_{\mathrm{L}\sigma i}}\right\} = v_{\mathrm{a}}\frac{\hat{i}_{\mathrm{L}\sigma i}\cos\left(\delta_{\mathrm{abc}i}\right)}{\pi}\cos\left(\phi_{\mathrm{a}i} - \phi_{\sigma i}\right), \tag{5.43}$$

$$p_{\mathrm{mb}i} = \mathrm{Re}\left\{\frac{1}{2}\underline{v}_{\mathrm{p,b}i}\overline{\underline{i}_{\mathrm{L}\sigma i}}\right\} = v_{\mathrm{b}}\frac{\hat{i}_{\mathrm{L}\sigma i}\cos\left(\delta_{\mathrm{abc}i}\right)}{\pi}\cos\left(\phi_{\mathrm{b}i} - \phi_{\sigma i}\right), \tag{5.44}$$

$$p_{\mathrm{mc}i} = \mathrm{Re}\left\{\frac{1}{2}\underline{v}_{\mathrm{p,c}i}\overline{\underline{i}_{\mathrm{L}\sigma i}}\right\} = v_{\mathrm{c}}\frac{\hat{i}_{\mathrm{L}\sigma i}\cos\left(\delta_{\mathrm{abc}i}\right)}{\pi}\cos\left(\phi_{\mathrm{c}i} - \phi_{\sigma i}\right). \tag{5.45}$$

Taking the reactive power consumed by the AC capacitors C_{ac} into account, the reference value of the control current can be represented by a phasor

$$\underline{I}_{\mathrm{m}i} = \underline{I}_{\mathrm{abc}} - \underline{I}_{\mathrm{C}i} \tag{5.46}$$

as shown in **Fig. 5.9(a)** where the capacitor current is given by

$$\underline{I}_{\mathrm{C}i} = j\omega_{\mathrm{abc}}\frac{C_{\mathrm{ac}}}{2}\left(\underline{V}_{\mathrm{abc}} - j\omega_{\mathrm{abc}}L_{\mathrm{ac}}\underline{I}_{\mathrm{abc}}\right). \tag{5.47}$$

The load is represented by a controlled current source $\underline{I}_{\mathrm{m}i}$ which corresponds to the drawn or injected power at the port in phase shift operation. The phasor of the phase reference current is

$$\underline{I}_{\mathrm{abc}} = \hat{I}_{\mathrm{abc}} e^{j\phi_{\mathrm{abc}}}. \tag{5.48}$$

$\hat{I}_{\mathrm{abc}}$ denotes the reference amplitude whereas ϕ_{abc} is the reference phase of the AC port currents i_{a}, i_{b}, i_{c}.

In the time domain, the reference values of the control currents per phase are then given by

$$i^*_{\mathrm{ma}i} = \hat{I}_{\mathrm{m}i} \cos\left(\omega_{\mathrm{abc}} t + \phi_{\mathrm{m}i}\right), \tag{5.49}$$

$$i^*_{\mathrm{mb}i} = \hat{I}_{\mathrm{m}i} \cos\left(\omega_{\mathrm{abc}} t - \frac{2\pi}{3} + \phi_{\mathrm{m}i}\right), \tag{5.50}$$

$$i^*_{\mathrm{mc}i} = \hat{I}_{\mathrm{m}i} \cos\left(\omega_{\mathrm{abc}} t - \frac{4\pi}{3} + \phi_{\mathrm{m}i}\right) \tag{5.51}$$

with amplitude $\hat{I}_{\mathrm{m}i} = |\underline{I}_{\mathrm{m}i}|$ and phase $\phi_{\mathrm{m}i} = \angle \underline{I}_{\mathrm{m}i}$.

The control functions $\phi_{\mathrm{a}i}$, $\phi_{\mathrm{b}i}$, $\phi_{\mathrm{c}i}$ can be determined using the nonlinear system of equations

$$i^*_{\mathrm{ma}i} = \frac{p_{\mathrm{ma}i}}{v_{\mathrm{a}}} = \frac{\hat{i}_{\mathrm{L}\sigma i} \cos\left(\delta_{\mathrm{abc}i}\right)}{\pi} \cos\left(\phi_{\mathrm{a}i} - \phi_{\sigma i}\right), \tag{5.52}$$

$$i^*_{\mathrm{mb}i} = \frac{p_{\mathrm{mb}i}}{v_{\mathrm{b}}} = \frac{\hat{i}_{\mathrm{L}\sigma i} \cos\left(\delta_{\mathrm{abc}i}\right)}{\pi} \cos\left(\phi_{\mathrm{b}i} - \phi_{\sigma i}\right), \tag{5.53}$$

$$i^*_{\mathrm{mc}i} = \frac{p_{\mathrm{mc}i}}{v_{\mathrm{c}}} = \frac{\hat{i}_{\mathrm{L}\sigma i} \cos\left(\delta_{\mathrm{abc}i}\right)}{\pi} \cos\left(\phi_{\mathrm{c}i} - \phi_{\sigma i}\right) \tag{5.54}$$

while considering $\hat{i}_{\mathrm{L}\sigma i} = |\underline{i}_{\mathrm{L}\sigma i}|$ and $\phi_{\sigma i} = \angle \underline{i}_{\mathrm{L}\sigma i}$.

By comparing (5.49)-(5.51) with (5.52)-(5.54) and knowing that $\delta_{\mathrm{abc}i}, \delta_{\mathrm{B}i} \in [0, \pi/2]$, the most obvious control functions which lead to sinusoidal AC port currents show the mathematical form

$$\phi_{\mathrm{a}i} = \omega_{\mathrm{abc}} t + \phi_{\mathrm{s}i}, \tag{5.55}$$

$$\phi_{\mathrm{b}i} = \omega_{\mathrm{abc}} t - \frac{2\pi}{3} + \phi_{\mathrm{s}i}, \tag{5.56}$$

$$\phi_{\mathrm{c}i} = \omega_{\mathrm{abc}} t - \frac{4\pi}{3} + \phi_{\mathrm{s}i}. \tag{5.57}$$

The amplitude and the phase of the reference values of the control currents according to (5.49)-(5.51) are then given by

$$\hat{I}_{\mathrm{m}i} = \frac{\hat{i}_{\mathrm{L}\sigma i} \cos\left(\delta_{\mathrm{abc}i}\right)}{\pi}, \tag{5.58}$$

$$\phi_{\mathrm{m}i} = \phi_{\mathrm{s}i} - \phi_{\sigma i} \tag{5.59}$$

where $\delta_{\mathrm{abc}i}$, $\phi_{\mathrm{s}i}$ represent the primary control variables from which the phase angles $\phi_{\mathrm{a}i}$, $\phi_{\mathrm{b}i}$, $\phi_{\mathrm{c}i}$ can be derived.

Inserting the control functions $\phi_{\mathrm{a}i}$, $\phi_{\mathrm{b}i}$, $\phi_{\mathrm{c}i}$ according to (5.55)-(5.57) into (5.35)-(5.37) and adding the voltage phasors, the composed voltage sum phasor

$$\underline{v}_{\mathrm{p,s}i} = \underline{v}_{\mathrm{p,a}i} + \underline{v}_{\mathrm{p,b}i} + \underline{v}_{\mathrm{p,c}i} = \hat{v}_{\mathrm{p,s}i} e^{j\phi_{\mathrm{s}i}} = \frac{3\hat{V}_{\mathrm{abc}} \cos\left(\delta_{\mathrm{abc}i}\right)}{\pi} e^{j\phi_{\mathrm{s}i}} \tag{5.60}$$

results which shows a time-independent amplitude $\hat{v}_{\mathrm{p,s}i}$ and a time-independent phase angle $\phi_{\mathrm{s}i}$. Applying the rotation operators $e^{j\phi_{\mathrm{a}i}}$, $e^{j\phi_{\mathrm{b}i}}$, $e^{j\phi_{\mathrm{c}i}}$ to the sinusoidal AC voltages v_{a}, v_{b}, v_{c}, a fixed space vector is formed which is then rotated over a switching cycle T_{s}. Due to the time-independent phasors $\underline{v}_{\mathrm{p,s}i}$, $\underline{v}'_{\mathrm{s,B}i}$, also the transformer leakage inductance current $\underline{i}_{\mathrm{L}\sigma i}$ shows a constant amplitude and phase over time. **Fig. 5.9(c)** depicts a phasor diagram of the MF phasors $\underline{v}_{\mathrm{p,s}i}$, $\underline{v}'_{\mathrm{s,B}i}$, $\underline{v}_{\mathrm{L}\sigma i}$, $\underline{i}_{\mathrm{L}\sigma i}$ in case of capacitive AC port currents.

Solutions of control variables

In order to control the AC port phase currents to a corresponding amplitude $\hat{I}_{\mathrm{abc}}$ and a phase ϕ_{abc}, the primary control variables $\delta_{\mathrm{abc}i}$, $\phi_{\mathrm{s}i}$ have to be determined. This can be done by solving the nonlinear system of equations (5.52)-(5.54) while taking the control functions (5.55)-(5.57) and the evaluation of (5.39) into account.

The solutions of the control variables for a module design example are depicted in **Fig. 5.11** for phase angles $\phi_{\mathrm{abc}} = \left\{-\frac{\pi}{2}, -\frac{\pi}{4}, 0, \frac{\pi}{4}, \frac{\pi}{2}\right\}$. For each phase angle, the AC port current amplitude is limited to a maximum which corresponds to the maximum transferrable apparent power at the specific phase angle. For small current amplitudes, the control variable $\delta_{\mathrm{abc}i}$ shows almost the same value where the voltage sum phasor $\underline{v}_{\mathrm{p,s}i}$ exhibits approximately the same length as the DC voltage phasor $\underline{v}'_{\mathrm{s,B}i}$.

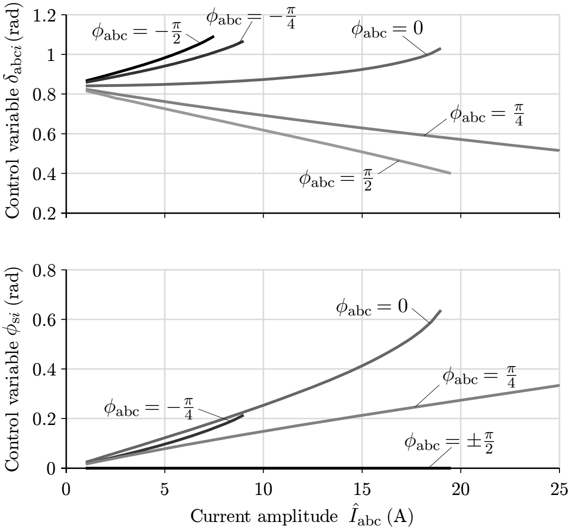


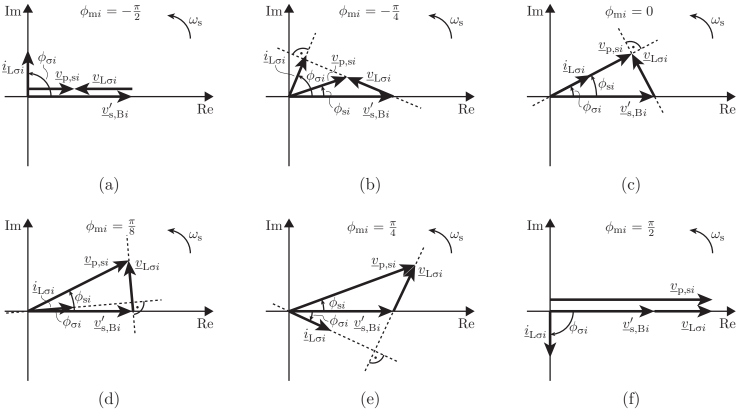
Figure 5.11: Control variables $\delta_{\mathrm{abc}i}$, $\phi_{\mathrm{s}i}$ plotted versus phase current amplitude $\hat{I}_{\mathrm{abc}}$ for $\delta_{\mathrm{B}i} = \frac{\pi}{6}$ and phase angles $\phi_{\mathrm{abc}} = \left\{-\frac{\pi}{2}, -\frac{\pi}{4}, 0, \frac{\pi}{4}, \frac{\pi}{2}\right\}$ for a module design example with the parameters $V_{\mathrm{abc,rms}} = 230\,\mathrm{V}$, $f_{\mathrm{abc}} = 50\,\mathrm{Hz}$, $V_{\mathrm{B}i} = 400\,\mathrm{V}$, $n = \frac{1}{2}$, $L_\sigma = 9\,\mu\mathrm{H}$, $f_{\mathrm{s}} = 20\,\mathrm{kHz}$.

Fig. 5.12 shows the MF phasor diagrams for different phase control angles $\phi_{\mathrm{m}i}$ in AC-to-DC operation. In case of negligible reactive power consumed by the AC capacitors C_{ac}, $\phi_{\mathrm{m}i}$ equals the phase current angle ϕ_{abc}.

Accuracy of fundamental model

In general, a periodic square-wave signal $s(t)$ with a clamping interval 2δ, an amplitude h and an angular frequency ω_{s} like the voltages depicted in **Fig. 5.10** can be represented by its Fourier series

$$s(t) = \frac{4h}{\pi} \sum_{k=1}^{\infty} \frac{\cos\left((2k-1)\delta\right) \sin\left((2k-1)\omega_{\mathrm{s}} t\right)}{2k-1}. \qquad (5.61)$$


Im
Re
ω_s
$\phi_{mi} = -\frac{\pi}{2}$
$\phi_{mi} = -\frac{\pi}{4}$
$\phi_{mi} = 0$
$\phi_{mi} = \frac{\pi}{8}$
$\phi_{mi} = \frac{\pi}{4}$
$\phi_{mi} = \frac{\pi}{2}$
$\underline{i}_{L\sigma i}$
$\underline{v}_{p,si}$
$\underline{v}_{L\sigma i}$
$\underline{v}'_{s,Bi}$
$\phi_{\sigma i}$
ϕ_{si}

(a) (b) (c) (d) (e) (f)

Figure 5.12: Phasor diagrams for the MF fundamental model for phase control angles $\phi_{mi} = -\frac{\pi}{2}$ (a), $\phi_{mi} = -\frac{\pi}{4}$ (b), $\phi_{mi} = 0$ (c), $\phi_{mi} = \frac{\pi}{8}$ (d), $\phi_{mi} = \frac{\pi}{4}$ (e) and $\phi_{mi} = \frac{\pi}{2}$ (f).

When adding the MF square-wave voltages $v_{p,ai}$, $v_{p,bi}$, $v_{p,ci}$ while considering their phase shifts from (5.55)-(5.57) and their amplitudes according to the half of (5.40)-(5.42), it can be seen from the Fourier series (5.61), that harmonics with an odd multiple of three of the MF fundamental frequency ω_s cancel out and are not present in the voltage sum $v_{p,si}$. Nevertheless, if $v_{s,Bi}$ exhibits these orders of MF harmonics, corresponding current harmonics in the transformer leakage inductance current are driven. This causes power shares at the AC ports which lead to LF current harmonics exhibiting odd multiples of three of the fundamental AC system frequency ω_{abc}. To suppress these LF AC current harmonics, $\delta_{Bi} = \frac{\pi}{6}$ can be chosen which in turn cancels out the corresponding MF harmonics in the square-wave voltage $v_{s,Bi}$. Besides the fundamental, MF current harmonics of order 5, 7, 11, 13, 17, ... remain in the transformer leakage inductance current and contribute to a small AC current distortion.

The control functions above are derived by setting

$$p^*_{abc} = p_{abc,(1)} \tag{5.62}$$

where p^*_{abc} denotes the reference value of the instantaneous power of the considered phase and $p_{abc,(1)}$ the MF fundamental power. In a next step, also higher order MF power shares are considered by solving

$$p^*_{\mathrm{abc}} = \sum_{k=1}^{\infty} p_{\mathrm{abc},(k)} \tag{5.63}$$

in order to get improved control functions and a lower input current total harmonic distortion (THD). This is shown in the next section where the control variables for a ZVS modulation are derived by a numerical optimization.

5.5.2 ZVS modulation

Since the modulation based on a fundamental wave model leads to undesirable AC phase current distortions at the AC ports of the multiport module, the development of an improved modulation scheme is mandatory. In addition to lowering the THD of the AC currents, also soft-switching in terms of ZVS for the use of MOSFETs is considered in the following.

The general power flow modeling described in Section 5.4 includes all imaginable types of modulation schemes with the control variables (phase shifts and clamping intervals) within their range of validity and can be used to look for optimal modulation schemes by means of numerical optimizations under certain constraints. This is done by minimizing the transformer leakage inductance RMS current under ZVS conditions as shown in the following.

Modulation and control under ZVS conditions

The derivation of a suitable modulation scheme under ZVS conditions is restricted to only positive instantaneous power flows from the AC ports to the DC port. This means that reactive power compensation at the AC ports is not considered in the following. Nevertheless, this can be achieved by further adjusting the modulation scheme which is beyond the scope of this thesis.

For simplification, the AC port voltages $v_{\mathrm{a}i}$, $v_{\mathrm{b}i}$, $v_{\mathrm{c}i}$ are sorted by their absolute values in descending order and accordingly renamed by $v_{\mathrm{ph1}i}$, $v_{\mathrm{ph2}i}$, $v_{\mathrm{ph3}i}$, such that the control variables only have to be obtained in a 30° sector of the AC line voltage. The solutions are then assigned to the corresponding phase in each sector. The degrees of freedom in control are the clamping intervals expressed by the variables

$\delta_{\mathrm{ph1}i}$, $\delta_{\mathrm{ph2}i}$, $\delta_{\mathrm{ph3}i}$, $\delta_{\mathrm{B}i}$ each multiplied by a factor of 2 and the phase angles $\phi_{\mathrm{ph1}i}$, $\phi_{\mathrm{ph2}i}$, $\phi_{\mathrm{ph3}i}$, $\phi_{\mathrm{B}i}$.

In **Fig. 5.13**, the square-wave voltages $v_{\mathrm{p,ph1}i}$, $v_{\mathrm{p,ph2}i}$, $v_{\mathrm{p,ph3}i}$, $v'_{\mathrm{s,B}i}$ applied to the AC- and DC-side windings are shown with the resulting leakage inductance current $i_{\mathrm{L}\sigma i}$ referred to the AC side.

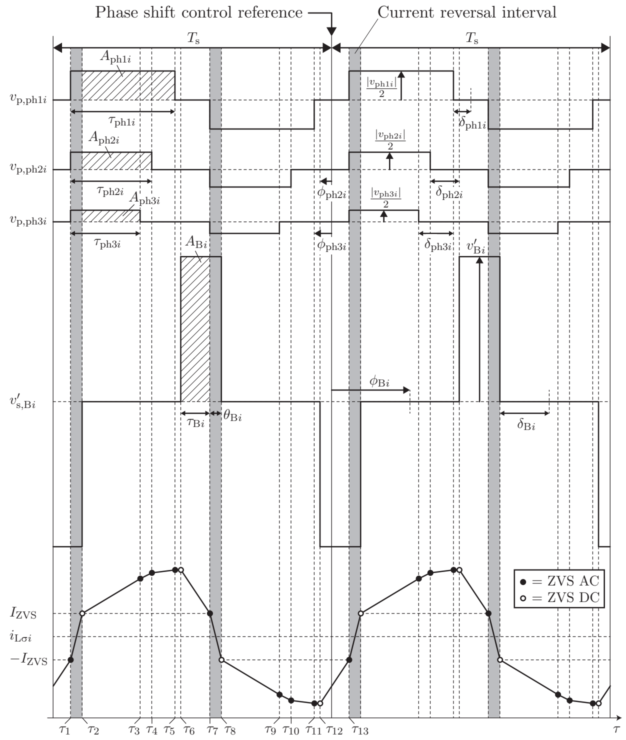

Phase shift control reference
Current reversal interval
T_s
T_s
$A_{\mathrm{ph1}i}$
$v_{\mathrm{p,ph1}i}$
$\frac{|v_{\mathrm{ph1}i}|}{2}$
$\tau_{\mathrm{ph1}i}$
$\delta_{\mathrm{ph1}i}$
$A_{\mathrm{ph2}i}$
$\frac{|v_{\mathrm{ph2}i}|}{2}$
$v_{\mathrm{p,ph2}i}$
$\tau_{\mathrm{ph2}i}$
$A_{\mathrm{ph3}i}$
$\phi_{\mathrm{ph2}i}$
$\frac{|v_{\mathrm{ph3}i}|}{2}$
$\delta_{\mathrm{ph2}i}$
$v_{\mathrm{p,ph3}i}$
$\tau_{\mathrm{ph3}i}$
$A_{\mathrm{B}i}$
$\phi_{\mathrm{ph3}i}$
$\delta_{\mathrm{ph3}i}$
$v'_{\mathrm{B}i}$
$\phi_{\mathrm{B}i}$
$v'_{\mathrm{s,B}i}$
$\tau_{\mathrm{B}i}$
$\theta_{\mathrm{B}i}$
$\delta_{\mathrm{B}i}$
● = ZVS AC
○ = ZVS DC
I_ZVS
$i_{\mathrm{L}\sigma i}$
$-I_\mathrm{ZVS}$
τ_1 τ_2 τ_3 τ_4 τ_5 τ_6 τ_7 τ_8 τ_9 τ_{10} τ_{11} τ_{12} τ_{13}
τ

Figure 5.13: Square-wave voltages $v_{\mathrm{p,ph1}i}$, $v_{\mathrm{p,ph2}i}$, $v_{\mathrm{p,ph3}i}$ applied to the AC-side windings, the AC-side referred square-wave voltage $v'_{\mathrm{s,B}i}$ applied to the series connection of the DC-side windings (or the single DC winding in case of a four-winding transformer) and the transformer leakage inductance current $i_{\mathrm{L}\sigma i}$ for the case $|v_{\mathrm{ph1}i}| > |v_{\mathrm{ph2}i}| > |v_{\mathrm{ph3}i}|$ in AC-to-DC operation over two switching cycles T_s.

The phase shift control reference is chosen to be the AC port with the highest absolute phase voltage, so that $\phi_{\mathrm{ph1}i} = 0$. Then, the total number of control variables to be determined equals seven (three phase angles and four clamping intervals).

To ensure ZVS conditions, the turn-off current of a switch has to be large enough to simultaneously charge and discharge the output capacitances of the switches in a bridge-leg within the interlocking interval (resonant transition). For the modulation scheme to achieve ZVS for all switches, the transformer leakage inductance current $i_{\mathrm{L}\sigma i}$ has to be positive in the interval $[\tau_2, \tau_7]$ and negative in the interval $[\tau_8, \tau_{13}]$ as shown by the dots in **Fig. 5.13** for the AC and the DC side.

This is achieved by defining a current reversal interval where the maximum available voltage is applied across the transformer leakage inductance L_σ as depicted in **Fig. 5.13** by the gray colored areas. During the time interval $[\tau_1, \tau_2]$ the AC-side winding voltages $v_{\mathrm{p,ph1}i}$, $v_{\mathrm{p,ph2}i}$, $v_{\mathrm{p,ph3}i}$ are positive whereas the DC-side winding voltage $v'_{\mathrm{s,B}i}$ is negative and vice versa during the interval $[\tau_7, \tau_8]$. The current reversal interval should be large enough to increase/decrease the current $i_{\mathrm{L}\sigma i}$ to the minimum commutation current $\pm I_{\mathrm{ZVS}}$ needed for ZVS. Simultaneously, this interval should not be too large, because it does not contribute to the active power transfer.

The restriction of the transformer leakage inductance current $i_{\mathrm{L}\sigma i}$ to its minimum commutation current $\pm I_{\mathrm{ZVS}}$ at the most critical points τ_1, τ_2, τ_7, τ_8 at the beginning and at the end of the current reversal intervals leads to a symmetrical alignment of the current points $i_{\mathrm{L}\sigma i}(\tau_1)$ and $i_{\mathrm{L}\sigma i}(\tau_2)$ as well as $i_{\mathrm{L}\sigma i}(\tau_7)$ and $i_{\mathrm{L}\sigma i}(\tau_8)$ around the zero line (see **Fig. 5.13**). This is done by setting the voltage-second product of the DC port equal to the sum of the voltage-second products of the AC ports during the power transfer interval $[\tau_2, \tau_7]$ according to

$$A_{\mathrm{B}i} = A_{\mathrm{ph1}i} + A_{\mathrm{ph2}i} + A_{\mathrm{ph3}i} \tag{5.64}$$

as shown by the shaded areas in **Fig. 5.13**. Since the sum of the absolute phase voltages varies with a six-pulse waveform, the primary referred DC voltage $v'_{\mathrm{B}i}$ should be always greater than the peak value of this sum. This means that the multi-port module operates always in AC-to-DC boost mode.

Optimal control variables

The solutions of the clamping intervals $2\delta_{\mathrm{ph1}i}$, $2\delta_{\mathrm{ph2}i}$, $2\delta_{\mathrm{ph3}i}$, $2\delta_{\mathrm{B}i}$ and the phase shifts $\phi_{\mathrm{ph1}i}$, $\phi_{\mathrm{ph2}i}$, $\phi_{\mathrm{ph3}i}$, $\phi_{\mathrm{B}i}$ (see **Fig. 5.13**) are numerically determined by minimizing the transformer leakage inductance RMS current $I_{\mathrm{L}\sigma i,\mathrm{rms}}$ subject to the power flow and the ZVS constraints in order to minimize the conduction losses. The corresponding optimization procedure is shown in **Fig. 5.14**.

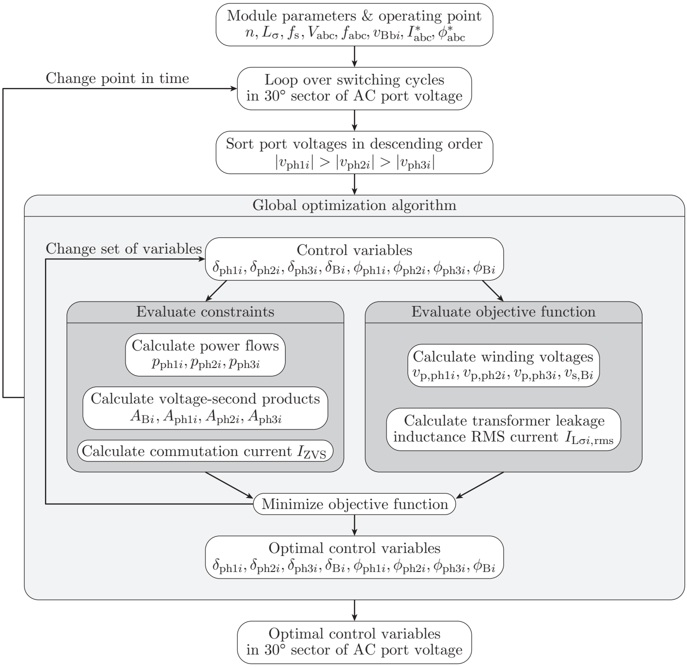

Module parameters & operating point
$n, L_\sigma, f_\mathrm{s}, V_\mathrm{abc}, f_\mathrm{abc}, v_{\mathrm{B}\mathrm{b}i}, I^*_\mathrm{abc}, \phi^*_\mathrm{abc}$
Change point in time
Loop over switching cycles in 30° sector of AC port voltage
Sort port voltages in descending order
$|v_{\mathrm{ph1}i}| > |v_{\mathrm{ph2}i}| > |v_{\mathrm{ph3}i}|$
Global optimization algorithm
Change set of variables
Control variables
$\delta_{\mathrm{ph1}i}, \delta_{\mathrm{ph2}i}, \delta_{\mathrm{ph3}i}, \delta_{\mathrm{B}i}, \phi_{\mathrm{ph1}i}, \phi_{\mathrm{ph2}i}, \phi_{\mathrm{ph3}i}, \phi_{\mathrm{B}i}$
Evaluate constraints
Calculate power flows
$p_{\mathrm{ph1}i}, p_{\mathrm{ph2}i}, p_{\mathrm{ph3}i}$
Calculate voltage-second products
$A_{\mathrm{B}i}, A_{\mathrm{ph1}i}, A_{\mathrm{ph2}i}, A_{\mathrm{ph3}i}$
Calculate commutation current I_ZVS
Evaluate objective function
Calculate winding voltages
$v_{\mathrm{p,ph1}i}, v_{\mathrm{p,ph2}i}, v_{\mathrm{p,ph3}i}, v_{\mathrm{s,B}i}$
Calculate transformer leakage inductance RMS current $I_{\mathrm{L}\sigma i,\mathrm{rms}}$
Minimize objective function
Optimal control variables
$\delta_{\mathrm{ph1}i}, \delta_{\mathrm{ph2}i}, \delta_{\mathrm{ph3}i}, \delta_{\mathrm{B}i}, \phi_{\mathrm{ph1}i}, \phi_{\mathrm{ph2}i}, \phi_{\mathrm{ph3}i}, \phi_{\mathrm{B}i}$
Optimal control variables in 30° sector of AC port voltage

Figure 5.14: Flow chart of the optimization algorithm to derive optimal control variables by minimizing the transformer leakage inductance RMS current $I_{\mathrm{L}\sigma i,\mathrm{rms}}$ subject to the power flow and the ZVS constraints. I^*_abc and ϕ^*_abc represent the reference values (RMS current and phase angle) for the AC port currents. For PFC operation, the reference phase ϕ^*_abc is set to zero.

For every switching cycle $T_\mathrm{s} = \frac{2\pi}{\omega_\mathrm{s}}$ in a 30° sector of the AC port voltage, the optimization routine calculates the optimal control variables.

The optimization problem is stated as

$$\min_{x} \left[\frac{1}{T_\mathrm{s}} \int\limits_{0}^{T_\mathrm{s}} i_{\mathrm{L}\sigma i}^2(x, \tau) \, \mathrm{d}\tau \right] \tag{5.65}$$

with respect to

$$x = \begin{bmatrix} \delta_{\mathrm{ph1}i} \\ \delta_{\mathrm{ph2}i} \\ \delta_{\mathrm{ph3}i} \\ \delta_{\mathrm{B}i} \\ \phi_{\mathrm{ph1}i} \\ \phi_{\mathrm{ph2}i} \\ \phi_{\mathrm{ph3}i} \\ \phi_{\mathrm{B}i} \end{bmatrix} \text{ with } x_\mathrm{lb} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ -\pi \\ -\pi \\ -\pi \\ -\pi \end{bmatrix}, \; x_\mathrm{ub} = \begin{bmatrix} \pi/2 \\ \pi/2 \\ \pi/2 \\ \pi/2 \\ \pi \\ \pi \\ \pi \\ \pi \end{bmatrix} \tag{5.66}$$

where x denotes the vector of control variables which is restricted to lower and upper bounds x_lb, x_ub.

The first equality constraints are given by the AC-side reference power flows $p^*_{\mathrm{ph1}i}$, $p^*_{\mathrm{ph2}i}$, $p^*_{\mathrm{ph3}i}$ according to

$$p_{\mathrm{ph1}i} = p^*_{\mathrm{ph1}i}, \tag{5.67}$$

$$p_{\mathrm{ph2}i} = p^*_{\mathrm{ph2}i}, \tag{5.68}$$

$$p_{\mathrm{ph3}i} = p^*_{\mathrm{ph3}i} \tag{5.69}$$

where the instantaneous power flows $p_{\mathrm{ph1}i}$, $p_{\mathrm{ph2}i}$, $p_{\mathrm{ph3}i}$ are calculated by the general power flow equation (5.31) with the power shares (5.32)-(5.34) expressed as functions of the power flow between two ports (5.30) depending on the control variables. The DC-side power flow is then inherently given. Further equality constraints are

$$\phi_{\mathrm{ph1}i} = 0, \tag{5.70}$$

$$\phi_{\mathrm{ph2}i} = \delta_{\mathrm{ph2}i} - \delta_{\mathrm{ph1}i}, \tag{5.71}$$

$$\phi_{\mathrm{ph3}i} = \delta_{\mathrm{ph3}i} - \delta_{\mathrm{ph1}i} \tag{5.72}$$

where phase 1 with the highest absolute phase voltage is defined as phase shift control reference and $\phi_{\mathrm{ph}2i}$, $\phi_{\mathrm{ph}3i}$ are written as functions of the AC-side clamping intervals (see **Fig. 5.13**). The last equality constraint is given by the voltage-second product equalization using (5.64). The inequality constraints arise from the position of the square-wave voltage applied at the DC port in relation to the AC-side applied MF voltages and the minimum commutation current for ZVS. The rising edge of the MF DC winding voltage from 0 to $v_{\mathrm{B}i}$ is constrained to the interval $[\tau_1, \tau_7]$ by means of

$$-\phi_{\mathrm{B}i} + \delta_{\mathrm{B}i} \geq \delta_{\mathrm{ph}1i} \ (= \tau_1), \tag{5.73}$$

$$-\phi_{\mathrm{B}i} + \delta_{\mathrm{B}i} \leq \delta_{\mathrm{ph}1i} + \pi \ (= \tau_7) \tag{5.74}$$

whereas the constraints for the rising edge from $-v_{\mathrm{B}i}$ to 0 in interval $[\tau_1, \tau_7]$ are given as

$$-\phi_{\mathrm{B}i} - \delta_{\mathrm{B}i} \geq \delta_{\mathrm{ph}1i} \ (= \tau_1), \tag{5.75}$$

$$-\phi_{\mathrm{B}i} - \delta_{\mathrm{B}i} \leq \delta_{\mathrm{ph}1i} + \pi \ (= \tau_7). \tag{5.76}$$

The minimum commutation current $I_{\mathrm{ZVS}} > 0$ needed for ZVS leads to the constraints

$$i_{\mathrm{L}\sigma i}(\tau_1) < -I_{\mathrm{ZVS}}, \tag{5.77}$$

$$i_{\mathrm{L}\sigma i}(\tau_2) > I_{\mathrm{ZVS}} \tag{5.78}$$

as can be seen from **Fig. 5.13**. At the time instants τ_7, τ_8, ZVS is then inherently guaranteed due to the symmetry of the modulation scheme in the first and the second half of the switching period. The transformer leakage inductance current $i_{\mathrm{L}\sigma i}$ at the switching instants τ_1, τ_2 is given by

$$i_{\mathrm{L}\sigma i}(\tau_1) = \frac{|v_{\mathrm{ph}1i}| + |v_{\mathrm{ph}2i}| + |v_{\mathrm{ph}3i}| + 2nv_{\mathrm{B}i}}{4\omega_{\mathrm{s}} L_\sigma} \left(\phi_{\mathrm{B}i} + \delta_{\mathrm{B}i} + \delta_{\mathrm{ph}1i}\right), \tag{5.79}$$

$$i_{\mathrm{L}\sigma i}(\tau_2) = -\frac{|v_{\mathrm{ph}1i}| + |v_{\mathrm{ph}2i}| + |v_{\mathrm{ph}3i}| + 2nv_{\mathrm{B}i}}{4\omega_{\mathrm{s}} L_\sigma} \left(\phi_{\mathrm{B}i} + \delta_{\mathrm{B}i} + \delta_{\mathrm{ph}1i}\right). \tag{5.80}$$

Analytic control variables

With the control variables numerically obtained by the above described optimization procedure (see **Fig. 5.14**), the rising edge of the MF DC winding voltage from 0 to $v_{\mathrm{B}i}$ is always lagging the falling edge of the MF AC winding voltage of phase 1 from $\frac{|v_{\mathrm{ph1}i}|}{2}$ to 0. This circumstance is used in the following for determining the control variables $\tau_{\mathrm{ph1}i}$, $\tau_{\mathrm{ph2}i}$, $\tau_{\mathrm{ph3}i}$, $\tau_{\mathrm{B}i}$, $\theta_{\mathrm{B}i}$ shown in **Fig. 5.13** analytically in a sequential calculation scheme.

First, from the minimum commutation current I_{ZVS} required for ZVS, the length of the current reversal interval is determined as

$$\theta_{\mathrm{B}i} = \frac{4\omega_{\mathrm{s}} L_\sigma I_{\mathrm{ZVS}}}{|v_{\mathrm{ph1}i}| + |v_{\mathrm{ph2}i}| + |v_{\mathrm{ph3}i}| + 2n v_{\mathrm{B}i}} \tag{5.81}$$

where $\omega_{\mathrm{s}} = \frac{2\pi}{T_{\mathrm{s}}}$. With the reference phase currents $i^*_{\mathrm{ph3}i}$, $i^*_{\mathrm{ph2}i}$, $i^*_{\mathrm{ph1}i}$, the control variables $\tau_{\mathrm{ph3}i}$, $\tau_{\mathrm{ph2}i}$, $\tau_{\mathrm{ph1}i}$ are then calculated by sequentially solving the equations

$$i^*_{\mathrm{ph3}i} = \frac{\mathrm{sign}(v_{\mathrm{ph3}i})}{2\pi} \int\limits_0^{\tau_{\mathrm{ph3}i}-\theta_{\mathrm{B}i}} \frac{|v_{\mathrm{ph1}i}| + |v_{\mathrm{ph2}i}| + |v_{\mathrm{ph3}i}|}{2\omega_{\mathrm{s}} L_\sigma}\tau + I_{\mathrm{ZVS}}\ \mathrm{d}\tau, \tag{5.82}$$

$$i^*_{\mathrm{ph2}i} = \alpha i^*_{\mathrm{ph3}i} + \frac{\mathrm{sign}(v_{\mathrm{ph2}i})}{2\pi} \int\limits_0^{\tau_{\mathrm{ph2}i}-\tau_{\mathrm{ph3}i}} \frac{|v_{\mathrm{ph1}i}| + |v_{\mathrm{ph2}i}|}{2\omega_{\mathrm{s}} L_\sigma}\tau + i_{\mathrm{L}\sigma i}(\tau_3)\ \mathrm{d}\tau, \tag{5.83}$$

$$i^*_{\mathrm{ph1}i} = \beta i^*_{\mathrm{ph2}i} + \frac{\mathrm{sign}(v_{\mathrm{ph1}i})}{2\pi} \int\limits_0^{\tau_{\mathrm{ph1}i}-\tau_{\mathrm{ph2}i}} \frac{|v_{\mathrm{ph1}i}|}{2\omega_{\mathrm{s}} L_\sigma}\tau + i_{\mathrm{L}\sigma i}(\tau_4)\ \mathrm{d}\tau \tag{5.84}$$

with the coefficients

$$\alpha = \frac{\mathrm{sign}(v_{\mathrm{ph2}i})}{\mathrm{sign}(v_{\mathrm{ph3}i})}, \tag{5.85}$$

$$\beta = \frac{\mathrm{sign}(v_{\mathrm{ph1}i})}{\mathrm{sign}(v_{\mathrm{ph2}i})} \tag{5.86}$$

where the integral terms represent the average current over a switching cycle from the AC ports to the DC port (see **Fig. 5.13**).

Finally, the voltage-second product equalization (5.64) shown by the shaded areas in **Fig. 5.13** leads to

$$\begin{aligned}\tau_{\mathrm{B}i} =& \frac{1}{2nv_{\mathrm{B}i}}\Bigg[|v_{\mathrm{ph1}i}|(\tau_{\mathrm{ph1}i}-\theta_{\mathrm{B}i}) \\ &+ |v_{\mathrm{ph2}i}|(\tau_{\mathrm{ph2}i}-\theta_{\mathrm{B}i}) + |v_{\mathrm{ph3}i}|(\tau_{\mathrm{ph3}i}-\theta_{\mathrm{B}i})\Bigg].\end{aligned} \tag{5.87}$$

The obtained control variables can then be transformed to the clamping intervals $\delta_{\mathrm{ph1}i}$, $\delta_{\mathrm{ph2}i}$, $\delta_{\mathrm{ph3}i}$, $\delta_{\mathrm{B}i}$ and the phase shifts $\phi_{\mathrm{ph1}i}$, $\phi_{\mathrm{ph2}i}$, $\phi_{\mathrm{ph3}i}$, $\phi_{\mathrm{B}i}$ according to

$$\delta_{\mathrm{ph1}i} = \frac{1}{2}\left(\pi - \tau_{\mathrm{ph1}i}\right), \tag{5.88}$$

$$\delta_{\mathrm{ph2}i} = \frac{1}{2}\left(\pi - \tau_{\mathrm{ph2}i}\right), \tag{5.89}$$

$$\delta_{\mathrm{ph3}i} = \frac{1}{2}\left(\pi - \tau_{\mathrm{ph3}i}\right), \tag{5.90}$$

$$\delta_{\mathrm{B}i} = \frac{1}{2}\left(\pi - \theta_{\mathrm{B}i} - \tau_{\mathrm{B}i}\right), \tag{5.91}$$

$$\phi_{\mathrm{ph1}i} = 0, \tag{5.92}$$

$$\phi_{\mathrm{ph2}i} = \delta_{\mathrm{ph2}i} - \delta_{\mathrm{ph1}i}, \tag{5.93}$$

$$\phi_{\mathrm{ph3}i} = \delta_{\mathrm{ph3}i} - \delta_{\mathrm{ph1}i}, \tag{5.94}$$

$$\phi_{\mathrm{B}i} = -\left(\delta_{\mathrm{ph1}i} + \theta_{\mathrm{B}i} + \delta_{\mathrm{B}i}\right). \tag{5.95}$$

Fig. 5.15 shows the control variables assigned to the phases over an AC mains period calculated for a multi-port module design example at an input power of 11 kW and a DC voltage of 460 V. For example, at 5 ms the clamping interval $\delta_{\mathrm{a}i}$ reaches its maximum value of $\frac{\pi}{2}$ where the reference power $p^*_{\mathrm{ma}i} = 0$ (PFC operation).

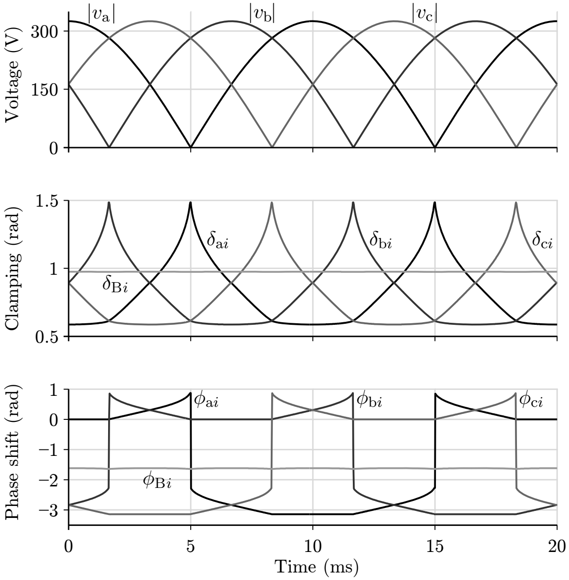


Figure 5.15: Control variables in terms of clamping intervals $\delta_{\mathrm{a}i}$, $\delta_{\mathrm{b}i}$, $\delta_{\mathrm{c}i}$, $\delta_{\mathrm{B}i}$ and phase shifts $\phi_{\mathrm{a}i}$, $\phi_{\mathrm{b}i}$, $\phi_{\mathrm{c}i}$, $\phi_{\mathrm{B}i}$ plotted over an AC mains period for a reference phase current $I^*_{\mathrm{abc}} = 16\,\mathrm{A}$ in PFC operation for a module design example with the parameters $V_{\mathrm{abc,rms}} = 230\,\mathrm{V}$, $f_{\mathrm{abc}} = 50\,\mathrm{Hz}$, $V_{\mathrm{B}i} = 460\,\mathrm{V}$, $n = 1$, $L_\sigma = 11.5\,\mathrm{\mu H}$, $f_\mathrm{s} = 50\,\mathrm{kHz}$.

Maximum power transfer

The maximum power that can be transferred to the DC port by using the ZVS modulation depends on the applied switching devices with a required minimal commutation current I_{ZVS} to achieve ZVS and can be calculated via the DC-side integral (see **Fig. 5.13**)

$$\begin{aligned} p_{\mathrm{B}i,\mathrm{max}} &= \frac{1}{\pi}\int_0^{\tau_{\mathrm{B}i}} n v_{\mathrm{B}i}\left(\frac{n v_{\mathrm{B}i}}{\omega_\mathrm{s} L_\sigma}\tau + I_{\mathrm{ZVS}}\right)\,\mathrm{d}\tau \\ &= \frac{1}{\pi}\left(\frac{n^2 v_{\mathrm{B}i}^2 \tau_{\mathrm{B}i}^2}{2\omega_\mathrm{s} L_\sigma} + n v_{\mathrm{B}i} I_{\mathrm{ZVS}} \tau_{\mathrm{B}i}\right). \end{aligned} \tag{5.96}$$

5.5.3 Alternative modulations

Besides the two presented and investigated modulation schemes for the multi-port module depicted in **Fig. 5.2**, one can think of other modulation variations. For instance modulation schemes that allow ZCS at the AC side for the use of IGBTs while maintaining ZVS at the DC side suitable for a MOSFET application. Furthermore, instead of transferring power from the AC ports at the same time in parallel, sequential schemes could be developed where only one phase transfers power while the other two are in a clamping state. Furthermore, by integrating a resonant circuit into the multi-port module a series or parallel resonant converter [75] can be built where suitable modulation schemes could be investigated.

5.6 Module design

For the evaluation of the efficiency of an AC-DC multi-port module as depicted in **Fig. 5.2**, a design example applying the ZVS modulation previously described in Section 5.5.2 is presented in the following. The multi-port design example basically represents a 10 kW three-phase bidirectional isolated AC-DC converter to connect to the 230 V low volt-

Table 5.1: Parameters of the AC-DC multi-port module design example.

Mains voltage	V_{abc}	230 V
Mains frequency	f_{abc}	50 Hz
Battery voltage	$V_{\mathrm{B}i}$	380 V…540 V
Nominal output power	$P_{\mathrm{B}i}$	10 kW
Switching frequency	$f_{\mathrm{s}i}$	50 kHz
Transformer turns ratio	n	1
Transformer leakage inductance	L_{σ}	11.5 µH
Transformer magnetizing inductance	-	neglected
Inductors	L_{ac}, L_{dc}	100 µH
Capacitors	C_{ac}	20 µF
Inductor	L_{dc}	100 µH
Capacitor	C_{dc}	60 µF

age AC grid and a DC-side storage battery pack with a voltage range of 380 V up to 540 V. The converter system can be used for instance as an electric vehicle battery charger or for uninterruptible power supplies. The parameters of the module design example are given in **Tab. 5.1** and are thoroughly discussed based on the selected components and the applied loss models in the following. A 3D model of the module design example is shown in **Fig. 5.16**.

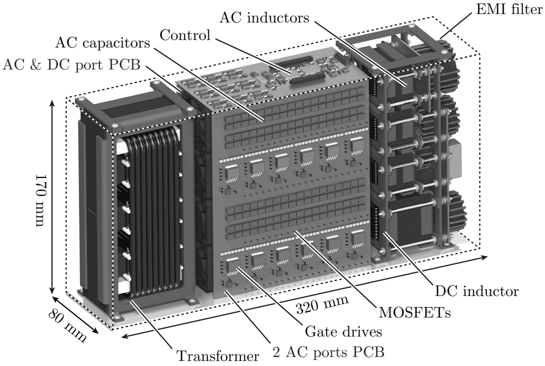

AC inductors
EMI filter
Control
AC capacitors
AC & DC port PCB
170 mm
DC inductor
320 mm
MOSFETs
80 mm
Gate drives
Transformer
2 AC ports PCB

Figure 5.16: 3D drawing of the 10 kW design example with a peak efficiency of 91.7 % at an output power of 10 kW and a battery voltage of 380 V. The power density is around 2.5 kW/L.

5.6.1 Power components

In order to evaluate the AC-DC multi-port module efficiencies at different operating points, the module components with their applied loss models are discussed. **Tab. 5.2** summarizes the components of the module design example.

Power MOSFETs

The use of the ZVS modulation described in Section 5.5.2 guarantees soft-switching for every switching device in the multi-port module at every switching instant. Therefore, MOSFETs are the best suited devices, preferably with a comparable low on-state resistance to keep the conduction losses low. As in the case of the AC-DC DAB module, a

Table 5.2: Components of the AC-DC multi-port module design example.

MOSFETs $S_{1\mathrm{a}}, S_{1\mathrm{b}}, S_{2\mathrm{a}}, S_{2\mathrm{b}}$	3x STY145N65M5, 650 V
MOSFETs $S_{3\mathrm{a}}, S_{3\mathrm{b}}$	3x STY145N65M5, 650 V
MOSFETs S_1, S_2, S_3, S_4	3x STY145N65M5, 650 V
Transformer	2x 2x E 80/38/20 N87 9 AC-side turns, 9 DC-side turns Litz wire, 2205 strands, 0.071 mm
Inductors L_{ac}	2x Kool Mu 4317 26u, 27 turns Litz wire, 20 strands, 0.355 mm
Inductor L_{dc}	2x Kool Mu 4022 26u, 24 turns Litz wire, 45 strands, 0.355 mm
Capacitors C_{ac}	36x Syfer 1825J630564KX, 560 nF
Capacitor C_{dc}	108x Syfer 1825J630564KX, 560 nF

650 V MOSFET with an on-state resistance of 14 mΩ at 25 °C from STMicroelectronics [149] is considered. The AC-side T-type circuits apply three MOSFETs in parallel for the half-bridge and three MOSFETs in parallel for the clamping switch. For the DC-side full-bridge, also three MOSFET devices are paralleled.

The MOSFET loss model is based on data sheet parameters and described in Section B.1.2. The gate drive losses are modeled according to Section B.1.3.

Transformer

For the design example, a four-winding transformer consisting of two stacked E-core sets E 80/38/20 [162] next to each other with N87 ferrite material [163] is used with the AC-side windings wound on separate magnetically paralleled legs and the DC winding around them as depicted in **Fig. 5.17(a)** and **Fig. 5.17(c)**. The leakage space between the AC windings and the DC winding defines the size of the total leakage inductance. The turns ratios n from each AC-side winding to the DC-side winding of the transformer are chosen such that

$$n v_{\mathrm{B}i} > \frac{\hat{V}_{\mathrm{abc}}}{2} \tag{5.97}$$

at the lowest battery voltage of 380 V with the battery voltage $v'_{\mathrm{B}i} = nv_{\mathrm{B}i}$ referred to the AC side of the transformer. This guarantees that the multi-port module is always operated in AC-to-DC boost mode what has been a prerequisite for developing the ZVS modulation.

The total leakage inductance of the four-winding transformer is approximated by a simplified analytical calculation of the magnetic field energy. The magnetic field is modeled by a 1D approximation as shown in **Fig. 5.17(b)** with a single component H_{z} whereas H_{x} and H_{y} are assumed to be zero. The fringing field at the top and the bottom of the windings (top view given in **Fig. 5.17(c)**) is neglected in the following.

The magnetic energy stored in an AC-side winding with a relative permeability of μ_{w}, a mean winding length of l_{p} and a winding layer thickness of d_{p} is given by

$$E_{\mathrm{ac}} = \frac{1}{2}\mu_0\mu_{\mathrm{w}} \int_0^{d_{\mathrm{p}}} \left(\frac{N_{\mathrm{p}} I_{\mathrm{p}}}{h_{\mathrm{w}}} \frac{x}{d_{\mathrm{p}}}\right)^2 l_{\mathrm{p}} h_{\mathrm{w}} \, \mathrm{d}x = \frac{\mu_0\mu_{\mathrm{w}} N_{\mathrm{p}}^2 I_{\mathrm{p}}^2 d_{\mathrm{p}} l_{\mathrm{p}}}{6h_{\mathrm{w}}}. \tag{5.98}$$

For the DC-side winding a similar calculation with a mean winding length of l_{s} and a winding layer thickness of d_{s} leads to the energy

$$E_{\mathrm{dc}} = \frac{1}{2}\mu_0\mu_{\mathrm{w}} \int_0^{d_{\mathrm{s}}} \left(\frac{N_{\mathrm{s}} I_{\mathrm{s}}}{h_{\mathrm{w}}} \frac{x}{d_{\mathrm{s}}}\right)^2 l_{\mathrm{s}} h_{\mathrm{w}} \, \mathrm{d}x = \frac{\mu_0\mu_{\mathrm{w}} N_{\mathrm{s}}^2 I_{\mathrm{s}}^2 d_{\mathrm{s}} l_{\mathrm{s}}}{6h_{\mathrm{w}}}. \tag{5.99}$$

For the magnetic energy stored in the leakage domain as depicted in **Fig. 5.17(c)**, the magnetic field component H_{z} is constant all over the volume $A_\sigma h_{\mathrm{w}}$ so that

$$E_\sigma = \frac{1}{2}\mu_0\mu_\sigma \left(\frac{N_{\mathrm{p}} I_{\mathrm{p}}}{h_{\mathrm{w}}}\right)^2 A_\sigma h_{\mathrm{w}} = \frac{\mu_0\mu_\sigma N_{\mathrm{p}}^2 I_{\mathrm{p}}^2 A_\sigma}{2h_{\mathrm{w}}}. \tag{5.100}$$

By comparing the total magnetic field energy to the energy stored in an AC-side referred total leakage inductance L_σ with

$$E_{\mathrm{tot}} = 3E_{\mathrm{ac}} + E_{\mathrm{dc}} + E_\sigma = \frac{1}{2} L_\sigma I_{\mathrm{p}}^2, \tag{5.101}$$

the leakage inductance is finally given by

$$L_\sigma = \frac{2E_{\mathrm{tot}}}{I_{\mathrm{p}}^2}. \tag{5.102}$$

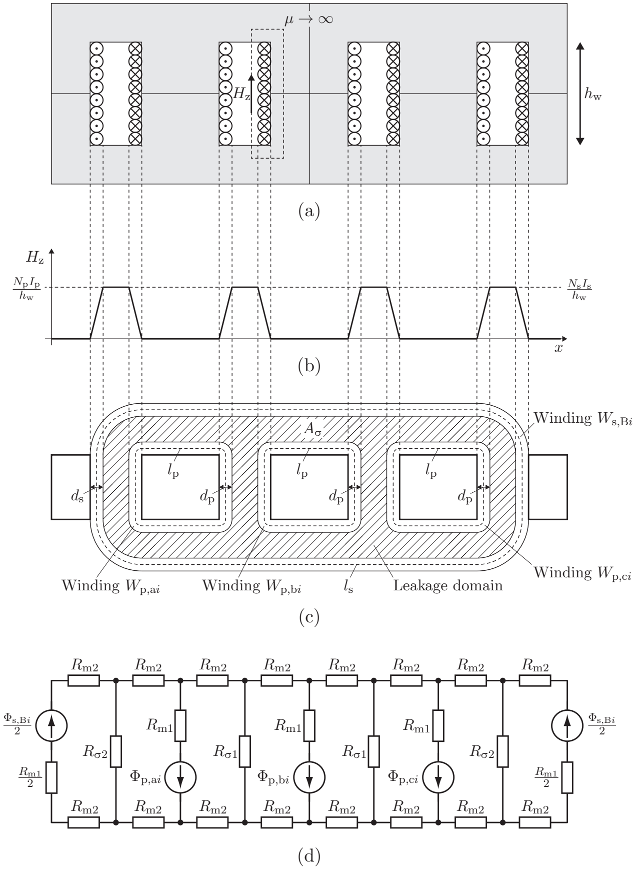

$\mu \to \infty$
H_z
h_w
(a)
H_z
$\frac{N_p I_p}{h_w}$
$\frac{N_s I_s}{h_w}$
x
(b)
Winding $W_{s,Bi}$
A_σ
l_p
l_p
l_p
d_s
d_p
d_p
d_p
Winding $W_{p,ai}$
Winding $W_{p,bi}$
l_s
Leakage domain
Winding $W_{p,ci}$
(c)
R_{m2}
$\frac{\Phi_{s,Bi}}{2}$
R_{m1}
$R_{\sigma 2}$
$R_{\sigma 1}$
$\frac{R_{m1}}{2}$
$\Phi_{p,ai}$
$\Phi_{p,bi}$
$\Phi_{p,ci}$
(d)

Figure 5.17: 2D drawing of the four-winding transformer in (a) consisting of two sets of E-cores. The AC-side windings $W_{p,ai}$, $W_{p,bi}$, $W_{p,ci}$ are wound on the inner legs with the DC-side winding $W_{s,Bi}$ wound around them. The leakage space between the AC windings and the DC winding defines the size of the total leakage inductance L_σ. In (b) the 1D magnetic field approximation with a single component H_z ($H_x = H_y = 0$ assumed) is depicted whereas (c) shows the top view of the four-winding transformer with the leakage domain A_σ. In (d) the reluctance model with the winding flux sources $\Phi_{p,ai}$, $\Phi_{p,bi}$, $\Phi_{p,ci}$, $\frac{\Phi_{s,Bi}}{2}$ is given.

The AC-side current excitation I_p cancels out due to Ampère's law with $N_\mathrm{p}I_\mathrm{p} = N_\mathrm{s}I_\mathrm{s}$ (see also **Fig. 5.17(b)**). The calculated leakage inductance deviates by 6.5 % for the considered four-winding transformer compared to a 3D finite element method (FEM) analysis carried out at 50 kHz. Especially with increasing core size, the fringing field at the top and the bottom of the windings cannot be neglected anymore as the deviations from the proposed calculation to a FEM analysis substantially increase.

The total transformer leakage inductance L_σ is determined in such a way, that the maximum power of 10 kW can be transferred at the switching frequency of 50 kHz and the lowest battery voltage of 380 V. From the maximum power flow equation (5.96), the leakage inductance L_σ is determined by setting $p_{\mathrm{B}i} = 10\,\mathrm{kW}$.

In the loss model, the core losses are calculated by applying the improved generalized Steinmetz equation (iGSE) as described in Section B.2.2 by solving the reluctance model of the four-winding transformer depicted in **Fig. 5.17(d)**. The skin and proximity effect losses in the litz wires for each current harmonic are determined according to Section B.2.1. The external magnetic field strength for evaluating proximity effect losses is derived by a 1D approximation.

For the given core arrangement, the total losses including core losses as well as skin and proximity effect losses using litz wire are minimized subject to turns ratio and leakage inductance constraints. The optimal number of turns is found to be 9 for all windings. 2114 strands for the AC windings and 2538 for the DC winding with a diameter of 0.08 mm lead to the lowest transformer losses. The design example applies the commercially available litz wire with 2205 strands with a diameter of 0.071 mm.

Inductors

The AC-side filter inductors L_ac are built with two stacked E-cores of type Kool Mu 4317 [154], the DC-side filter inductor L_dc with two stacked E-cores of type Kool Mu 4022 [164]. The chosen material for both core types is 26u from Magnetics [155]. Powder cores are ideally suited for the design example because they offer a distributed air gap and a high saturation flux density of around 1 T and are therefore advantageous over ferrite cores with a large air gap exhibiting considerable fringing magnetic field. Both inductors are wound with litz wire of 0.355 mm strand diameter, 20 strands in case of the AC inductors

L_{ac} and 45 strands for the DC inductor L_{dc}. The number of turns for the AC inductors are 27, for the DC inductor 24, so that a minimum inductance value of 100 µH is guaranteed at the highest peak current.

Again, the core losses are calculated by using the iGSE as given in Section B.2.2, the Steinmetz parameters are obtained from the material curves provided by the manufacturer [155]. The skin and proximity effect losses in the litz wire for each current harmonic are calculated according to Section B.2.1 with a 1D magnetic field approximation.

Capacitors

For the AC and DC port capacitors C_{ac}, C_{dc}, paralleled 560 nF, 630 V ceramic capacitors with dielectric X7R from Syfer [156] are used. Multilayer ceramic capacitors exhibit a high energy density and are therefore ideally suited to achieve high power densities. The applied loss model by considering the equivalent series resistance (ESR) from the manufacturers data sheet is discussed in Section B.3.

Auxiliary losses

Besides the load-dependent losses shown in the previous sections, a constant loss share of 40 W for the pre-charging relays, the FPGA control board, the sensing and four fans is considered. Additional losses caused by the EMI filter are approximated by an equivalent resistance of 4 mΩ.

Cooling system

The number of semiconductors basically defines the base plate size of the heat sink as 160 mm × 113 mm for the AC- and DC-side switching devices, so that a double-sided heat sink can be used. Four fans of type San Ace 40 mm × 40 mm are utilized for forced convection cooling. After optimizing the cooling system as described in [157], a thermal heat sink to ambient resistance of $R_{\mathrm{th,s\text{-}a}} = 0.12\,\mathrm{K/W}$ results which in turn leads to a cooling system performance index (CSPI) of 20.8.

5.6.2 Efficiency calculations

With the described power components above, the efficiencies of the module design example over the output power range are calculated for the battery voltages 380 V, 460 V and 540 V as shown in **Fig. 5.18**.

A peak efficiency of 91.7 % is reached at an output power of 10.1 kW and a battery voltage of 380 V. The estimated power density is around 2.5 kW/L.

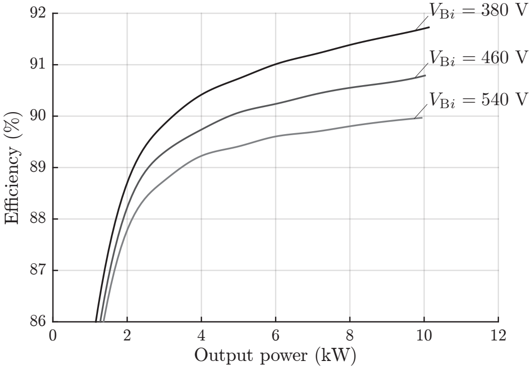


Figure 5.18: Calculated efficiencies of the AC-DC multi-port module design example applying the ZVS modulation from Section 5.5.2 over the output power range for the battery voltages 380 V, 460 V and 540 V. Due to relatively high switching losses and conduction losses caused by the circulating current through all ports, the efficiency of the AC-DC multi-port module is relatively low.

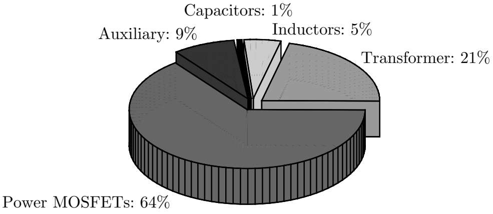


Figure 5.19: Calculated loss distribution between the AC-DC multi-port module components at the maximum output power of 10 kW and a battery voltage of 460 V applying the ZVS modulation from Section 5.5.2.

The loss distribution between the module components at the maximum output power of 10 kW and a battery voltage of 460 V is depicted in **Fig. 5.19**. The major parts of the losses represent the MOSFET losses with a percentage of 64 % and the transformer losses with a percentage of 21 %. The remaining percentage of 15 % accounts for the losses occurring in the AC- and DC-side filter inductors and capacitors as well as the auxiliary losses for the sensing, the control and the cooling.

5.7 Module simulation

For validating the developed modulation schemes for the AC-DC multi-port module, a circuit simulation in GeckoCIRCUITS [161] is performed. The simulation model corresponds to the multi-port module depicted in **Fig. 5.2**. The parameters of the simulation model are given below, separately for each modulation scheme.

The transformer arrangement is modeled with three single-phase transformers with an AC-side leakage inductance of $\frac{L_\sigma}{3}$ and the DC-side windings connected in series as previously shown in **Fig. 5.3**. The applied two-winding transformer model is the one of a basic ideal transformer without considering the magnetizing inductance but with the leakage inductance connected in series to the AC-side winding. Since the focus of the simulation lies on the implementation and verification of the modulation schemes for the proposed multi-port module, the transformer arrangement is only modeled in the electric domain.

Also for the storage battery, the application of a sophisticated model in terms of the open-circuit voltage depending on the state of charge (SOC) is not required as the verification of the modulation scheme in simulation can be done over a few AC grid cycle periods. Moreover, since only the steady state operation of the module is investigated, transient battery models are not necessary. Therefore, the storage battery is modeled as a constant voltage source.

In the following, the simulation results of the AC-DC multi-port module for the two proposed modulation schemes are presented and discussed.

5.7.1 Fundamental phasor modulation

The fundamental phasor modulation developed and proposed in Section 5.5.1 is implemented in Java as part of the simulation model. The parameters of the model are summarized in **Tab. 5.3**.

Table 5.3: Simulation parameters of the AC-DC multi-port module applying the fundamental phasor modulation.

Mains voltage	V_{abc}	230 V
Mains frequency	f_{abc}	50 Hz
Battery voltage	$V_{\mathrm{B}i}$	400 V
Switching frequency	$f_{\mathrm{s}i}$	20 kHz
Transformer turns ratios	n	1/2
Transformer leakage inductance	L_σ	9 µH
Transformer magnetizing inductance	-	neglected
Inductors	L_{ac}, L_{dc}	100 µH
Capacitors	C_{ac}	50 µF
Inductor	L_{dc}	100 µH
Capacitor	C_{dc}	50 µF

The control functions for the phase angles $\phi_{\mathrm{a}i}$, $\phi_{\mathrm{b}i}$, $\phi_{\mathrm{c}i}$ and the clamping interval $\delta_{\mathrm{abc}i}$ are calculated numerically via the primary control variables $\delta_{\mathrm{abc}i}$, $\phi_{\mathrm{s}i}$ (as depicted in **Fig. 5.11**) by solving the nonlinear system of equations (5.52)-(5.54) while taking the control functions (5.55)-(5.57) and the evaluation of (5.39) into account. The results are then stored in a lookup table (LUT) and loaded on each simulation start.

To keep the LF harmonic distortion at the AC grid side low, the AC-side clamping interval is fixed by setting $\delta_{\mathrm{B}i} = \frac{\pi}{6}$. The simulation is run without a feedback loop in place in order to validate the mathematical model of the modulation scheme. The reference phase current amplitude is set to $\hat{I}^*_{\mathrm{abc}} = 20\,\mathrm{A}$ with a reference phase angle $\phi^*_{\mathrm{abc}} = \frac{\pi}{8}$ (capacitive AC-to-DC operation).

Fig. 5.20 shows the simulated AC phase currents i_{a}, i_{b}, i_{c} and the DC current $i_{\mathrm{B}i}$ of the AC-DC multi-port module. Moreover, the module port voltages $v_{\mathrm{a}i}$, $v_{\mathrm{b}i}$, $v_{\mathrm{c}i}$, which are the voltages across the series connection of the two capacitors C_{ac}, with their characteristic sinusoidal waveforms in each phase are shown. It can be seen that the AC phase currents are slightly distorted which comes from the applied fundamental phasor modulation which does not consider high order MF harmonics in the model as discussed previously.

In **Fig. 5.21**, the simulated voltages across the transformer windings $v_{\mathrm{p,a}i}$, $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$, $v_{\mathrm{s,B}i}$ are shown with the transformer winding currents $i_{\mathrm{p,a}i}$, $i_{\mathrm{p,b}i}$, $i_{\mathrm{p,c}i}$, $i_{\mathrm{s,B}i}$. Since the magnetizing inductances of the transformers are neglected, all AC-side winding currents equal the leakage inductance current $i_{\mathrm{L}\sigma i}$ referred to the AC side. Furthermore, the resulting AC-side voltage sum $v_{\mathrm{p,s}i}$ with its corresponding six-pulse waveform is depicted.

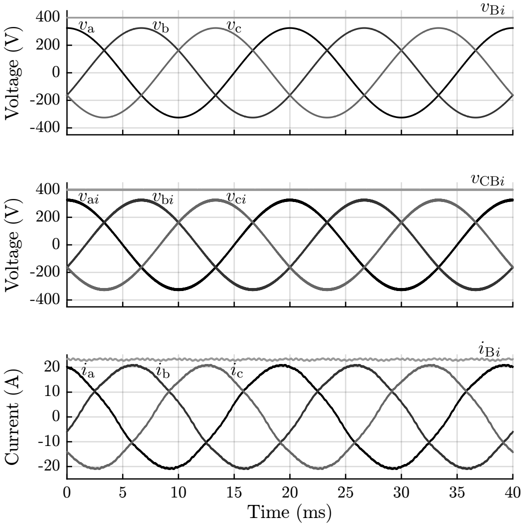


Figure 5.20: Simulated AC phase currents i_{a}, i_{b}, i_{c} and DC current $i_{\mathrm{B}i}$ of the AC-DC multi-port module (see **Fig. 5.2**) with the parameters given in **Tab. 5.3** applying the fundamental phasor modulation for the reference values $\hat{I}^{*}_{\mathrm{abc}} = 20\,\mathrm{A}$ and $\phi^{*}_{\mathrm{abc}} = \frac{\pi}{8}$ in AC-to-DC operation. The module voltages $v_{\mathrm{a}i}$, $v_{\mathrm{b}i}$, $v_{\mathrm{c}i}$ represent the voltages across the series connection of the two capacitors C_{ac} in each phase. $v_{\mathrm{CB}i}$ is the voltage across the DC capacitor C_{dc}.

Finally, the zoom of **Fig. 5.21** is given in **Fig. 5.22** where the actual MF voltage signals applied to the transformer windings and the resulting leakage inductance current can be clearly seen. The transformer current $i_{\mathrm{L}\sigma i}$ is shaped by the MF voltages $v_{\mathrm{p,s}i}$ and $v_{\mathrm{s,B}i}$. Nevertheless, the shape of the current $i_{\mathrm{L}\sigma i}$ cannot be controlled in such a way, that at every switching instant ZVS is achieved. This is, besides the LF current distortion, a further drawback of the introduced MF fundamental model.

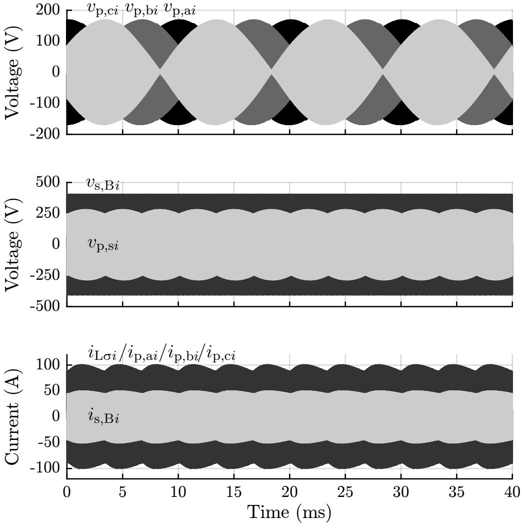


Figure 5.21: Simulated voltages $v_{\mathrm{p,a}i}$, $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$, $v_{\mathrm{s,B}i}$ across the transformer windings, resulting AC-side voltage sum $v_{\mathrm{p,s}i}$ and transformer winding currents $i_{\mathrm{p,a}i}$, $i_{\mathrm{p,b}i}$, $i_{\mathrm{p,c}i}$, $i_{\mathrm{s,B}i}$ of the AC-DC multi-port module (see **Fig. 5.2**) with the parameters given in **Tab. 5.3** applying the fundamental phasor modulation for the reference values $\hat{I}^*_{\mathrm{abc}} = 20\,\mathrm{A}$ and $\phi^*_{\mathrm{abc}} = \frac{\pi}{8}$ in AC-to-DC operation.

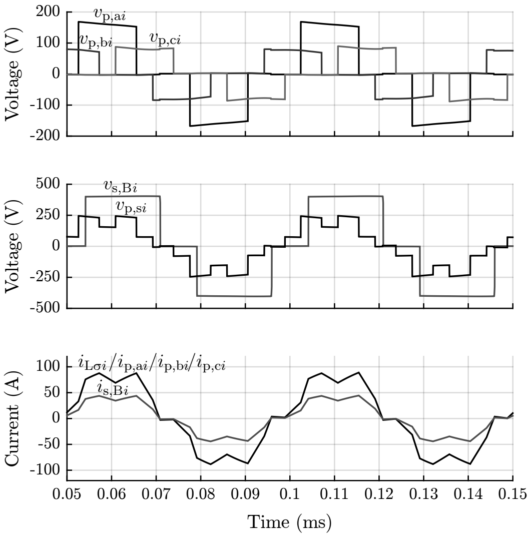


Figure 5.22: Zoom of **Fig. 5.21** with the simulated voltages $v_{\mathrm{p,a}i}$, $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$, $v_{\mathrm{s,B}i}$ across the transformer windings, resulting AC-side voltage sum $v_{\mathrm{p,s}i}$ and transformer winding currents $i_{\mathrm{p,a}i}$, $i_{\mathrm{p,b}i}$, $i_{\mathrm{p,c}i}$, $i_{\mathrm{s,B}i}$ of the AC-DC multi-port module (see **Fig. 5.2**) with the parameters given in **Tab. 5.3** applying the fundamental phasor modulation for the reference values $\hat{I}^{*}_{\mathrm{abc}} = 20\,\mathrm{A}$ and $\phi^{*}_{\mathrm{abc}} = \frac{\pi}{8}$ in AC-to-DC operation.

5.7.2 ZVS modulation

Also for the ZVS modulation presented in Section 5.5.2, the implementation is done in Java as part of the simulation model. The parameters of the model are summarized in **Tab. 5.4**. The control functions for the phase angles $\phi_{\mathrm{a}i}$, $\phi_{\mathrm{b}i}$, $\phi_{\mathrm{c}i}$, $\phi_{\mathrm{B}i}$ and the clamping intervals $\delta_{\mathrm{a}i}$, $\delta_{\mathrm{b}i}$, $\delta_{\mathrm{c}i}$, $\delta_{\mathrm{B}i}$ (as depicted in **Fig. 5.15**) are calculated numerically via the primary control variables $\tau_{\mathrm{ph1}i}$, $\tau_{\mathrm{ph2}i}$, $\tau_{\mathrm{ph3}i}$, $\tau_{\mathrm{B}i}$, $\theta_{\mathrm{B}i}$ shown in **Fig. 5.13** by sequentially solving the equations (5.81)-(5.87).

Table 5.4: Simulation parameters of the AC-DC multi-port module applying the ZVS modulation.

Mains voltage	V_{abc}	230 V
Mains frequency	f_{abc}	50 Hz
Battery voltage	$V_{\mathrm{B}i}$	460 V
Switching frequency	$f_{\mathrm{s}i}$	50 kHz
Transformer turns ratios	n	1
Transformer leakage inductance	L_{σ}	11.5 µH
Transformer magnetizing inductance	-	neglected
Inductors	L_{ac}, L_{dc}	100 µH
Capacitors	C_{ac}	20 µF
Inductor	L_{dc}	100 µH
Capacitor	C_{dc}	60 µF

Thereafter, the transformation equations given in (5.88)-(5.95) are applied to get the phase angles and the clamping intervals. The results are then stored in a LUT and loaded on each simulation start.

As in the case of the fundamental phasor modulation, the focus of the simulation lies on the validation of the ZVS modulation model what is done without a feedback loop in place. The reference phase RMS current is set to $I^*_{\mathrm{abc}} = 16\,\mathrm{A}$ with a reference phase angle $\phi^*_{\mathrm{abc}} = 0$ (AC-to-DC operation). With the developed ZVS modulation scheme, reactive power compensation at the AC ports is not possible, so that the AC-side capacitance values C_{ac} are substantially reduced compared to the case of the fundamental phasor modulation. This ensures to achieve a high power factor (PF) at the AC ports.

Fig. 5.23 shows the simulated AC phase currents i_{a}, i_{b}, i_{c} and the DC current $i_{\mathrm{B}i}$ of the AC-DC multi-port module. Furthermore, the module port voltages $v_{\mathrm{a}i}$, $v_{\mathrm{b}i}$, $v_{\mathrm{c}i}$ which are the voltages across the series connection of the two capacitors C_{ac} with their characteristic sinusoidal waveforms in each phase are shown. It can be seen that the AC phase currents are slightly leading the phase voltages which is due to the capacitive AC ports and the inability of the ZVS modulation to compensate the reactive power.

In **Fig. 5.24**, the simulated voltages across the transformer windings $v_{\mathrm{p,a}i}$, $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$, $v_{\mathrm{s,B}i}$ are shown with the transformer winding currents $i_{\mathrm{p,a}i}$, $i_{\mathrm{p,b}i}$, $i_{\mathrm{p,c}i}$, $i_{\mathrm{s,B}i}$. Since the magnetizing inductances of the transformers are neglected, all AC-side winding currents equal the leakage inductance current $i_{\mathrm{L}\sigma i}$ referred to the AC side. Furthermore, the resulting AC-side voltage sum $v_{\mathrm{p,s}i}$ with its corresponding six-pulse waveform is depicted.

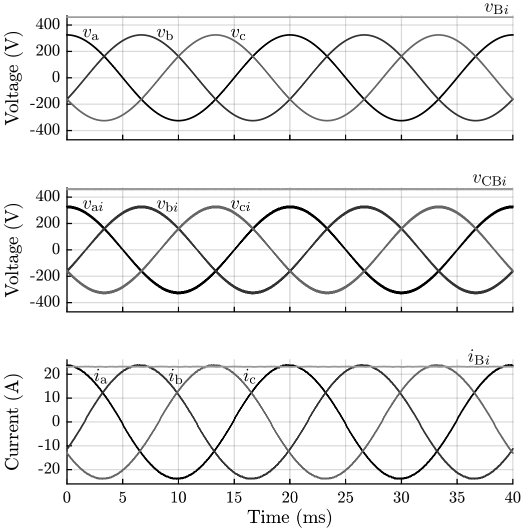


Figure 5.23: Simulated AC phase currents i_a, i_b, i_c and DC current $i_{\mathrm{B}i}$ of the AC-DC multi-port module (see **Fig. 5.2**) with the parameters given in **Tab. 5.4** applying the ZVS modulation for the reference values $I^*_\mathrm{abc} = 16\,\mathrm{A}$, $\phi^*_\mathrm{abc} = 0$ in AC-to-DC operation. The module voltages $v_{\mathrm{a}i}$, $v_{\mathrm{b}i}$, $v_{\mathrm{c}i}$ represent the voltages across the series connection of the two capacitors C_ac in each phase. $v_{\mathrm{CB}i}$ is the voltage across the DC capacitor C_dc.

Additionally, the zoom of **Fig. 5.24** is given in **Fig. 5.25** where the actual MF voltage signals applied to the transformer windings and the resulting leakage inductance current are depicted. The transformer current $i_{\mathrm{L}\sigma i}$ is shaped by the MF voltages $v_{\mathrm{p,s}i}$ and $v_{\mathrm{s,B}i}$ in such a way, that at every switching instant ZVS can be achieved. The simulated waveforms validate the theoretical ones previously shown in **Fig. 5.13**. Compared to the fundamental phasor modulation, the leakage inductance current $i_{\mathrm{L}\sigma i}$ can be controlled to allow ZVS and to also reduce the LF current distortion.

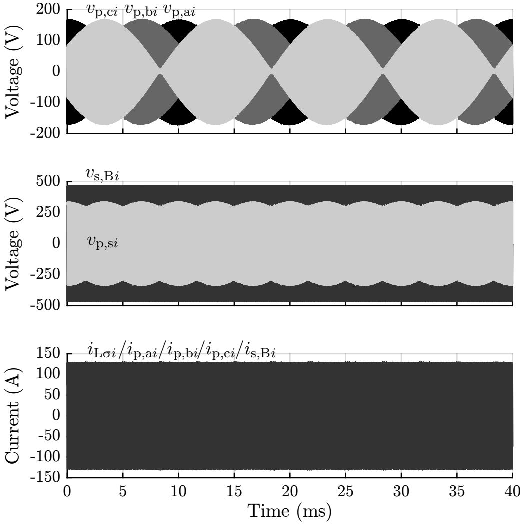


Figure 5.24: Simulated voltages $v_{\mathrm{p,a}i}$, $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$, $v_{\mathrm{s,B}i}$ across the transformer windings, resulting AC-side voltage sum $v_{\mathrm{p,s}i}$ and transformer winding currents $i_{\mathrm{p,a}i}$, $i_{\mathrm{p,b}i}$, $i_{\mathrm{p,c}i}$, $i_{\mathrm{s,B}i}$ of the AC-DC multi-port module (see **Fig. 5.2**) with the parameters given in **Tab. 5.4** applying the ZVS modulation for the reference values $I^*_{\mathrm{abc}} = 16\,\mathrm{A}$, $\phi^*_{\mathrm{abc}} = 0$ in AC-to-DC operation.

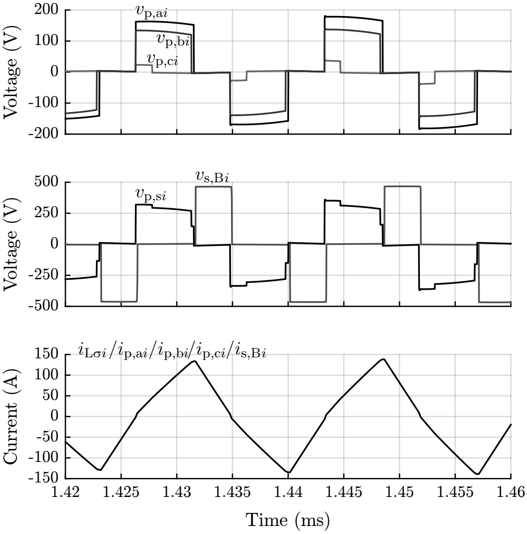


Figure 5.25: Zoom of **Fig. 5.24** with the simulated voltages $v_{\mathrm{p,a}i}$, $v_{\mathrm{p,b}i}$, $v_{\mathrm{p,c}i}$, $v_{\mathrm{s,B}i}$ across the transformer windings, resulting AC-side voltage sum $v_{\mathrm{p,s}i}$ and transformer winding currents $i_{\mathrm{p,a}i}$, $i_{\mathrm{p,b}i}$, $i_{\mathrm{p,c}i}$, $i_{\mathrm{s,B}i}$ of the AC-DC multi-port module (see **Fig. 5.2**) with the parameters given in **Tab. 5.4** applying the ZVS modulation for the reference values $I^*_{\mathrm{abc}} = 16\,\mathrm{A}, \phi^*_{\mathrm{abc}} = 0$ in AC-to-DC operation.

5.8 Summary and conclusion

In this chapter, a new cascaded AC-DC multi-port converter for battery energy storage systems is introduced. The topology is derived from state-of-the-art DC-DC multi-port converters in order to integrate module-level galvanic isolation and to provide bidirectional power flow capability. Each converter module consists of three AC ports for the three different phases and one DC port to attach a storage battery pack. The AC ports belonging to the same phase are connected in series to distribute the AC phase voltage among the converter modules.

The developed module topology allows the summation of the AC-side winding voltages by applying either three two-winding transformers with the DC-side windings electrically connected in series or a four-winding transformer with the AC-side windings magnetically connected in parallel. In this way, a three-phase AC port is formed by the series connection of the AC ports belonging to the three different phases, so that an approximately constant sum of the half-cycle voltage-second products applied to the AC-side windings becomes available for control. Since the series connection of the AC port windings lead to clamping intervals varying in a wide range depending on the instantaneous phase current/power, the use of T-type blocks at the AC side is advantageous as the conduction losses caused by the circulating current flowing through all ports (three AC and one DC port) can be reduced with the use of semiconductor devices rated for a lower blocking voltage in the clamping switch (lower on-state resistance) compared to the devices in the half-bridge.

Moreover, the operating principle on module as well as on system level is briefly explained. The AC-DC multi-port modules are modeled by their three capacitive AC voltage ports consisting of the series connection of two filter capacitors and a controlled current source in parallel. By adjusting the power transfer at an AC port of the multi-port module, the current sources are controlled in order to regulate the AC port module voltages and therefore the grid current. By controlling the AC port module voltages, also the power distribution among the AC ports in the same phase is set since all AC ports in a phase string are connected in series and exhibit the same module current.

For designing and controlling a multi-port converter system, the mathematical description of the power flows depending on the control variables is essential. With the well-known approach using piecewise linear equations for the transformer leakage inductance current, several mathematical cases depending on the phase shifts and the clamping intervals have to be distinguished. Due to the mathematical complexity, especially for high port numbers, a new modeling approach is introduced by using basic superposition principles to find general analytical formulas for the power flows. With this approach, there is no need for a mathematical distinction of cases.

For the AC-DC multi-port module, two different modulation schemes are developed. A first one is based on a simple fundamental wave model of the MF square-wave voltages applied to the transformer windings where higher order harmonics are neglected. An analytical calculation scheme is established for determining the control variables in terms of phase shifts and clamping intervals. The main drawbacks induced are the LF harmonic phase current distortions as well as the lack of soft-switching conditions at every switching instant since the transformer leakage inductance current is not actively shaped. To overcome these drawbacks, a second modulation scheme based on the introduced general power flow equations considering also ZVS conditions is developed. The control variables are first determined numerically by implementing an optimization for minimizing the transformer leakage inductance RMS current under ZVS constraints. The results obtained numerically show a structure that can be also modeled by analytic equations which is presented in a second step.

Furthermore, a design example of a 10 kW AC-DC multi-port module is presented with the components and losses described by state-of-the-art models for evaluating the theoretical efficiencies that could be reached. The design example predicts a peak efficiency of around 91.7 % at an output power of 10 kW and a battery voltage of 380 V. The estimated power density is around 2.5 kW/L. With the series connection of all ports given through the module topology, the conduction losses caused by the circulating current substantially decrease the achievable efficiency. In general, a relatively large chip area is required at the AC side (the design example uses three MOSFET devices in parallel).

For validating the theoretical aspects of the developed modulation schemes, the AC-DC multi-port module is simulated with the modulation schemes implemented as part of the simulation model. The obtained simulation curves conform to the developed mathematical models for the modulation schemes and show the feasibility of their implementation by using LUTs precalculated offline. For the fundamental phasor modulation the LF harmonic distortions of the AC phase currents can be clearly seen whereas in case of the ZVS modulation the harmonic distortion of the AC current waveforms is substantially decreased.

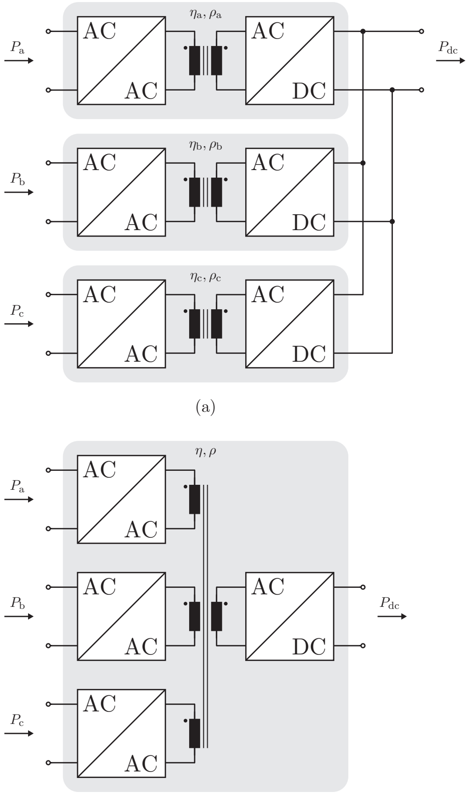
6

Multi-Objective Optimization and Comparison

After proposing and investigating two different bidirectional isolated AC-DC converter systems for battery energy storage systems on system as well as on module level, this chapter deals with the multi-objective optimization and final comparison of the considered converter systems. The power components and the associated losses are modeled in the electric, magnetic and thermal domain and comprehensive converter optimizations are carried out for

- the single-stage AC-DC dual active bridge (DAB) module,
- the single-stage AC-DC multi-port module,
- the conventional two-stage AC-DC H-bridge module connected to a DC-DC dual active bridge (DAB).

The optimization and comparison covers the single-stage AC-DC DAB module and the two-stage AC-DC H-bridge module connected to a DC-DC DAB as single-phase converter systems whereas the single-stage AC-DC multi-port module represents a three-phase converter system. To compare the single-phase converters with the three-phase converter, equivalent three-phase modules as a combination of three single-phase modules by paralleling their DC outputs are considered as depicted in **Fig. 6.1**.


η_a, ρ_a
P_a
AC
AC
AC
DC
P_{dc}
η_b, ρ_b
P_b
η_c, ρ_c
P_c
η, ρ

(a)

(b)

Figure 6.1: Three single-phase AC-DC converter modules (exemplarily shown for a single-stage solution) extended to a three-phase AC-DC converter module by paralleling their DC outputs (a) and a three-phase AC-DC converter module based on the multi-port approach (b).

The AC input power is assumed to be equal for all three phases with

$$P_{ph} = P_a = P_b = P_c. \tag{6.1}$$

Furthermore, with equally built single-phase modules the volume per phase is given by

$$V_{ph} = V_a = V_b = V_c. \tag{6.2}$$

The DC output power of the three-phase module consisting of single-phase modules (see **Fig. 6.1(a)**) with a given phase input power and efficiency is expressed as

$$P_{\mathrm{dc}} = \eta_{\mathrm{a}} P_{\mathrm{a}} + \eta_{\mathrm{b}} P_{\mathrm{b}} + \eta_{\mathrm{c}} P_{\mathrm{c}}. \tag{6.3}$$

Considering single-phase modules with an equal AC input power and equal efficiencies

$$\eta = \eta_{\mathrm{a}} = \eta_{\mathrm{b}} = \eta_{\mathrm{c}} \tag{6.4}$$

the DC power can be rewritten as

$$P_{\mathrm{dc}} = \eta(P_{\mathrm{a}} + P_{\mathrm{b}} + P_{\mathrm{c}}) = 3\eta P_{\mathrm{ph}} \tag{6.5}$$

with η being the efficiency of an equivalent three-phase system. In a similar way, the DC output power of combined single-phase modules can be formulated depending on their volume and their power density as

$$P_{\mathrm{dc}} = \rho_{\mathrm{a}} V_{\mathrm{a}} + \rho_{\mathrm{b}} V_{\mathrm{b}} + \rho_{\mathrm{c}} V_{\mathrm{c}}. \tag{6.6}$$

Assuming an equal volume as well as an equal power density for all single-phase modules with

$$\rho = \rho_{\mathrm{a}} = \rho_{\mathrm{b}} = \rho_{\mathrm{c}} \tag{6.7}$$

the DC power can be represented as

$$P_{\mathrm{dc}} = \rho(V_{\mathrm{a}} + V_{\mathrm{b}} + V_{\mathrm{c}}) = 3\rho V_{\mathrm{ph}} \tag{6.8}$$

with ρ being the power density of an equivalent three-phase system. Provided that the single-phase modules with their properties stated above are combined to an equivalent three-phase module as depicted in **Fig. 6.1(a)**, the following optimization can be carried out for comparing single-phase to three-phase converter modules in terms of efficiency and power density.

6.1 Specifications of converter modules

The converter modules considered for the multi-objective optimization are the single-stage AC-DC DAB module from Chapter 4 depicted in **Fig. 6.2**, the single-stage AC-DC multi-port module from Chapter 5 depicted in **Fig. 6.4** and the conventional two-stage AC-DC H-bridge module connected to a DC-DC DAB depicted in **Fig. 6.3** which represents a state-of-the-art implementation of the galvanic isolation on module level in a cascaded H-bridge converter (CHB).

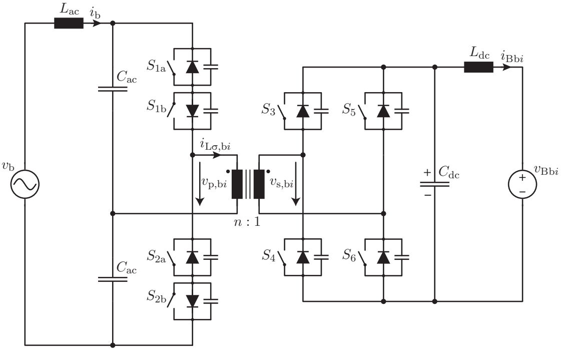

L_{ac}
i_{b}
$S_{1\mathrm{a}}$
C_{ac}
$S_{1\mathrm{b}}$
L_{dc}
$i_{\mathrm{B}bi}$
S_3
S_5
$i_{\mathrm{L}\sigma,\mathrm{b}i}$
v_{b}
$v_{\mathrm{p,b}i}$
$v_{\mathrm{s,b}i}$
+
C_{dc}
−
$v_{\mathrm{B}bi}$
+
−
$n:1$
$S_{2\mathrm{a}}$
C_{ac}
S_4
S_6
$S_{2\mathrm{b}}$

Figure 6.2: Single-stage AC-DC DAB converter module applying a grid-side half-bridge with bidirectional switches, a battery-side full-bridge with unidirectional switches and a medium-frequency transformer providing the galvanic isolation. The AC voltage v_{b} corresponds to the sinusoidal grid voltage waveform.

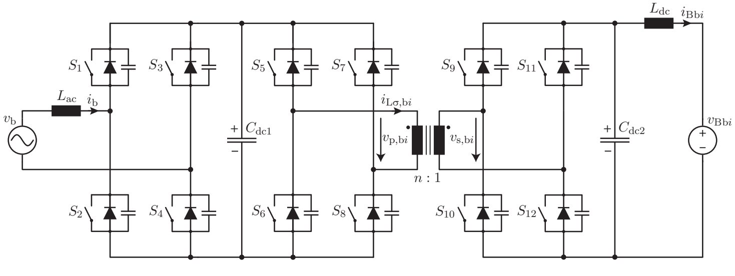

L_{dc}
$i_{\mathrm{B}bi}$
S_1
S_3
S_5
S_7
S_9
S_{11}
L_{ac}
i_{b}
$i_{\mathrm{L}\sigma,\mathrm{b}i}$
v_{b}
+
C_{dc1}
−
$v_{\mathrm{p,b}i}$
$v_{\mathrm{s,b}i}$
+
C_{dc2}
−
$v_{\mathrm{B}bi}$
+
−
$n:1$
S_2
S_4
S_6
S_8
S_{10}
S_{12}

Figure 6.3: Two-stage converter module consisting of an AC-DC H-bridge module with unidirectional switches connected to a DC-DC DAB converter with a primary and a secondary full-bridge for providing the galvanic isolation. The AC voltage v_{b} corresponds to the sinusoidal grid voltage waveform.

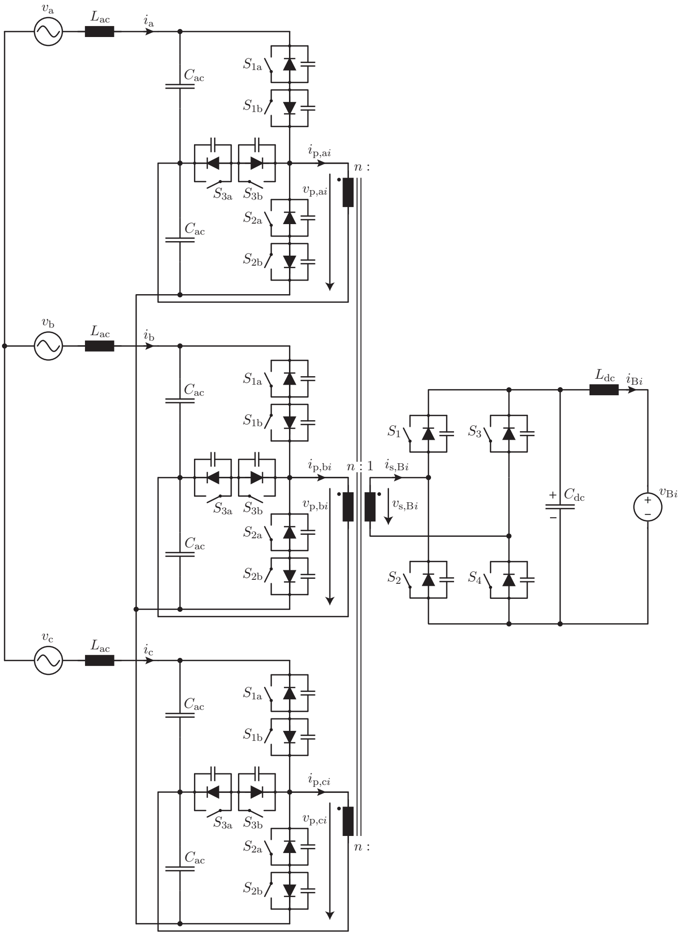

v_a
L_ac
i_a
S_1a
C_ac
S_1b
$i_{\mathrm{p,a}i}$
$n:$
S_3a
S_3b
$v_{\mathrm{p,a}i}$
S_2a
S_2b
v_b
i_b
$i_{\mathrm{p,b}i}$
$n:1$
$i_{\mathrm{s,B}i}$
$v_{\mathrm{p,b}i}$
$v_{\mathrm{s,B}i}$
L_dc
$i_{\mathrm{B}i}$
S_1
S_3
S_2
S_4
C_dc
$v_{\mathrm{B}i}$
v_c
i_c
$i_{\mathrm{p,c}i}$
$v_{\mathrm{p,c}i}$

Figure 6.4: Single-stage AC-DC multi-port converter module applying grid-side T-type blocks with bidirectional switches, a battery-side full-bridge with unidirectional switches and a four-winding medium-frequency transformer providing the galvanic isolation. The AC voltages v_a, v_b, v_c correspond to the sinusoidal grid voltage waveforms.

For the AC-DC DAB module, the ZVS modulation with variable switching frequency as discussed in Section 4.3.2 is applied whereas for the AC-DC multi-port module, the ZVS modulation presented in Section 5.5.2 is considered. For both converter modules, the control variables are derived by the proposed optimization procedures covered in the corresponding sections.

The AC-DC H-bridge module in the conventional two-stage approach is operated by a state-of-the-art three-level carrier based pulse width modulation (PWM). For the connected DC-DC DAB converter at the DC link, the standard phase shift modulation is considered as this modulation scheme allows a high efficiency at a relatively high power density.

For the comparison of the module types, the AC mains voltage is fixed at 230 V, 50 Hz, the battery voltage and the DC link voltage in the two-stage system is assumed to be 400 V. With a reference phase current of 16 A, the AC-DC DAB module, the AC-DC H-bridge module and the DC-DC DAB converter are operated at an input power of 3.68 kW. The AC-DC multi-port module is connected to a three-phase voltage system, so that an input power of 11.04 kW results.

The passive filter components in terms of the inductors L_{ac}, L_{dc} and the capacitors C_{ac}, C_{dc}, C_{dc1}, C_{dc2} are dimensioned during the optimization procedure to guarantee peak-to-peak voltage ripples below 5 % and peak-to-peak current ripples below 2.5 %. With these specifications, the input and output currents of all module types fulfill the same current ripple limits. The implemented modulation schemes further ensure that low order current harmonics at the AC side are kept low. The

Table 6.1: Specifications of the converter modules for the multi-objective optimization and comparison.

Mains voltage	V_{a}, V_{b}, V_{c}	230 V
Mains frequency	f_{a}, f_{b}, f_{c}	50 Hz
Battery voltage	$V_{\mathrm{Bb}i}$, $V_{\mathrm{B}i}$	400 V
DC link voltage	V_{dc1}	400 V
Reference phase current	I_{a}, I_{b}, I_{c}	16 A
Transformer turns ratio	n	1
Capacitor voltage ripple	$v_{\mathrm{ac,pp}}$, $v_{\mathrm{dc,pp}}$, $v_{\mathrm{dc1,pp}}$, $v_{\mathrm{dc2,pp}}$	5 %
Inductor current ripple	$i_{\mathrm{a,pp}}$, $i_{\mathrm{b,pp}}$, $i_{\mathrm{c,pp}}$, $i_{\mathrm{Bb}i\mathrm{,pp}}$, $i_{\mathrm{B}i\mathrm{,pp}}$	2.5 %
Ambient temperature	T_{a}	40 °C

specifications of the converter modules are summarized in **Tab. 6.1**.

The implemented optimization uses discrete semiconductor devices with the total number of devices per converter power limited to a maximum for a reasonable comparison of single-phase and three-phase converter modules. The optimization procedure varies the number of parallel switching devices as shown later in Section 6.3 until the maximum chip area for the converter module is reached.

6.2 Modeling of power components

For the multi-objective optimization and comparison of the converter modules in terms of efficiency and power density, the modeling of the power components is an important prerequisite. In the following, the applied models of the semiconductor devices, the inductive components like inductors and transformers as well as the capacitors are given. A multi-domain modeling approach is chosen which considers the electric, magnetic and thermal domain.

6.2.1 Semiconductor devices

The semiconductor model uses a discrete reference MOSFET for the operation under ZVS conditions in the single-stage converter modules and a discrete reference IGBT operated under hard-switching conditions for the H-bridge in the two-stage converter module. The selected reference devices are

- the 650 V MOSFET IPW65R019C7 from Infineon [165] in a TO-247 package,
- the 650 V IGBT IKW50N65F5 with an antiparallel diode from Infineon [166] in a TO-247 package,

both from the same voltage class with a comparable low on-state resistance and a low collector-emitter saturation voltage respectively.

The conduction and switching losses are calculated based on data sheet parameters with the loss models given in Section B.1.1 for IGBTs and in Section B.1.2 for MOSFETs. The gate drive losses are modeled according to Section B.1.3.

For the semiconductor devices, a forced convection cooling system with a cooling system performance index (CSPI) of 15 W/(K·dm^3) [167]

is assumed. The junction temperatures T_j are supposed to be 125 °C for the MOSFETs and 150 °C for the IGBTs. These temperatures are 25 °C below the maximum junction temperatures allowed by the manufacturer.

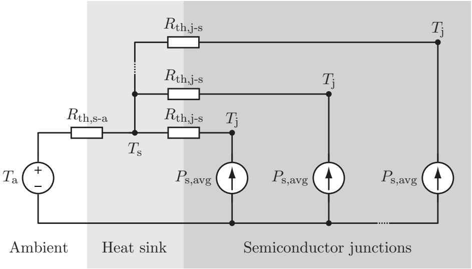

$R_\mathrm{th,j\text{-}s}$
T_j
$R_\mathrm{th,j\text{-}s}$
T_j
$R_\mathrm{th,s\text{-}a}$
$R_\mathrm{th,j\text{-}s}$
T_j
T_s
T_a
$P_\mathrm{s,avg}$
$P_\mathrm{s,avg}$
$P_\mathrm{s,avg}$
Ambient
Heat sink
Semiconductor junctions

Figure 6.5: Thermal model of the forced convection cooling system for the semiconductor devices considered in the optimization process. $P_\mathrm{s,avg}$ represents the average losses per semiconductor device.

The determination of the heat sink volume is done by solving the thermal model shown in **Fig. 6.5**. First, the heat sink temperature T_s is calculated with

$$T_\mathrm{s} = T_\mathrm{j} - R_\mathrm{th,j\text{-}s} P_\mathrm{s,avg} \tag{6.9}$$

with the average power loss $P_\mathrm{s,avg}$ per semiconductor device and a thermal resistance junction-to-sink

$$R_\mathrm{th,j\text{-}s} = \frac{R_\mathrm{th,j\text{-}s,Anom}}{A_\mathrm{chip}} \tag{6.10}$$

applying the data sheet study from [168] with a nominal junction-to-sink resistance of $R_\mathrm{th,j\text{-}s,Anom} = 30\,\mathrm{K/(W{\cdot}mm^2)}$. The chip area A_chip is approximated by the mounting area of a TO-247 case. The thermal resistance sink-to-ambient is then given by

$$R_\mathrm{th,s\text{-}a} = \frac{T_\mathrm{s} - T_\mathrm{a}}{\sum P_\mathrm{s,avg}}, \tag{6.11}$$

so that the heat sink volume can be determined depending on the assumed CSPI with

$$V_\mathrm{s} = \frac{1}{\mathrm{CSPI} \cdot R_\mathrm{th,s\text{-}a}}. \tag{6.12}$$

6.2.2 Inductive components

The inductive components in terms of an inductor or a transformer are both modeled with E-cores where the geometry is varied to find the Pareto optimal points. The introduced geometry parameters are the dimensions a_c, b_c, c_c, d_c (see **Fig. 6.6(a)**) with their limits given by

$$b_\mathrm{c} \in [10\,\mathrm{mm}, 50\,\mathrm{mm}]\,, \tag{6.13}$$

$$d_\mathrm{c} \in [b_\mathrm{c}, 2b_\mathrm{c}]\,, \tag{6.14}$$

$$a_\mathrm{c} \in [2b_\mathrm{c} + 10\,\mathrm{mm}, 6b_\mathrm{c}]\,, \tag{6.15}$$

$$c_\mathrm{c} \in [10\,\mathrm{mm}, 2b_\mathrm{c}]\,. \tag{6.16}$$

The core material considered for the inductive components are

- the Kool Mu 26u material (powder cores) from Magnetics [155] for the inductors with the maximum allowable flux density set to $B_\mathrm{max} = 1\,\mathrm{T} \cdot 60\,\%$,
- the nanocrystalline VITROPERM 500F material from VACUUMSCHMELZE [151] for the transformers with the maximum allowable flux density set to $B_\mathrm{max} = 1.2\,\mathrm{T} \cdot 60\,\%$.

Powder cores with a distributed air gap are ideally suited for the inductors since no additional air gap has to be introduced in the E-core which would result in undesirable additional winding losses caused by the fringing magnetic field. The VITROPERM 500F material exhibits a high relative permeability of around $\mu_\mathrm{r} = 20\,000$ [151] (around a factor of 10 higher than ferrite) which allows to build a transformer with a comparable high magnetizing inductance. This is especially advantageous for DAB based converter systems since the derivation of the modulation schemes usually neglect the magnetizing inductance of the transformer.

Besides the variation of the core dimensions, the number of turns of a (primary) winding is iterated within the limits

- $N_\mathrm{w} \in [5, 20]$ for the filter inductors L_ac, L_dc,

- $N_{\mathrm{w}} \in [5, 200]$ for the boost inductance L_{ac} in the H-bridge module because of the high inductance values required for the given AC current ripple specification (see **Tab. 6.1**),
- $N_{\mathrm{w1}} \in [5, 20]$ for the two- as well as the four-winding transformer in the AC-DC DAB, the AC-DC multi-port and the DC-DC DAB module.

In case of a transformer, the number of turns of the secondary winding is given by the fixed transformer turns ratio n and can be calculated as $N_{\mathrm{w2}} = \frac{N_{\mathrm{w1}}}{n}$.

For the windings, litz wire is assumed in order to reduce skin and proximity effect losses compared to solid round wire and to allow a better mechanical assembly due to the flexibility of the wire. The optimization considers a discrete selection of litz wire windings with any combination of

- strand diameters 0.071 mm, 0.1 mm, 0.125 mm, 0.2 mm [169],
- number of strands 500, 1000, 1500, 2000.

The current density per strand is limited to $J_{\max} = 4\,\mathrm{A/mm^2}$ by the optimization procedure.

Inductor

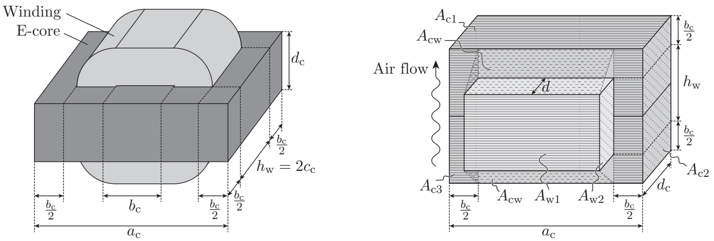
The 3D drawing of the inductor considered in the optimization is given in **Fig. 6.6(a)** with the relevant surface areas for free convection cooling depicted in **Fig. 6.6(b)**.

The inductance value L can be determined with the reluctance model shown in **Fig. 6.7** as

$$L = \frac{N_{\mathrm{w}}^2}{R_{\mathrm{m}}} = \frac{N_{\mathrm{w}}^2}{\frac{l_{\mathrm{m}}}{\mu_0 \mu_{\mathrm{m}} A_{\mathrm{e}}}} \tag{6.17}$$

with N_{w} being the number of turns, A_{e} the core cross section area and μ_{m} the relative permeability of the core material. The mean magnetic length l_{m} is given by

$$l_{\mathrm{m}} = a_{\mathrm{c}} + 2h_{\mathrm{w}}. \tag{6.18}$$


Winding
E-core
d_c
$\frac{b_c}{2}$
$h_w = 2c_c$
$\frac{b_c}{2}$
b_c
$\frac{b_c}{2}$
a_c
A_{c1}
A_{cw}
Air flow
d
$\frac{b_c}{2}$
h_w
$\frac{b_c}{2}$
A_{c2}
d_c
A_{c3}
A_{cw}
A_{w1}
A_{w2}
$\frac{b_c}{2}$
$\frac{b_c}{2}$
a_c

(a) (b)

Figure 6.6: 3D drawing of the inductor considered for the optimization and the module comparison with the dimensions of the geometry labeled in (a) and the relevant surface areas for free convection cooling shaded in (b) which are used in the thermal model for the inductor.

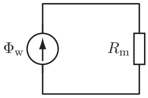


Figure 6.7: Reluctance model of the inductor considered in the optimization process for determining the core losses. The flux source Φ_w represents the flux in the core driven by the winding current i_w.

The core losses are calculated by using the improved generalized Steinmetz equation (iGSE) as given in Section B.2.2, the Steinmetz parameters are obtained from the material curves provided by the manufacturer [155]. With the reluctance model depicted in **Fig. 6.7**, the flux in the core excited by the winding current is given by

$$\Phi_w = \frac{L}{N_w} i_w, \tag{6.19}$$

so that the iGSE can be applied for the reluctance R_m. The inductance value L is assumed to be constant which requires the operation of the inductor in the linear region of the core material.

The skin and proximity effect losses in the litz wire for each current harmonic are calculated according to Section B.2.1 with a 1D magnetic field approximation.

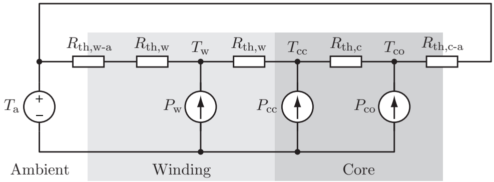


Figure 6.8: Thermal model of the inductor (see **Fig. 6.6**) considered in the optimization process. P_{w} are the winding losses, P_{cc} are the core losses in the core volume covered by the winding and P_{co} are the core losses in the core volume that is exposed to the air.

Fig. 6.8 shows the thermal model of the inductor considered in the optimization process with the winding losses P_{w}, the covered core losses P_{cc} and the core losses P_{co} in the volume exposed to the air. $R_{\text{th,rad}}$ and $R_{\text{th,tan}}$ are the distributed thermal resistances in the radial and the tangential direction of the winding according to [170]. For the sake of simplicity, the litz wire is thermally modeled like a solid round conductor. The detailed equations for the radial and tangential resistances are given in [170] which are then connected in parallel to obtain the thermal winding resistance

$$R_{\text{th,w}} = \frac{1}{2}\frac{R_{\text{th,rad}}R_{\text{th,tan}}}{R_{\text{th,rad}} + R_{\text{th,tan}}}\frac{n_{\text{L}}}{n_{\text{T}}} \tag{6.20}$$

with n_{L} being the number of layers and n_{T} the number of turns per layer. The thermal resistance of the core is given by

$$R_{\text{th,c}} = \frac{1}{4}\frac{b_{\text{c}} + h_{\text{w}} + \frac{a_{\text{c}}-2b_{\text{c}}}{2}}{\lambda_{\text{c}}\frac{A_{\text{e}}}{2}} \tag{6.21}$$

with the thermal conductivity of the Kool Mu material $\lambda_{\text{c}} = 80\,\text{W/(K·m)}$ [171]. With the assumption of free convection cooling, the thermal transfer resistance between the winding and the ambient is given by

$$R_{\text{th,w-a}} = \frac{1}{\alpha_{\text{c}}A_{\text{w}}} \tag{6.22}$$

and the thermal transfer resistance between the core and the ambient by

$$R_{\text{th,c-a}} = \frac{1}{\alpha_{\text{c}}A_{\text{c}}}. \tag{6.23}$$

The relevant surface areas A_w, A_c where the cooling air is flowing along (see **Fig. 6.6(b)**) for the winding and the core can be determined as

$$\begin{aligned} A_\mathrm{w} &= 2\left(A_\mathrm{w1} + 2A_\mathrm{w2} + 2\frac{A_\mathrm{cw}}{2}\right) \\ &= 2\left(h_\mathrm{w}(a_\mathrm{c} - b_\mathrm{c}) + 2h_\mathrm{w}d + (a_\mathrm{c} - b_\mathrm{c})\sqrt{\left(\frac{b_\mathrm{c}}{2}\right)^2 + d^2}\right) \end{aligned} \tag{6.24}$$

and

$$\begin{aligned} A_\mathrm{c} &= 2A_\mathrm{c1} + 2A_\mathrm{c2} + 2\left(2A_\mathrm{c3} + 2\frac{A_\mathrm{cw}}{2}\right) \\ &= 2a_\mathrm{c}d_\mathrm{c} + 2(h_\mathrm{w} + b_\mathrm{c})d_\mathrm{c} \\ &\quad + 2\left(2(h_\mathrm{w} + b_\mathrm{c})\frac{b_\mathrm{c}}{2} + (a_\mathrm{c} - b_\mathrm{c})\sqrt{\left(\frac{b_\mathrm{c}}{2}\right)^2 + d^2}\right). \end{aligned} \tag{6.25}$$

A heat transfer coefficient of $\alpha_\mathrm{c} = 10\,\mathrm{W/(K{\cdot}m^2)}$ for free convection cooling [172] is considered in the optimization.

The heat source P_w in **Fig. 6.8** represents the total losses occurring in the winding. The core losses are split into the part P_cc occurring in the volume covered by the winding and the remaining part P_co which describes the losses in the core volume that is exposed to the air. The heat sources in the core are then given by

$$P_\mathrm{cc} = \frac{V_\mathrm{cc}}{V_\mathrm{cc} + V_\mathrm{co}} P_\mathrm{c}, \tag{6.26}$$

$$P_\mathrm{co} = \frac{V_\mathrm{co}}{V_\mathrm{cc} + V_\mathrm{co}} P_\mathrm{c} \tag{6.27}$$

with the total core losses P_c and the core volumes

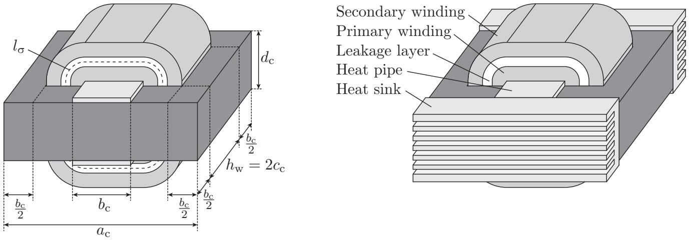
$$V_\mathrm{cc} = b_\mathrm{c} h_\mathrm{w} d_\mathrm{c}, \tag{6.28}$$

$$V_\mathrm{co} = a_\mathrm{c}(b_\mathrm{c} + h_\mathrm{w})d_\mathrm{c}. \tag{6.29}$$

For every calculation of the thermal model, the temperatures T_w, T_cc, T_co (see **Fig. 6.8**) are evaluated. If these temperatures exceed the limit of $T_\mathrm{max} = 90\,^\circ\mathrm{C}$, the design point is determined to be not feasible and discarded by the optimization.

Two-winding transformer

The 3D drawing of the two-winding transformer considered in the optimization is given in **Fig. 6.9(a)** with heat sinks mounted for forced convection cooling depicted in **Fig. 6.9(b)**. An additional heat pipe is inserted on the top and the bottom of the core for a sufficient heat removal in the primary winding and in the covered core volume.



(a) (b)

Figure 6.9: 3D drawing of the two-winding transformer considered for the optimization and the module comparison with the dimensions of the geometry labeled in (a) and the final assembly shown in (b) including heat sinks.

The leakage inductance value L_σ is adjusted by the distance between the primary and the secondary winding with a leakage layer in between. The dimensioning is done at the maximum power point according to (4.72) for the AC-DC DAB module (peak power of 7.36 kW) and at a 20 % phase shift for the DC-DC DAB converter in the two-stage module (constant power of 3.68 kW). The value of the leakage inductance itself depending on the geometry is calculated with the magnetic energy stored in the windings and the leakage layer as described by (5.98)-(5.102) for a four-winding transformer.

The core losses are calculated by using the iGSE as given in Section B.2.2, the Steinmetz parameters are obtained from the material curves provided by the manufacturer [151]. With the reluctance model depicted in **Fig. 6.10**, the flux in the core excited by the voltages v_{w1}, v_{w2} applied to the windings are given by

$$\Phi_{w1} = \frac{1}{N_{w1}} \int v_{w1}(t)\ dt, \tag{6.30}$$

$$\Phi_{\mathrm{w2}} = \frac{1}{N_{\mathrm{w2}}} \int v_{\mathrm{w2}}(t)\ \mathrm{d}t \tag{6.31}$$

with N_{w1}, N_{w2} being the primary and secondary number of turns. By solving the magnetic circuit shown in **Fig. 6.10**, the flux in the reluctances R_{m1}, R_{m2}, R_{σ} are determined to evaluate the associated core losses applying the iGSE.

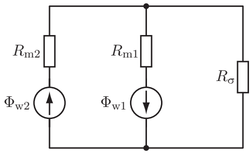

R_{m2}
R_{m1}
R_{σ}
Φ_{w2}
Φ_{w1}

Figure 6.10: Reluctance model of the two-winding transformer (see **Fig. 6.9**) considered in the optimization process for determining the core losses. The flux sources Φ_{w1}, Φ_{w2} represent the fluxes in the core impressed by the square-wave voltages v_{w1}, v_{w2} applied to the windings.

The skin and proximity effect losses in the litz wire for each current harmonic are calculated according to Section B.2.1 with a 1D magnetic field approximation.

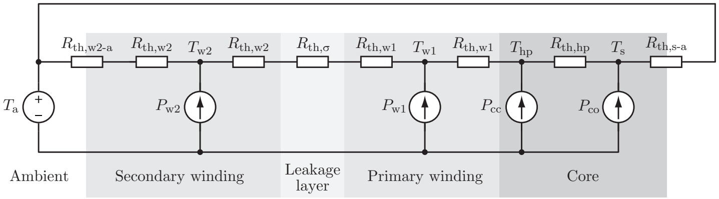

$R_{\mathrm{th,w2\text{-}a}}$
$R_{\mathrm{th,w2}}$
T_{w2}
$R_{\mathrm{th,w2}}$
$R_{\mathrm{th},\sigma}$
$R_{\mathrm{th,w1}}$
T_{w1}
$R_{\mathrm{th,w1}}$
T_{hp}
$R_{\mathrm{th,hp}}$
T_{s}
$R_{\mathrm{th,s\text{-}a}}$
T_{a}
+
−
P_{w2}
P_{w1}
P_{cc}
P_{co}
Ambient
Secondary winding
Leakage layer
Primary winding
Core

Figure 6.11: Thermal model of the two-winding transformer (see **Fig. 6.9**) considered in the optimization process. P_{w1} are the primary and P_{w2} the secondary winding losses, P_{cc} are the core losses in the core volume covered by the primary winding and P_{co} are the core losses in the core volume that is exposed to the air and the heat sinks respectively.

In **Fig. 6.11**, the thermal model of the two-winding transformer considered in the optimization process is depicted. P_{w1} are the primary winding losses, P_{w2} the secondary winding losses, P_{cc} the covered core losses and P_{co} the core losses in the volume exposed to the heat sinks and the air. The heat sources P_{cc}, P_{co} are given by (6.26)-(6.29) depending on the total core losses P_{c}.

The thermal winding resistances $R_{\mathrm{th,w1}}$, $R_{\mathrm{th,w2}}$ are determined as in the case of the inductor with (6.20) by inserting the radial and tangential resistances as described in [170]. With the thickness d_σ and the mean circumference l_σ of the leakage layer (see **Fig. 6.9**), its thermal resistance can be calculated by

$$R_{\mathrm{th},\sigma} = \frac{d_\sigma}{\lambda_\sigma l_\sigma h_{\mathrm{w}}} \tag{6.32}$$

with a thermal conductivity of $\lambda_\sigma = 0.24\,\mathrm{W/(K{\cdot}m)}$ assumed for the leakage/isolation layer [170]. The heat pipe is made out of copper with a high thermal conductivity of $\lambda_{\mathrm{Cu}} = 401\,\mathrm{W/(K{\cdot}m)}$ [170] with the thermal resistance given by

$$R_{\mathrm{th,hp}} = \frac{1}{4}\frac{\frac{h_{\mathrm{w}}+b_{\mathrm{c}}}{2}}{\lambda_{\mathrm{Cu}} b_{\mathrm{c}} h_{\mathrm{hp}}}. \tag{6.33}$$

The height of the heat pipe h_{hp} is adjusted depending on the width of the middle core leg of the E-core with

$$h_{\mathrm{hp}} = \frac{b_{\mathrm{c}}}{8}. \tag{6.34}$$

Considering the assumption of forced convection cooling of the outer winding with a heat transfer coefficient of $\alpha_{\mathrm{c}} = 40\,\mathrm{W/(K{\cdot}m^2)}$ [172], the thermal transfer resistance between the secondary winding and the ambient is given by

$$R_{\mathrm{th,w2\text{-}a}} = \frac{1}{\alpha_{\mathrm{c}} A_{\mathrm{w}}} \tag{6.35}$$

where the relevant surface area for the cooling is described by (6.24). For the heat sinks, a thermal transfer resistance of 0.4 K/W is taken into account so that

$$R_{\mathrm{th,s\text{-}a}} = \frac{1}{2}\cdot 0.4\,\mathrm{K/W}. \tag{6.36}$$

The evaluation of the thermal model shown in **Fig. 6.11** leads to the temperatures T_{w1}, T_{w2}, T_{hp}, T_{s}. If these temperatures exceed the limit of $T_{\max} = 90\,°\mathrm{C}$, the design point is determined to be not feasible and discarded by the optimization.

Four-winding transformer

The 3D drawing of the four-winding transformer considered in the optimization of the AC-DC multi-port converter module is depicted in **Fig. 6.12(a)** with heat sinks mounted for forced convection cooling depicted in **Fig. 6.12(b)**. As in the case of the two-winding transformer, an additional heat pipe is inserted on the top and the bottom of the core for each primary or AC-side winding in order to provide a sufficient heat removal in the inner windings and in the covered core volumes.

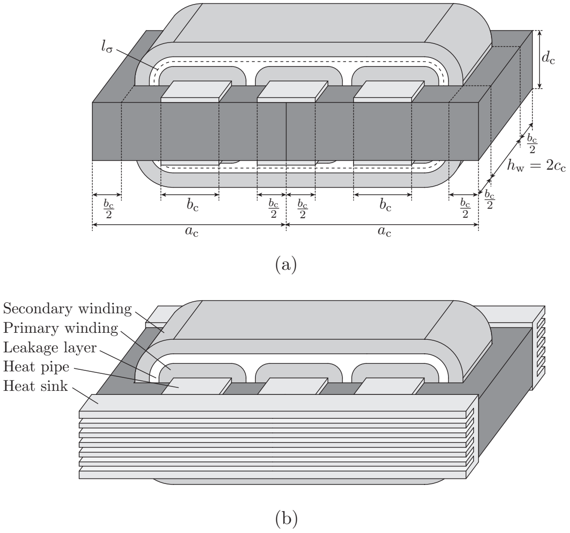

l_σ
d_c
$\frac{b_c}{2}$
$h_w = 2c_c$
$\frac{b_c}{2}$
$\frac{b_c}{2}$
b_c
$\frac{b_c}{2}$
$\frac{b_c}{2}$
b_c
$\frac{b_c}{2}$
a_c
a_c
(a)
Secondary winding
Primary winding
Leakage layer
Heat pipe
Heat sink
(b)

Figure 6.12: 3D drawing of the four-winding transformer considered for the optimization and the module comparison with the dimensions of the geometry labeled in (a) and the final assembly shown in (b) including heat sinks.

The leakage inductance value L_σ is adjusted by the distance between the primary windings and the secondary winding with a leakage layer in between. Similar to the AC-DC DAB module, the dimensioning is done at the maximum power point according to (5.96) (constant power of 11.04 kW for the three-phase module). The value of the leakage inductance depending on the geometry is calculated with the magnetic energy stored in the windings and the leakage layer with (5.98)-(5.102).

Again, the core losses are calculated by using the iGSE as summarized in Section B.2.2, the Steinmetz parameters are obtained from the material curves provided by the manufacturer [151]. With the reluctance model depicted in **Fig. 6.13**, the flux in the core excited by the voltages $v_{\mathrm{w1,a}}$, $v_{\mathrm{w1,b}}$, $v_{\mathrm{w1,c}}$, v_{w2} applied to the windings are given by

$$\Phi_{\mathrm{w1,a}} = \frac{1}{N_{\mathrm{w1}}} \int v_{\mathrm{w1,a}}(t)\ \mathrm{d}t, \tag{6.37}$$

$$\Phi_{\mathrm{w1,b}} = \frac{1}{N_{\mathrm{w1}}} \int v_{\mathrm{w1,b}}(t)\ \mathrm{d}t, \tag{6.38}$$

$$\Phi_{\mathrm{w1,c}} = \frac{1}{N_{\mathrm{w1}}} \int v_{\mathrm{w1,c}}(t)\ \mathrm{d}t, \tag{6.39}$$

$$\Phi_{\mathrm{w2}} = \frac{1}{N_{\mathrm{w2}}} \int v_{\mathrm{w2}}(t)\ \mathrm{d}t \tag{6.40}$$

with N_{w1}, N_{w2} being the primary and secondary number of turns. By solving the magnetic circuit shown in **Fig. 6.13**, the flux in the reluctances R_{m1}, R_{m2}, $R_{\sigma 1}$, $R_{\sigma 2}$ are determined to evaluate the associated core losses applying the iGSE.

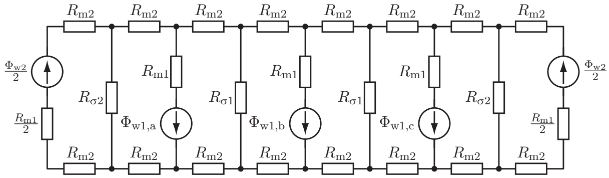


Figure 6.13: Reluctance model of the four-winding transformer (see **Fig. 6.12**) considered in the optimization process for determining the core losses. The flux sources $\Phi_{\mathrm{w1,a}}$, $\Phi_{\mathrm{w1,b}}$, $\Phi_{\mathrm{w1,c}}$, Φ_{w2} represent the fluxes in the core impressed by the square-wave voltages $v_{\mathrm{w1,a}}$ (phase a), $v_{\mathrm{w1,b}}$ (phase b), $v_{\mathrm{w1,c}}$ (phase c), v_{w2} (DC side) applied to the windings.

Again, the skin and proximity effect losses in the litz wire for each current harmonic are calculated according to Section B.2.1 with a 1D magnetic field approximation.

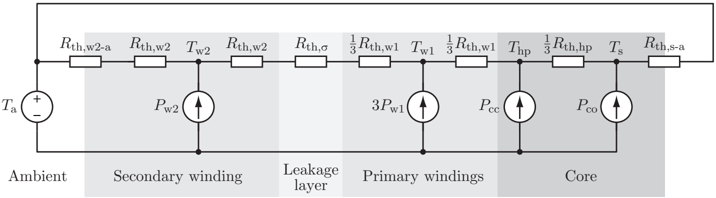

$R_{\mathrm{th,w2\text{-}a}}$
$R_{\mathrm{th,w2}}$
T_{w2}
$R_{\mathrm{th,w2}}$
$R_{\mathrm{th},\sigma}$
$\frac{1}{3}R_{\mathrm{th,w1}}$
T_{w1}
$\frac{1}{3}R_{\mathrm{th,w1}}$
T_{hp}
$\frac{1}{3}R_{\mathrm{th,hp}}$
T_{s}
$R_{\mathrm{th,s\text{-}a}}$
T_{a}
P_{w2}
$3P_{\mathrm{w1}}$
P_{cc}
P_{co}
Ambient
Secondary winding
Leakage layer
Primary windings
Core

Figure 6.14: Thermal model of the four-winding transformer (see **Fig. 6.12**) considered in the optimization process. $3P_{\mathrm{w1}}$ are the primary and P_{w2} the secondary winding losses, P_{cc} are the core losses in the core volume covered by the primary windings and P_{co} are the core losses in the core volume that is exposed to the air and the heat sinks respectively.

Fig. 6.14 shows the thermal model of the four-winding transformer considered in the optimization process with the winding losses P_{w1} per primary winding, the secondary winding losses P_{w2}, the covered core losses P_{cc} and the core losses P_{co} in the volume exposed to the heat sinks and the air. The heat sources P_{cc}, P_{co} are given by (6.26)-(6.27) depending on the total core losses P_{c}.

The thermal resistances of the windings $R_{\mathrm{th,w1}}$, $R_{\mathrm{th,w2}}$ are calculated as in the case of the inductor with (6.20) by inserting the radial and tangential resistances as presented in [170]. To account for the three primary windings, the total effective thermal resistance from temperature T_{w1} to temperature T_{hp} is reduced to $\frac{1}{3}R_{\mathrm{th,w1}}$ as shown in **Fig. 6.14**. The thermal resistances $R_{\mathrm{th},\sigma}$, $R_{\mathrm{th,hp}}$ can be calculated in the same way as for the two-winding transformer by applying (6.32)-(6.34). For the thermal resistance of the leakage layer, the heat flow between the primary windings through the leakage layer is neglected as the contribution to the heat removal is rather low, so that the circumference l_σ can be approximated along the outer winding as depicted in **Fig. 6.12(a)**. The thermal transfer resistance from the secondary winding to the ambient $R_{\mathrm{th,w2\text{-}a}}$ is again given by (6.35) with a heat transfer coefficient of $\alpha_{\mathrm{c}} = 40\,\mathrm{W/(K{\cdot}m^2)}$ [172] and the resistance from the heat sink to the ambient $R_{\mathrm{th,s\text{-}a}}$ by (6.36).

With the calculation of the thermal model depicted in **Fig. 6.14**, the temperatures T_{w1}, T_{w2}, T_{hp}, T_{s} are determined. If these temperatures exceed the limit of $T_{\mathrm{max}} = 90\,°\mathrm{C}$, the design point is marked to be not feasible and discarded by the optimization.

6.2.3 Capacitors

For the converter modules, ceramic capacitors are considered as they allow to reach a high power density, can be used for AC and DC applications and exhibit a comparable low equivalent series resistance (ESR). By paralleling ceramic capacitors, the medium- to high-frequency currents occurring in DAB based converter systems and the associated power losses are distributed among the components what simplifies also the heat removal.

The optimization applies reference capacitors from Syfer [156] with a X7R dielectric considering a constant capacitance derating of 40 % as a worst-case scenario. The considered components are

- the 250 V, 1 µF ceramic capacitor with a maximum power dissipation of 350 mW for the AC-side capacitors,
- the 630 V, 1 µF ceramic capacitor with a maximum power dissipation of 400 mW for the DC-side capacitors.

The lower limit for the number of paralleled capacitors is either given by the maximum current and the induced power dissipation per component or the target capacitance value that has to be reached. The power losses in the capacitors are calculated according to Section B.3 with the ESR data available from the manufacturer [156].

6.3 Optimization procedure

With the models of the power components introduced, the multi-objective optimization of the single-stage AC-DC DAB module, the single-stage AC-DC multi-port module and the conventional two-stage AC-DC H-bridge module connected to a DC-DC DAB in terms of efficiency and power density can be performed. The optimization procedures for the three module types are depicted in **Fig. 6.15**, **Fig. 6.16** and **Fig. 6.17**.

For a reasonable comparison of the converter modules, the maximum chip area per converter power is limited to the same value. The optimization applies a discrete number of semiconductor devices to account for practical converter implementations. The number of paralleled semiconductor devices is varied by the optimization until the maximum chip area is reached.

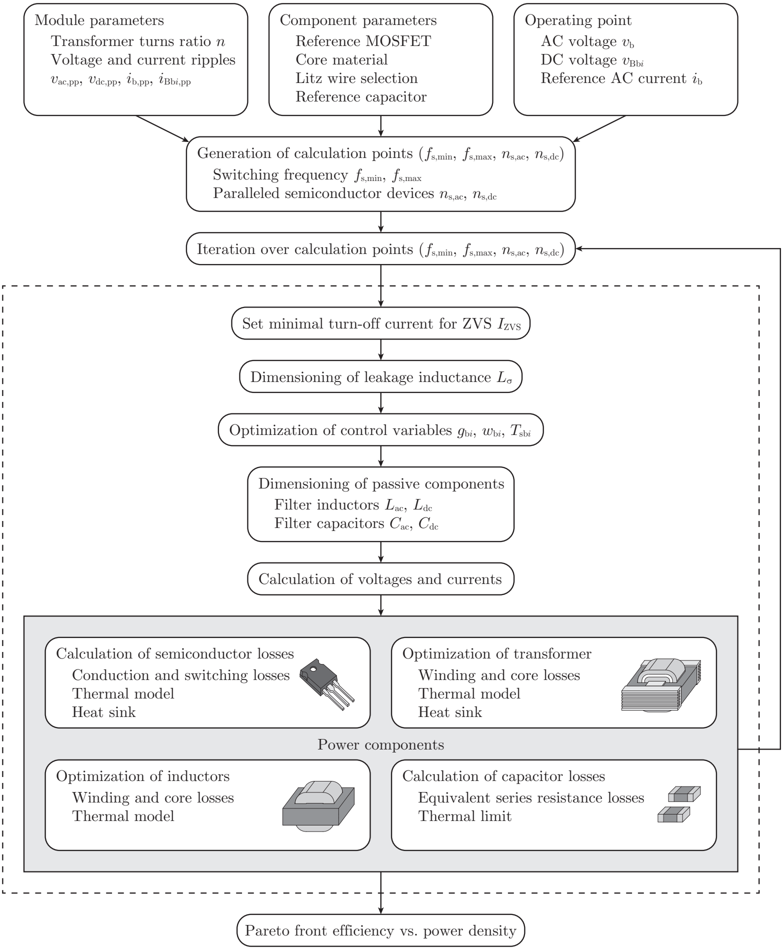

Module parameters
Transformer turns ratio n
Voltage and current ripples
v_ac,pp, v_dc,pp, i_b,pp, i_Bbi,pp
Component parameters
Reference MOSFET
Core material
Litz wire selection
Reference capacitor
Operating point
AC voltage v_b
DC voltage v_Bbi
Reference AC current i_b
Generation of calculation points (f_s,min, f_s,max, n_s,ac, n_s,dc)
Switching frequency f_s,min, f_s,max
Paralleled semiconductor devices n_s,ac, n_s,dc
Iteration over calculation points (f_s,min, f_s,max, n_s,ac, n_s,dc)
Set minimal turn-off current for ZVS I_ZVS
Dimensioning of leakage inductance L_σ
Optimization of control variables g_bi, w_bi, T_sbi
Dimensioning of passive components
Filter inductors L_ac, L_dc
Filter capacitors C_ac, C_dc
Calculation of voltages and currents
Calculation of semiconductor losses
Conduction and switching losses
Thermal model
Heat sink
Optimization of transformer
Winding and core losses
Thermal model
Heat sink
Power components
Optimization of inductors
Winding and core losses
Thermal model
Calculation of capacitor losses
Equivalent series resistance losses
Thermal limit
Pareto front efficiency vs. power density

Figure 6.15: Flow chart of the optimization procedure for the AC-DC DAB converter module depicted in **Fig. 6.2**.

For the single-stage AC-DC DAB module, the optimization procedure changes the number of parallel devices at the AC and the DC side $n_{\mathrm{s,ac}}$, $n_{\mathrm{s,dc}}$ within the limit

$$4n_{\mathrm{s,ac}} + 4n_{\mathrm{s,dc}} \leq 24. \tag{6.41}$$

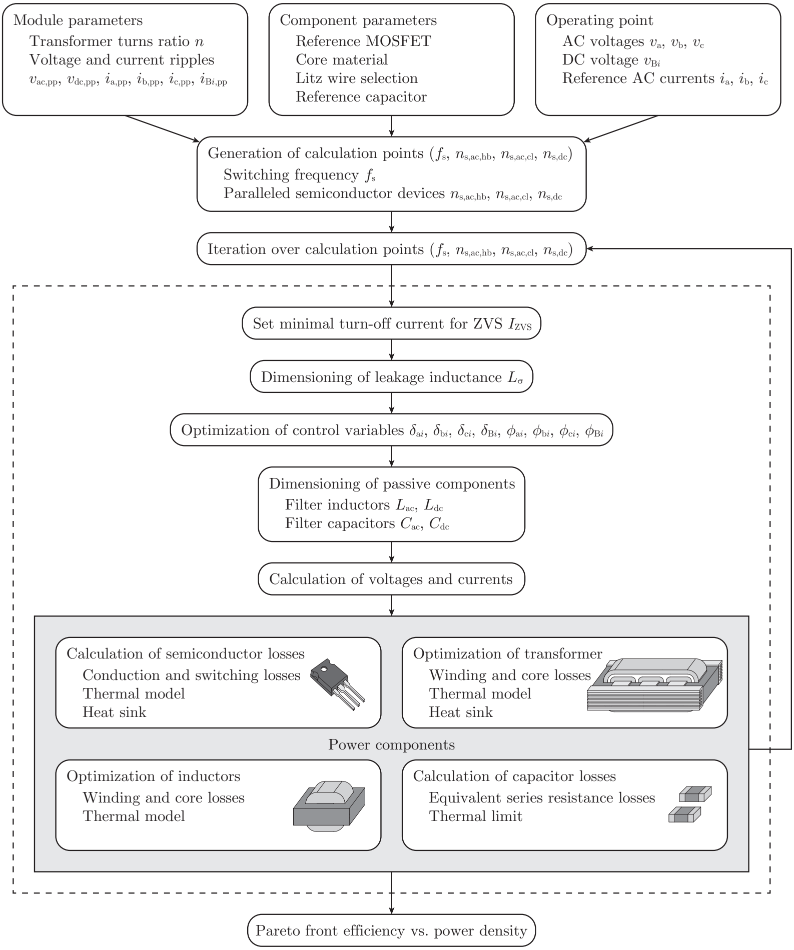

Module parameters
Transformer turns ratio n
Voltage and current ripples
$v_{\mathrm{ac,pp}}$, $v_{\mathrm{dc,pp}}$, $i_{\mathrm{a,pp}}$, $i_{\mathrm{b,pp}}$, $i_{\mathrm{c,pp}}$, $i_{\mathrm{B}i\mathrm{,pp}}$
Component parameters
Reference MOSFET
Core material
Litz wire selection
Reference capacitor
Operating point
AC voltages v_{a}, v_{b}, v_{c}
DC voltage $v_{\mathrm{B}i}$
Reference AC currents i_{a}, i_{b}, i_{c}
Generation of calculation points (f_{s}, $n_{\mathrm{s,ac,hb}}$, $n_{\mathrm{s,ac,cl}}$, $n_{\mathrm{s,dc}}$)
Switching frequency f_{s}
Paralleled semiconductor devices $n_{\mathrm{s,ac,hb}}$, $n_{\mathrm{s,ac,cl}}$, $n_{\mathrm{s,dc}}$
Iteration over calculation points (f_{s}, $n_{\mathrm{s,ac,hb}}$, $n_{\mathrm{s,ac,cl}}$, $n_{\mathrm{s,dc}}$)
Set minimal turn-off current for ZVS I_{ZVS}
Dimensioning of leakage inductance L_{σ}
Optimization of control variables $\delta_{\mathrm{a}i}$, $\delta_{\mathrm{b}i}$, $\delta_{\mathrm{c}i}$, $\delta_{\mathrm{B}i}$, $\phi_{\mathrm{a}i}$, $\phi_{\mathrm{b}i}$, $\phi_{\mathrm{c}i}$, $\phi_{\mathrm{B}i}$
Dimensioning of passive components
Filter inductors L_{ac}, L_{dc}
Filter capacitors C_{ac}, C_{dc}
Calculation of voltages and currents
Calculation of semiconductor losses
Conduction and switching losses
Thermal model
Heat sink
Optimization of transformer
Winding and core losses
Thermal model
Heat sink
Power components
Optimization of inductors
Winding and core losses
Thermal model
Calculation of capacitor losses
Equivalent series resistance losses
Thermal limit
Pareto front efficiency vs. power density

Figure 6.16: Flow chart of the optimization procedure for the AC-DC multi-port converter module depicted in **Fig. 6.4**.

The T-type blocks at the AC side of the AC-DC multi-port module are split into the half-bridge with parallel devices $n_{\mathrm{s,ac,hb}}$ and the clamping switch with parallel devices $n_{\mathrm{s,ac,cl}}$. With $n_{\mathrm{s,dc}}$ being the number of paralleled devices at the DC side, the optimization is executed then within the limit

$$12n_{\mathrm{s,ac,hb}} + 6n_{\mathrm{s,ac,cl}} + 4n_{\mathrm{s,dc}} \leq 72. \tag{6.42}$$

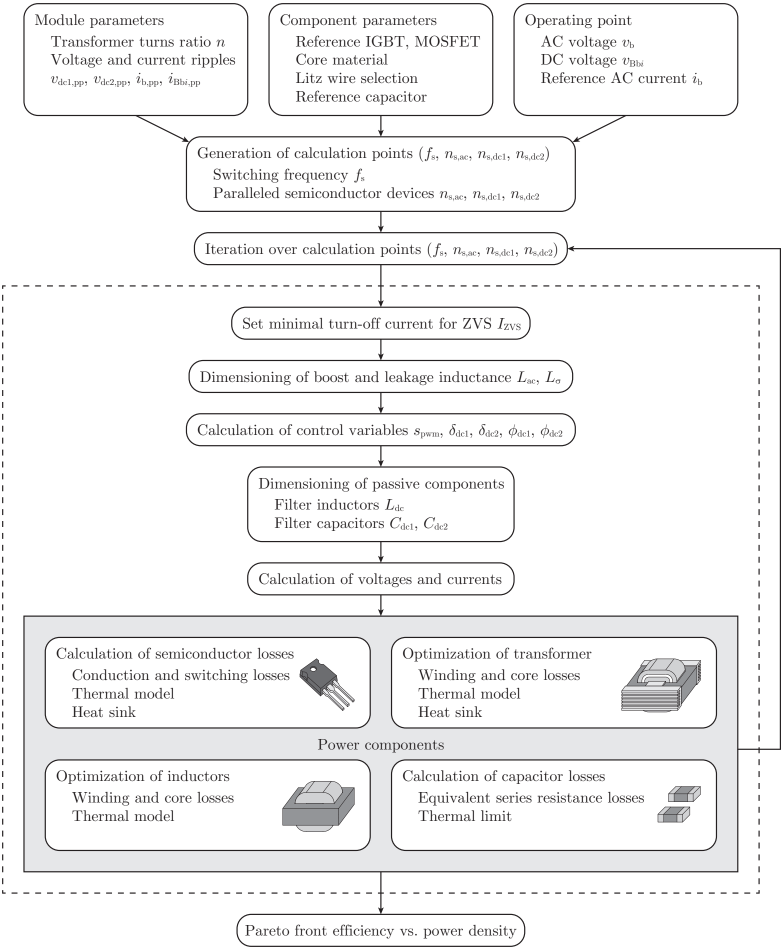

Module parameters
Transformer turns ratio n
Voltage and current ripples
$v_{\mathrm{dc1,pp}}$, $v_{\mathrm{dc2,pp}}$, $i_{\mathrm{b,pp}}$, $i_{\mathrm{B}bi\mathrm{,pp}}$
Component parameters
Reference IGBT, MOSFET
Core material
Litz wire selection
Reference capacitor
Operating point
AC voltage v_{b}
DC voltage $v_{\mathrm{B}bi}$
Reference AC current i_{b}
Generation of calculation points (f_{s}, $n_{\mathrm{s,ac}}$, $n_{\mathrm{s,dc1}}$, $n_{\mathrm{s,dc2}}$)
Switching frequency f_{s}
Paralleled semiconductor devices $n_{\mathrm{s,ac}}$, $n_{\mathrm{s,dc1}}$, $n_{\mathrm{s,dc2}}$
Iteration over calculation points (f_{s}, $n_{\mathrm{s,ac}}$, $n_{\mathrm{s,dc1}}$, $n_{\mathrm{s,dc2}}$)
Set minimal turn-off current for ZVS I_{ZVS}
Dimensioning of boost and leakage inductance L_{ac}, L_{σ}
Calculation of control variables s_{pwm}, δ_{dc1}, δ_{dc2}, ϕ_{dc1}, ϕ_{dc2}
Dimensioning of passive components
Filter inductors L_{dc}
Filter capacitors C_{dc1}, C_{dc2}
Calculation of voltages and currents
Calculation of semiconductor losses
Conduction and switching losses
Thermal model
Heat sink
Optimization of transformer
Winding and core losses
Thermal model
Heat sink
Power components
Optimization of inductors
Winding and core losses
Thermal model
Calculation of capacitor losses
Equivalent series resistance losses
Thermal limit
Pareto front efficiency vs. power density

Figure 6.17: Flow chart of the optimization procedure for the AC-DC H-bridge converter module connected to a DC-DC DAB converter depicted in **Fig. 6.3**.

In case of the two-stage AC-DC H-bridge module connected to a DC-DC DAB, the number of paralleled devices in the H-bridge $n_{\mathrm{s,ac}}$ as well as the number of paralleled devices at the primary and secondary side of the DC-DC DAB $n_{\mathrm{s,dc1}}$, $n_{\mathrm{s,dc2}}$ are varied within the limit

$$4n_{\mathrm{s,ac}} + 4n_{\mathrm{s,dc1}} + 4n_{\mathrm{s,dc2}} \leq 24. \tag{6.43}$$

The maximum total number of semiconductor devices per converter power is then equal for all three types of converter modules. The three-phase module exhibits a converter power with a factor of 3 higher than the single-phase modules, so that the maximum number of semiconductor devices is given by $3 \cdot 24 = 72$. With the stated limits above, no more than 3-4 devices are paralleled which is in a reasonable range from the hardware implementation effort and cost point of view.

Besides the number of paralleled semiconductor devices, the optimization procedure considers the switching frequency

- $f_{\mathrm{s,min}} \in [20\,\mathrm{kHz}, 60\,\mathrm{kHz}]$ and $f_{\mathrm{s,max}} = f_{\mathrm{s,min}} + 100\,\mathrm{kHz}$ for the AC-DC DAB module,
- $f_{\mathrm{s}} \in [20\,\mathrm{kHz}, 100\,\mathrm{kHz}]$ for the AC-DC multi-port module,
- $f_{\mathrm{s}} \in [20\,\mathrm{kHz}, 100\,\mathrm{kHz}]$ for the AC-DC H-bridge module and the connected DC-DC DAB.

The lower limit of 20 kHz limits the volume of the passive components to a maximum which leads to a restricted power density. Furthermore, it is commonly referred as the upper limit of the hearing range of a human. With an increasing switching frequency, the maximum possible efficiency drops until the limit of 100 kHz and 160 kHz respectively is reached.

At the beginning of the optimization procedures shown in **Fig. 6.15**, **Fig. 6.16** and **Fig. 6.17**, the module parameters, the parameters of the power components and the operating point in terms of the AC and the DC voltage as well as the reference AC current are set in order to generate the calculation points depending on the switching frequency and the number of paralleled semiconductor devices.

The optimization iterates over the discrete set of calculation points to evaluate several converter module designs with respect to the power losses and the volume. Before determining the control variables of the modulation, the minimal turn-off current required for ZVS I_{ZVS} as a function of the number of paralleled semiconductor devices for the AC-DC DAB module, the AC-DC multi-port module and the DC-DC DAB converter in the two-stage module is set which has a direct influence on the control variables optimization/calculation (see **Fig. 6.15**, **Fig. 6.16** and **Fig. 6.17**). Moreover, the dependency of the control variables on the transformer leakage inductance L_σ as well as on the boost inductance L_ac in the H-bridge module requires the dimensioning routine of L_σ and/or L_ac to be executed before. The control variables to be determined afterwards are

- $g_{\mathrm{b}i}$, $w_{\mathrm{b}i}$, $T_{\mathrm{sb}i}$ for the ZVS modulation with variable switching frequency of the AC-DC DAB module,
- $\delta_{\mathrm{a}i}$, $\delta_{\mathrm{b}i}$, $\delta_{\mathrm{c}i}$, $\delta_{\mathrm{B}i}$, $\phi_{\mathrm{a}i}$, $\phi_{\mathrm{b}i}$, $\phi_{\mathrm{c}i}$, $\phi_{\mathrm{B}i}$ for the ZVS modulation of the AC-DC multi-port module,
- s_pwm for the three-level carrier based PWM of the H-bridge module and δ_dc1, δ_dc2, ϕ_dc1, ϕ_dc2 for the connected DC-DC DAB converter in the two-stage module.

s_pwm represents the time-dependent switching state of the H-bridge for the three-level PWM with the possible switching states $\{00, 01, 10, 11\}$.

With the control variables fixed, the passive filter components L_ac, L_dc, C_ac, C_dc for the AC-DC DAB module and the AC-DC multi-port module and the components L_dc, C_dc1, C_dc2 for the two-stage module can be dimensioned to fulfill the ripple specifications introduced in **Tab. 6.1**. Then, the characteristic voltage and current waveforms are calculated and fed into the power component routines where the losses and the volume are evaluated. Besides the calculation of the semiconductor losses and the capacitor losses, for the inductors and the transformer, inner optimization routines are executed to determine the Pareto optimal design points of the inductive components (see **Fig. 6.15**, **Fig. 6.16** and **Fig. 6.17**).

If the routine identifies a converter design point to be not feasible because of thermal limitations of a component or the component itself being not feasible within the given boundaries (e.g. inductance value, core cross section, geometry, number of turns restrictions) the current iteration is aborted and the optimization moves to the next calculation point. At the end of the iteration, the most promising designs with the lowest power losses at a given volume are identified to draw the Pareto front in terms of efficiency vs. power density.

6.3.1 Inductor optimization

For each inductor existing in the converter module, the optimization procedure executes the inner optimization routine depicted in **Fig. 6.18** in order to determine the Pareto optimal design points for the component.

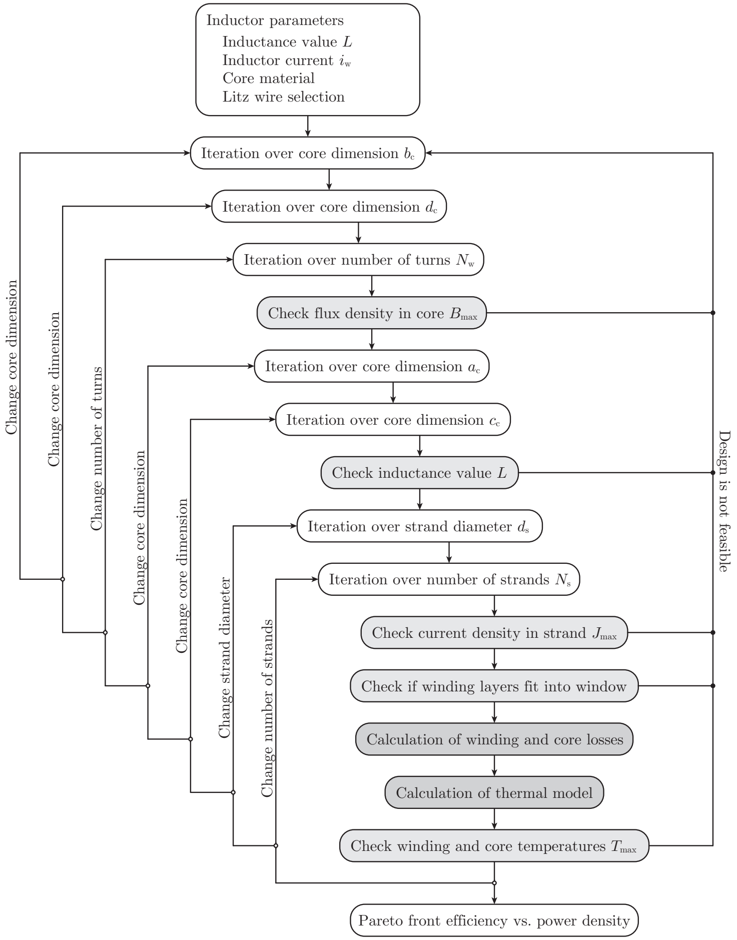

Inductor parameters
Inductance value L
Inductor current i_w
Core material
Litz wire selection
Iteration over core dimension b_c
Iteration over core dimension d_c
Iteration over number of turns N_w
Check flux density in core B_max
Iteration over core dimension a_c
Iteration over core dimension c_c
Check inductance value L
Iteration over strand diameter d_s
Iteration over number of strands N_s
Check current density in strand J_max
Check if winding layers fit into window
Calculation of winding and core losses
Calculation of thermal model
Check winding and core temperatures T_max
Pareto front efficiency vs. power density
Change core dimension
Change core dimension
Change number of turns
Change core dimension
Change core dimension
Change strand diameter
Change number of strands
Design is not feasible

Figure 6.18: Flow chart of the inner optimization procedure for an inductor depicted in **Fig. 6.6** in a converter module.

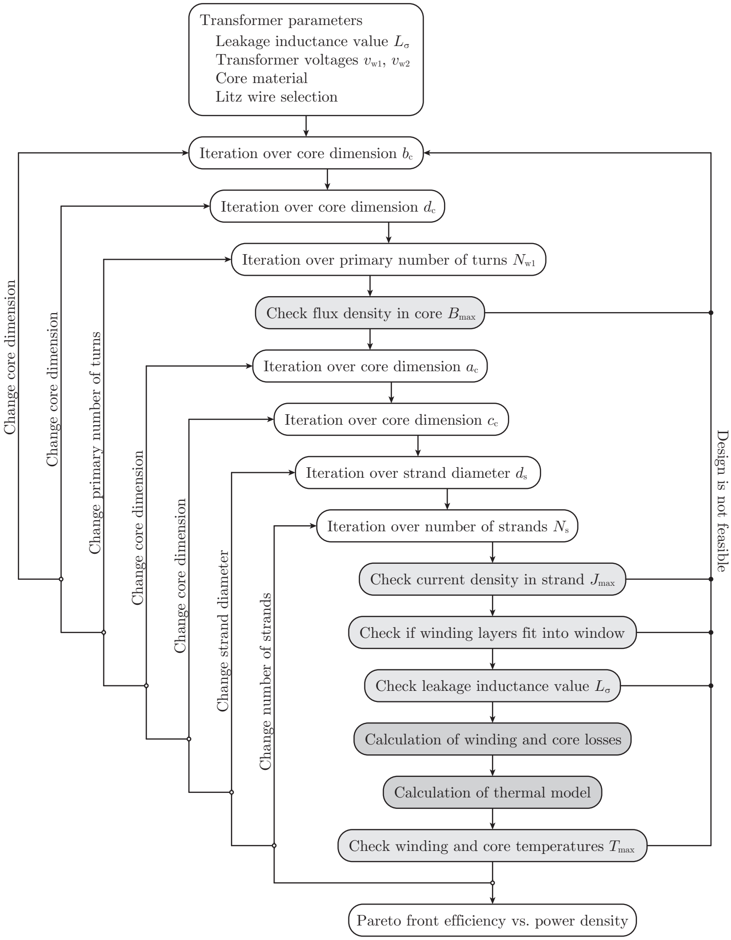

Transformer parameters
Leakage inductance value L_σ
Transformer voltages v_{w1}, v_{w2}
Core material
Litz wire selection
Iteration over core dimension b_c
Iteration over core dimension d_c
Iteration over primary number of turns N_{w1}
Check flux density in core B_{max}
Iteration over core dimension a_c
Iteration over core dimension c_c
Iteration over strand diameter d_s
Iteration over number of strands N_s
Check current density in strand J_{max}
Check if winding layers fit into window
Check leakage inductance value L_σ
Calculation of winding and core losses
Calculation of thermal model
Check winding and core temperatures T_{max}
Pareto front efficiency vs. power density
Change core dimension
Change core dimension
Change primary number of turns
Change core dimension
Change core dimension
Change strand diameter
Change number of strands
Design is not feasible

Figure 6.19: Flow chart of the inner optimization procedure for a two- or a four-winding transformer depicted in **Fig. 6.9** and **Fig. 6.12** in a converter module.

First, the inductor parameters are passed from the top-level calculation routine before the iterations over the geometry dimensions, the number of turns, the strand diameter and the number of strands starts. The check points, where the calculation can be terminated prematurely and the design point is discarded, are marked by the light gray shaded boxes shown in **Fig. 6.18** and are the check of the maximum flux density in the core $B_{\max}$, the check that the required inductance value L is reached by the design, the check of the maximum current density per strand $J_{\max}$, the check if the winding layers fit into the core window and the final check if the maximum temperature $T_{\max}$ is exceeded. The core calculations executed for assessing the performance of the inductor design point determine the core and winding losses and finally the resulting temperatures.

6.3.2 Transformer optimization

Also for the transformer in the converter module, an inner optimization routine is called which is depicted in **Fig. 6.19**. Similar to the inductor optimization, the geometry parameters are varied in the respective ranges as well as the number of primary turns and the litz wire selection adjusted for each design point. At the check points marked by the light gray shaded boxes, the current design point is discarded if it is determined to be not feasible.

6.4 Optimization results

In the following, the results obtained by running the optimizations described above and depicted in **Fig. 6.15**, **Fig. 6.16** and **Fig. 6.17** applying the power component models presented in Section 6.2 for the single-stage AC-DC DAB module, the single-stage AC-DC multi-port module and the two-stage AC-DC H-bridge module connected to a DC-DC DAB converter are discussed.

The overall module Pareto front in terms of losses vs. volume and efficiency vs. power density is evaluated by identifying the module design points with the lowest losses for a given volume for each of the converter modules. Moreover, the Pareto limits resulting at different switching frequencies and different number of paralleled semiconductor devices are presented.

In a final step, the three investigated module types are compared with respect to the reachable efficiency and power density applying the models of the power components given in Section 6.2 for different switching frequencies.

6.4.1 AC-DC dual active bridge module

From the optimization procedure presented in **Fig. 6.15** for the AC-DC DAB module, the Pareto front in terms of losses vs. volume and efficiency vs. power density shown in **Fig. 6.20** results. The gray dots represent the Pareto optimal design points which are obtained within one iteration over the calculation points (see **Fig. 6.15**). At a power density of 1 kW/L an efficiency of 97.0 % and at a power density of 2 kW/L an efficiency of 96.8 % is reached.

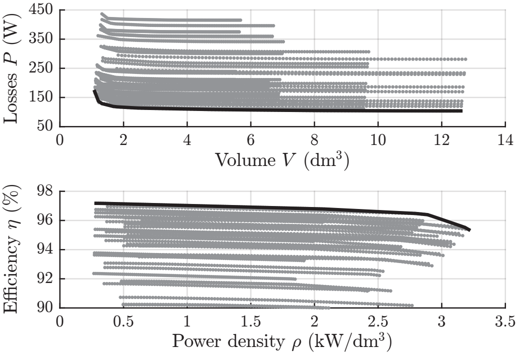


Figure 6.20: Pareto front in terms of losses vs. volume and efficiency vs. power density for the single-stage AC-DC DAB converter module depicted in **Fig. 6.2**. The optimization procedure to obtain the Pareto limits is given in **Fig. 6.15**.

Evaluating the Pareto limits at different minimal switching frequencies $f_{\mathrm{s,min}}$ (for the ZVS modulation with variable switching frequency $f_{\mathrm{s,max}}$ is limited as discussed above in Section 6.3) **Fig. 6.21** is obtained. With a minimal switching frequency of 20 kHz, a module efficiency of up to 97.1 % can be achieved. The power density is limited there around 2 kW/L. Increasing the switching frequency shifts the Pareto curves to lower reachable efficiencies due to the rising switching losses of the semiconductor devices and the rising high-frequency losses in the transformer. Nevertheless, designs with a higher power density are possible as long as the thermal limits can be met.

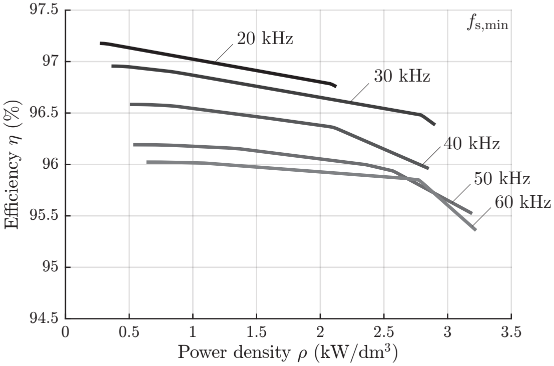


Figure 6.21: Pareto front in terms of efficiency vs. power density for the single-stage AC-DC DAB converter module depicted in **Fig. 6.2** for various switching frequencies $f_{\mathrm{s,min}}$.

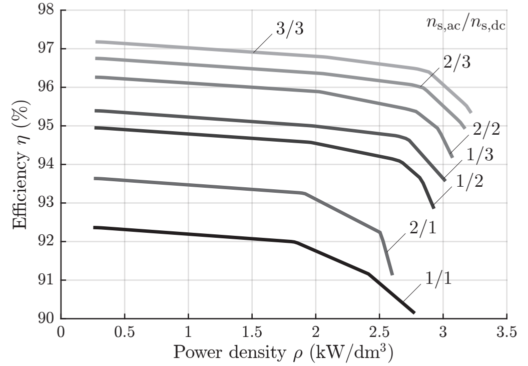


Figure 6.22: Pareto front in terms of efficiency vs. power density for the single-stage AC-DC DAB converter module depicted in **Fig. 6.2** for different combinations of paralleled semiconductor devices $n_{\mathrm{s,ac}}$, $n_{\mathrm{s,dc}}$.

The highest efficiency is obtained for paralleling three MOSFETs at the AC side as well as at the DC side concluded from **Fig. 6.22** where the Pareto curves for different combinations of the number of paralleled semiconductor devices are shown. It can be seen that the additional paralleling at the DC side from 1/1 to 1/2 results in a higher efficiency gain than the additional paralleling at the AC side from 1/1 to 2/1. Furthermore, paralleling semiconductor devices results in lower losses up to a certain limit, so that a greater thermal resistance from heat sink to ambient is allowable what in turn reduces the required heat sink volume and the power density is increased.

6.4.2 AC-DC multi-port module

For the AC-DC multi-port module, the optimization procedure depicted in **Fig. 6.16** leads to the Pareto front given in **Fig. 6.23**. Again, the gray dots represent the Pareto optimal design points which are obtained within one iteration over the calculation points (see **Fig. 6.16**). At a power density of 1 kW/L an efficiency of 93.7 %, at a power density of 2 kW/L an efficiency of 93.6 % and at a power density of 3 kW/L an efficiency of 93.4 % can be achieved. The Pareto curve is quite flat in terms of an approximately constant efficiency over a wide power density range which shows that the construction size of the four-winding transformer can be reduced without a significant increase of the losses until the thermal limit is reached.

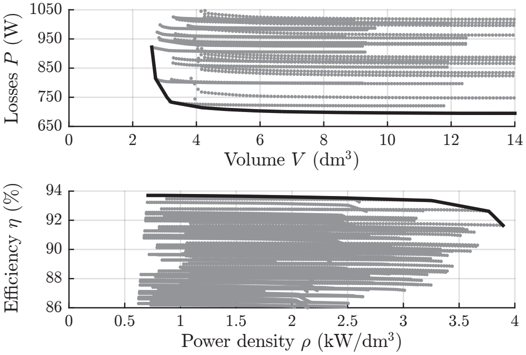


Figure 6.23: Pareto front in terms of losses vs. volume and efficiency vs. power density for the single-stage AC-DC multi-port converter module depicted in **Fig. 6.4**. The optimization procedure to obtain the Pareto limits is given in **Fig. 6.16**.

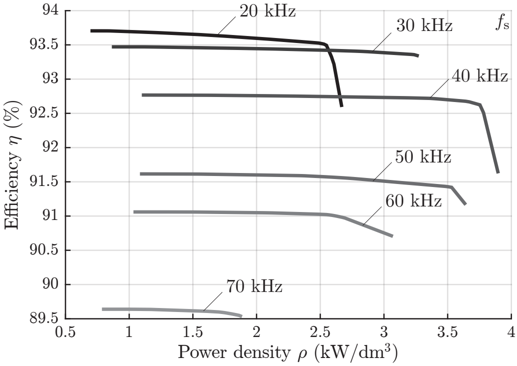


Figure 6.24: Pareto front in terms of efficiency vs. power density for the single-stage AC-DC multi-port converter module depicted in **Fig. 6.4** for various switching frequencies f_s.

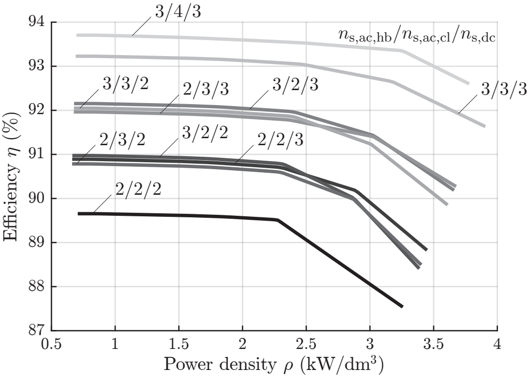


Figure 6.25: Pareto front in terms of efficiency vs. power density for the single-stage AC-DC multi-port converter module depicted in **Fig. 6.4** for different combinations of paralleled semiconductor devices $n_{s,ac,hb}$, $n_{s,ac,cl}$, $n_{s,dc}$.

In **Fig. 6.24**, the Pareto limits at different switching frequencies f_s are depicted. With a switching frequency of 20 kHz, a module efficiency of up to 93.7 % can be achieved. The power density is limited there around 2.5 kW/L. Increasing the switching frequency shifts the Pareto curves to lower reachable efficiencies due to the rising switching losses of the semiconductor devices and the rising high-frequency losses in the transformer. At around 40 kHz, the maximum power density that can be achieved is reached. With a further rise of the switching frequency, the power density decreases again as the thermal restrictions can only be met by a corresponding heat sink size for the semiconductor devices and an enlarged transformer volume.

By paralleling three MOSFETs in the half-bridge and four MOSFETs in the clamping switch of the AC-side T-type blocks as well as three MOSFETs in the H-bridge at the DC side, the highest efficiency is reached concluded from **Fig. 6.25** where the Pareto curves for different combinations of the number of paralleled semiconductor devices are shown. It can be seen that the additional paralleling in the half-bridge at the AC side from 2/2/2 to 3/2/2, in the clamping switch at the AC side from 2/2/2 to 2/3/2 or in the H-bridge at the DC side from 2/2/2 to 2/2/3 results in a similar efficiency gain. Moreover, paralleling semiconductor devices results in lower losses up to a certain limit, so that the required heat sink volume is reduced and the power density increased.

6.4.3 AC-DC H-bridge module with DC-DC dual active bridge

In case of the conventional two-stage converter optimized with the routine described in **Fig. 6.17**, the performance of the AC-DC H-bridge module and the connected DC-DC DAB converter are evaluated separately first. In a second step, the Pareto limits for the cascaded two-stage module are presented.

AC-DC H-bridge module

For the AC-DC H-bridge module, **Fig. 6.26** shows the Pareto front in terms of losses vs. volume and efficiency vs. power density. The gray dots represent the Pareto optimal design points which are obtained within one iteration over the calculation points (see **Fig. 6.17**). At a power density of 1 kW/L an efficiency of 98.4 %, at a power density of 2 kW/L an efficiency of 98.2 % and at a power density of 3 kW/L an efficiency of 97.9 % can be achieved.

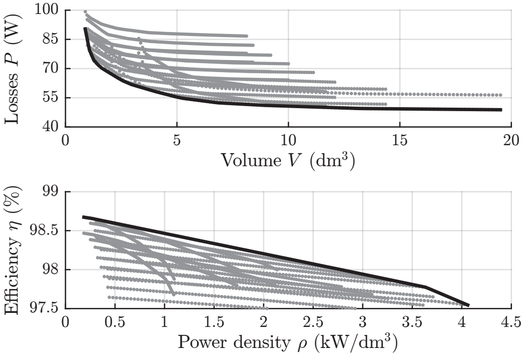


Figure 6.26: Pareto front in terms of losses vs. volume and efficiency vs. power density for the AC-DC H-bridge stage of the two-stage converter module depicted in **Fig. 6.3**. The optimization procedure to obtain the Pareto limits is given in **Fig. 6.17**.

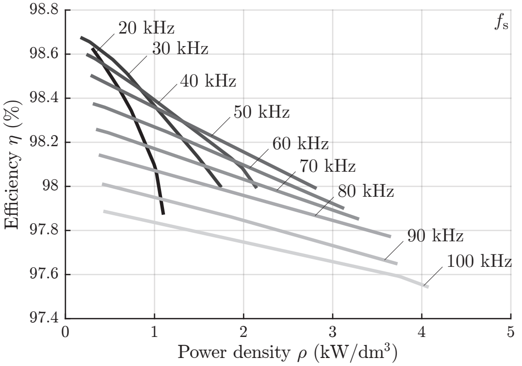


Figure 6.27: Pareto front in terms of efficiency vs. power density for the AC-DC H-bridge stage of the two-stage converter module depicted in **Fig. 6.3** for various switching frequencies f_s.

Evaluating the Pareto limits at different switching frequencies f_s, **Fig. 6.27** is obtained. With a switching frequency of 20 kHz, a module efficiency of up to 98.6 % can be achieved. The power density is limited there around 1 kW/L which is rather low since with the given AC current ripple specification (see **Tab. 6.1**) high boost inductance values are necessary which result in a relatively large construction size for an AC current of 16 A. Increasing the switching frequency shifts the Pareto curves to lower reachable efficiencies due to the rising switching losses of the IGBTs and substantially increases the power density as the required boost inductance value drops.

DC-DC dual active bridge

In case of the DC-DC DAB converter, **Fig. 6.28** depicts the Pareto front in terms of losses vs. volume and efficiency vs. power density. Again, the gray dots represent the Pareto optimal design points which are obtained within one iteration over the calculation points (see **Fig. 6.17**). At a power density of 5 kW/L an efficiency of 99.4 %, at a power density of 10 kW/L an efficiency of 99.3 % and at a power density of 15 kW/L an efficiency of 99.1 % can be achieved.

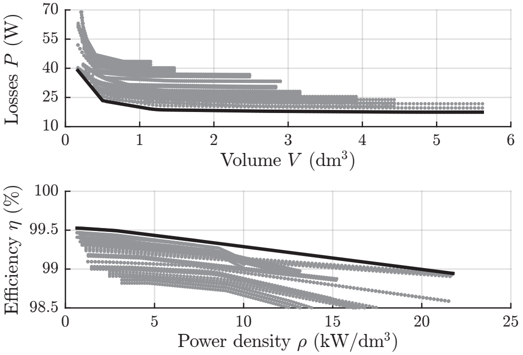


Figure 6.28: Pareto front in terms of losses vs. volume and efficiency vs. power density for the DC-DC DAB stage of the two-stage converter module depicted in **Fig. 6.3**. The optimization procedure to obtain the Pareto limits is given in **Fig. 6.17**.

Such a high power density for a DAB converter is only achievable for a rather low leakage inductance value of the transformer in combination with the operation by the standard phase shift modulation scheme and a transformer turns ratio near unity. Nevertheless, with the 20 % phase shift limit for the maximum power transfer as discussed above, the power operating range of the DAB is quite limited.

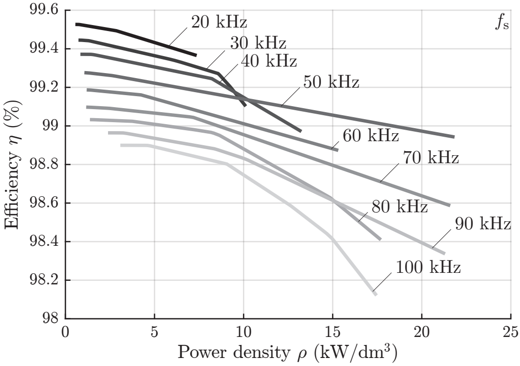


Figure 6.29: Pareto front in terms of efficiency vs. power density for the DC-DC DAB stage of the two-stage converter module depicted in **Fig. 6.3** for various switching frequencies f_s.

Fig. 6.29 shows the Pareto curves obtained for different switching frequencies f_s. With a switching frequency of 20 kHz, a converter efficiency of up to 99.5 % can be achieved. The power density is limited there around 7.3 kW/L. Increasing the switching frequency shifts the Pareto curves to lower reachable efficiencies due to the rising switching losses of the semiconductor devices and the rising high-frequency losses in the transformer. Between 50 kHz and 70 kHz the maximum power density that can be achieved is reached. With a further rise of the switching frequency, the power density decreases again as the thermal restrictions can only be met by a corresponding heat sink size for the semiconductor devices and an enlarged transformer volume.

Two-stage AC-DC module

After the investigation of the single converter stages of the conventional two-stage AC-DC module, **Fig. 6.30** combines the Pareto limits to assess the performance of the two-stage AC-DC H-bridge module connected to a DC-DC DAB converter.

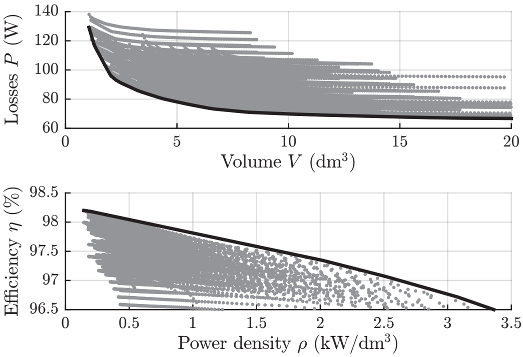


Figure 6.30: Pareto front in terms of losses vs. volume and efficiency vs. power density for the two-stage converter module with an AC-DC H-bridge module connected to a DC-DC DAB converter depicted in **Fig. 6.3**. The optimization procedure to obtain the Pareto limits is given in **Fig. 6.17**.

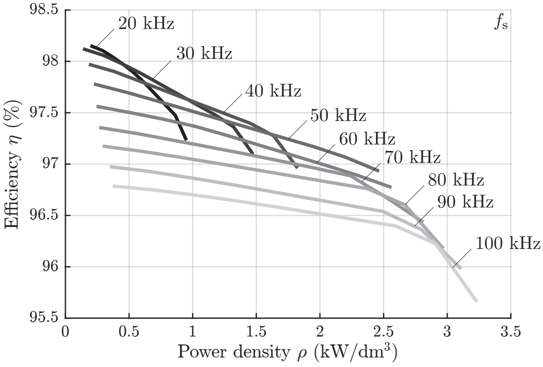


Figure 6.31: Pareto front in terms of efficiency vs. power density for the two-stage converter module with an AC-DC H-bridge module connected to a DC-DC DAB converter depicted in **Fig. 6.3** for various switching frequencies f_s.

As in the previous graphs, the gray dots represent the Pareto optimal design points which are obtained within one iteration over the calculation points (see **Fig. 6.17**). The two-stage converter module achieves an efficiency of 97.8 % at a power density of 1 kW/L, an efficiency of 97.3 % at a power density of 2 kW/L and an efficiency of 96.7 % at a power density of 3 kW/L.

By evaluating the Pareto limits at different switching frequencies f_s, **Fig. 6.31** is obtained. With a switching frequency of 20 kHz, a module efficiency of up to 98.1 % can be achieved. The power density is limited there around 0.9 kW/L. Increasing the switching frequency shifts the Pareto curves to lower reachable efficiencies due to the rising switching losses of the semiconductor devices and the rising high-frequency losses in the transformer. Nevertheless, designs with a higher power density are possible as long as the thermal limits can be met.

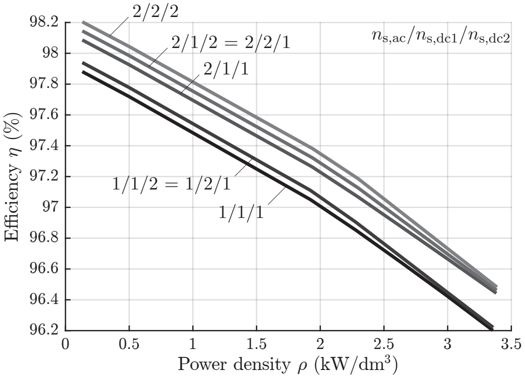


Figure 6.32: Pareto front in terms of efficiency vs. power density for the two-stage converter module with an AC-DC H-bridge module connected to a DC-DC DAB converter depicted in **Fig. 6.3** for different combinations of paralleled semiconductor devices $n_\mathrm{s,ac}$, $n_\mathrm{s,dc1}$, $n_\mathrm{s,dc2}$.

The highest efficiency is obtained for paralleling two IGBTs in the AC-DC H-bridge stage and two MOSFETs in the DC-DC DAB converter both at the primary and the secondary side concluded from **Fig. 6.32** where the Pareto curves for different combinations of the number of paralleled semiconductor devices are shown. It can be seen that the additional paralleling in the DC-DC DAB converter from 1/1/1 to 1/1/2 or 1/2/1 is less effective in terms of an efficiency gain compared to the additional paralleling in the H-bridge stage from 1/1/1 to 2/1/1. Furthermore, although paralleling semiconductor devices results in lower losses up to a certain limit, the reachable power density cannot be substantially increased for the considered combinations of number of paralleled switches.

6.5 Comparison of converter modules

For the final comparison of the proposed single-stage converter modules covering the AC-DC DAB module and the AC-DC multi-port module to the conventional two-stage AC-DC H-bridge module connected to a DC-DC DAB converter, the module Pareto limits by applying the power component models from Section 6.2 are presented together in **Fig. 6.33** for a switching frequency of 20 kHz and in **Fig. 6.34** for a switching frequency of 50 kHz.

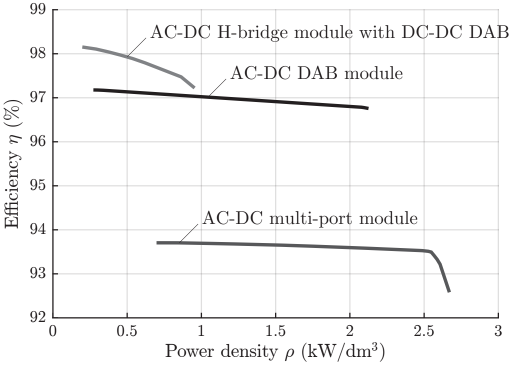


Figure 6.33: Pareto front in terms of efficiency vs. power density for the single-stage AC-DC DAB module, the single-stage AC-DC multi-port module and the two-stage AC-DC H-bridge module connected to a DC-DC DAB converter at a switching frequency of $f_s = f_{s,\min} = 20\,\text{kHz}$ for comparison.

In both cases, the highest efficiency can be achieved by using the conventional two-stage module, namely an efficiency of 98.1 % at 20 kHz and 97.7 % at 50 kHz respectively. The power density is quite limited due to the strict AC current ripple specification at around 1 kW/L for 20 kHz and 2.5 kW/L for 50 kHz.

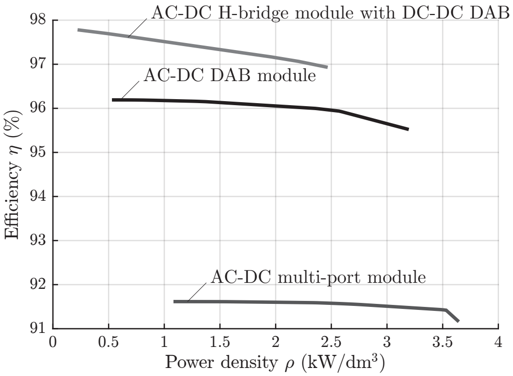


Figure 6.34: Pareto front in terms of efficiency vs. power density for the single-stage AC-DC DAB module, the single-stage AC-DC multi-port module and the two-stage AC-DC H-bridge module connected to a DC-DC DAB converter at a switching frequency of $f_\mathrm{s} = f_\mathrm{s,min} = 50\,\mathrm{kHz}$ for comparison.

The AC-DC DAB module achieves slightly lower efficiencies with its maximum being at 97.2 % for 20 kHz and 96.2 % for 50 kHz. Compared to the two-stage module, the power density can be increased up to 2.1 kW/L for 20 kHz and 3.2 kW/L for 50 kHz.

The complex concept of the AC-DC multi-port module exhibits substantially lower possible efficiencies at 93.7 % for a 20 kHz and 91.6 % for a 50 kHz operation. Nevertheless, the power density can be increased to 2.6 kW/L for 20 kHz and 3.6 kW/L for 50 kHz.

On the basis of the outcome of the multi-objective optimization of the three different converter modules, it is concluded, that the integration of the galvanic isolation on module level for a phase-modular single-stage AC-DC converter system leads to a reasonable performance in terms of efficiency and power density compared to a conventional two-stage approach. This is especially given for the investigated single-phase converter module. In case of the AC-DC multi-port module, the realization of the galvanic isolation through a complex magnetic coupling of the AC and the DC ports results in substantially lower reachable efficiencies originating from the high circulating currents which lead to high semiconductor and transformer losses.

6.6 Summary and conclusion

In this chapter, the multi-objective optimization and the final comparison of the two proposed bidirectional isolated AC-DC converter systems for battery energy storage systems are presented. On module level the single-stage AC-DC DAB module and the single-stage AC-DC multi-port module are compared to the conventional two-stage AC-DC H-bridge module connected to a DC-DC DAB for the use in a CHB converter with respect to efficiency and power density.

The converter module optimizations are carried out at a fixed operating point in terms of a 230 V, 50 Hz AC mains connection, a constant battery and/or DC link voltage of 400 V and a reference AC phase current of 16 A. At the input and output terminals of the modules, the same maximum voltage and current ripple specifications are assumed. The implemented optimization uses discrete semiconductor devices with the total number of devices per converter power limited to a maximum for a reasonable comparison of the single-phase and the three-phase converter modules.

In order to evaluate the losses and the volume of the power components, comprehensive models in the electric, magnetic and thermal domain are introduced as these are an important prerequisite for the optimization.

The semiconductor model uses a discrete reference MOSFET for the operation under ZVS conditions in the single-stage converter modules and a discrete reference IGBT operated under hard-switching conditions for the H-bridge in the two-stage converter module. The heat sink volume is determined by the calculation of the thermal sink-to-ambient resistance in combination with an assumed CSPI of $15\,\mathrm{W/(K{\cdot}dm^3)}$.

In case of the inductive components like the filter inductors as well as the two- and four-winding transformer, the model uses E-cores where the geometry dimensions are varied by the optimization. For the inductors, powder cores with the Kool Mu 26u material and for the transformers, the nanocrystalline VITROPERM 500F material is considered. The windings are realized by litz wires with a discrete selection of the strand diameters and the number of strands fed into the optimization. In the thermal model, free convection cooling for the inductors and forced convection cooling for the transformers using heat pipes on the top and the bottom of the core connected to an outer heat sink for a sufficient heat removal is assumed.

In order to reach a high power density, ceramic capacitors are applied with two reference components for different voltages (the capacitors in the AC-side series connection have a lower voltage rating than the DC-side capacitors). The thermal model checks the power dissipation of a single component and increases the number of paralleled capacitors as soon as the maximum current is exceeded.

The optimization procedure is implemented based on an iteration over a discrete set of calculation points within the same or comparable boundaries for all three types of converter modules. If the routine identifies a converter design point to be not feasible because of thermal limitations of a component or the component itself being not feasible within the given boundaries, the current iteration is aborted and the optimization moves to the next calculation point. At the end of the iteration, the most promising designs with the lowest power losses at a given volume are identified to draw the Pareto front in terms of efficiency vs. power density.

From the obtained optimization results, the efficiencies achieved at a power density of 2.5 kW/L are for the single-stage AC-DC DAB module 96.6 %, for the single-stage AC-DC multi-port module 93.5 % and for the two-stage AC-DC H-bridge module connected to a DC-DC DAB 97.1 %.

For a phase-modular single-stage AC-DC converter system, the integration of the galvanic isolation on module level leads to a reasonable performance in terms of efficiency and power density compared to a conventional two-stage approach. This can be seen for the investigated single-phase converter module. Nevertheless, in case of the AC-DC multi-port module, high circulating currents exist given through the complex magnetic coupling of the AC and the DC ports leading to high semiconductor and transformer losses, so that only substantially lower efficiencies are achievable.

7

Conclusion and Outlook

This thesis focuses on the integration of the galvanic isolation on module level for phase-modular AC-DC converter topologies connected to a medium voltage (MV) AC grid. For an ultra-fast charging station for electric vehicles (EVs) with an integrated battery energy storage system, mainly two new converter concepts for the AC-DC grid interface are introduced and thoroughly investigated. These are the cascaded AC-DC dual active bridge (DAB) converter as well as the cascaded AC-DC multi-port converter with a three-phase AC port and a DC port. By implementing a multi-objective optimization, the performance of the proposed converter systems with respect to efficiency and power density is evaluated and compared to the conventional two-stage approach using AC-DC H-bridge modules connected to DC-DC DAB converters.

7.1 Summary and conclusion

The cascaded AC-DC DAB converter for battery energy storage systems is developed based on a state-of-the-art cascaded H-bridge (CHB) converter and integrates module-level galvanic isolation using series-connected single-stage bidirectional isolated AC-DC converter modules. The modules discussed are AC-DC DAB topologies, since they allow a high power density design and the operation in a power range of several kW.

Based on the degrees of freedom in control and a qualitative comparison of the semiconductor losses, the topology with an AC-side half-bridge and a DC-side full-bridge is identified as the most suitable topology since the hardware control effort as well as the system costs can be significantly reduced compared to a standard full-bridge/full-bridge DAB. Besides the commonly used control variables of the phase shift and the clamping intervals for a DAB, the switching frequency is considered for control as an additional degree of freedom available for optimizing the transformer peak and/or RMS currents. Considering the semiconductor losses, the AC-side half-bridge is comparable to an AC-side full-bridge assuming full-block voltage operation without clamping. At the DC side, for the same degrees of freedom in control, the use of a full-bridge is more beneficial than using a T-type circuit since commonly the clamping interval is minimized in order to reduce the circulating current and therefore the reactive power.

The overall cascaded AC-DC DAB converter is modeled by the series connection of the grid-side equivalent circuits of the AC-DC DAB modules per phase leg with their capacitive voltage ports consisting of two filter capacitors and a controlled current source in parallel. Adjusting the power transfer of a DAB module, the current source is controlled in order to regulate the AC-side module voltage and therefore the grid current. By controlling the module voltage, also the power distribution among the modules is set since all modules in a phase string are connected in series and exhibit the same module current.

On module level, two different modulation schemes are developed. One which allows ZCS at the grid side with IGBTs and ZVS at the battery side with MOSFETs presuming a constant switching frequency and another one which allows ZVS on both sides with MOSFETs considering also the variation of the switching frequency. To derive the power flow equations including their borders for the minimum and the maximum power transfer, a mathematical analysis of the transformer leakage inductance current by using piecewise linear equations is conducted. In case of the ZVS modulation with variable switching frequency, a numerical optimization scheme is developed for determining the optimal control variables in order to minimize the transformer leakage inductance peak currents.

For controlling the cascaded AC-DC DAB converter with an integrated battery energy storage system, the top-level as well as the module-level control is introduced. The objectives of the top-level control are obtaining the grid and phase angles by means of phase-locked loops (PLLs), controlling the grid current in the dq-frame and balancing the average state of charge (SOC) values of the storage batteries over the three phases. On the module level, the SOCs of the batteries in one phase

are balanced and the grid-side module voltages are controlled.
For validating the theoretical aspects of the new ZVS modulation including switching frequency variation, an AC-DC DAB module is designed and a 3.3 kW hardware prototype built. The developed modulation and control scheme is implemented in VHDL on an FPGA device. The measurements at the hardware prototype prove the concept and the practical feasibility of the modulation and conform to the developed mathematical models. Moreover, the analysis of the harmonics of the AC module current shows full compliance with the IEC 61000-3-2 class A standard. The measured efficiency of the prototype at 1.7 kW output power is 95 % whereas the reached power density is around 2.5 kW/L.
The simulation of a 45 kW cascaded AC-DC DAB converter with an integrated battery energy storage system connected to a 2.4 kV AC grid finally validates the aspects of the developed control structure on system and module level. Within the simulation model, three AC-DC DAB modules per phase leg with an input voltage of 460 V ± 30 % and a nominal output power of 5 kW are considered. Each module is connected to a storage battery pack modeled as a constant voltage source of 350 V. The simulation curves verify the effectiveness of the discussed control methods to balance the SOCs between the phase legs as well as between the single batteries in a phase leg while maintaining sinusoidal grid currents in phase with the grid voltages (PFC operation).

The cascaded AC-DC multi-port converter for battery energy storage systems is derived from state-of-the-art DC-DC multi-port converters to integrate module-level galvanic isolation and to provide bidirectional power flow capability. For the three different phases, each converter module connects three AC ports to one DC port to attach a storage battery pack. To distribute the AC phase voltage among the converter modules, the AC ports belonging to the same phase are connected in series.
With the developed module topology, the AC-side winding voltages are summed up by applying either three two-winding transformers with the DC-side windings electrically connected in series or a four-winding transformer with the AC-side windings magnetically connected in parallel. This leads to a three-phase AC port formed by the series connection of the AC ports belonging to the three different phases, so that an approximately constant sum of the half-cycle voltage-second products applied to the AC-side windings becomes available for control. Since the series connection of the AC port windings lead to clamping in-

tervals varying in a wide range depending on the instantaneous phase current/power, the use of T-type blocks at the AC side is advantageous as the conduction losses caused by the circulating current flowing through all ports (three AC and one DC port) can be reduced with the use of semiconductor devices rated for a lower blocking voltage in the clamping switch (lower on-state resistance) compared to the devices in the half-bridge.

The overall cascaded AC-DC multi-port converter is modeled by the series connection of the grid-side equivalent circuits of the AC-DC multiport modules per phase leg with their three capacitive AC voltage ports consisting of two filter capacitors and a controlled current source in parallel. In order to regulate the AC port module voltages and therefore the grid current, the power transfer at an AC port of the multi-port module is adjusted in terms of controlling the current source. The power distribution among the AC ports in the same phase is set by controlling the AC port module voltages since all AC ports in a phase string are connected in series and exhibit the same module current.

The mathematical analysis of the power flows in a multi-port converter system depending on the control variables is an essential prerequisite for the design process of the hardware as well as the control. With the well-known approach using piecewise linear equations for the transformer leakage inductance current, several mathematical cases depending on the phase shifts and the clamping intervals have to be distinguished. Due to the mathematical complexity, especially for high port numbers, a new modeling approach is developed by using basic superposition principles to find general analytical formulas for the power flows. With this approach, there is no need for a mathematical distinction of cases.

On module level, two different modulation schemes are developed. One is based on a simple fundamental wave model of the medium-frequency (MF) square-wave voltages applied to the transformer windings where higher order harmonics are neglected. An analytical calculation scheme is established for determining the control variables in terms of phase shifts and clamping intervals. The main drawbacks induced are the low-frequency (LF) harmonic phase current distortions as well as the lack of soft-switching conditions at every switching instant since the transformer leakage inductance current is not actively shaped. To overcome these drawbacks, another modulation scheme based on the introduced general power flow equations considering also ZVS conditions is developed. The control variables are first determined numerically by

implementing an optimization for minimizing the transformer leakage inductance RMS current under ZVS constraints. The results obtained numerically show a structure that can be also modeled by analytic equations which is presented in a second step.
For evaluating the theoretical efficiencies, a design example of a 10 kW AC-DC multi-port module is presented with the components and losses described by state-of-the-art models. The design example predicts a peak efficiency of around 91.7 % at an output power of 10 kW and a battery voltage of 380 V. The estimated power density is around 2.5 kW/L. The conduction losses caused by the circulating current originating from the series connection of all ports given through the module topology substantially decrease the achievable efficiency. In general, a relatively large chip area is required at the AC side (the design example uses three MOSFET devices in parallel).
For validating the theoretical aspects of the developed modulations, the AC-DC multi-port module is simulated with the modulation schemes implemented as part of the simulation model. The obtained simulation curves conform to the developed mathematical models for the modulation schemes and show the feasibility of their implementation by using lookup tables (LUTs) precalculated offline. For the fundamental phasor modulation, the LF harmonic distortions of the AC phase currents can be clearly seen whereas in case of the ZVS modulation the harmonic distortion of the AC current waveforms is substantially decreased.

For the evaluation of the performance of the proposed converter systems with respect to efficiency and power density, a multi-objective optimization for the single-stage AC-DC DAB module, the single-stage AC-DC multi-port module and the conventional two-stage AC-DC H-bridge module connected to a DC-DC DAB for the use in a CHB converter is implemented. For the optimizations, the converter modules are operated at a fixed 230 V, 50 Hz AC mains voltage, a constant battery and/or DC link voltage of 400 V and a reference AC phase current of 16 A. At the input and output terminals of the modules, the same maximum voltage and current ripple specifications are assumed. To ensure a reasonable comparison of the single-phase and the three-phase converter modules, the total number of semiconductor devices per converter power is limited to a maximum.
As an important prerequisite for the optimization, comprehensive models of the power components in the electric, magnetic and thermal domain are developed in order to determine the losses and the volume.

For the operation under ZVS conditions in case of the single-stage converter modules, a discrete reference MOSFET is considered whereas for the operation under hard-switching conditions in case of the H-bridge in the two-stage converter module, a discrete reference IGBT is selected. The thermal model evaluates the sink-to-ambient resistance to obtain the required heat sink volume based on an assumed cooling system performance index (CSPI) of $15\,\mathrm{W/(K{\cdot}dm^3)}$.

The inductive components like the filter inductors as well as the two- and four-winding transformer are modeled with E-cores where the optimization varies the geometry dimensions. The core material is not changed during the optimization and given by the Kool Mu 26u material for the inductors and by the nanocrystalline VITROPERM 500F material for the transformers. The windings are realized by litz wires with a discrete selection of the strand diameters and the number of strands. For the inductors, free convection cooling is assumed while the transformers apply additional heat pipes on the top and the bottom of the core connected to an outer heat sink for forced convection cooling in order to ensure a sufficient heat removal.

For the capacitors, two reference ceramic components for different voltages (the capacitors in the AC-side series connection have a lower voltage rating than the DC-side capacitors) are selected to reach a high power density design. Concerning the heat removal, the optimization checks the power dissipation of a single component and increases the number of paralleled capacitors as soon as the maximum current is exceeded.

The optimization procedure is implemented based on an iteration over a discrete set of calculation points within the same or comparable boundaries for all three types of converter modules. At converter design points that are marked by the optimization as being not feasible because of thermal limitations of a component or the component itself being not feasible within the given boundaries, the current iteration is aborted and the optimization moves to the next calculation point. The most promising designs with the lowest power losses at a given volume are identified at the end of the iteration to draw the Pareto front in terms of efficiency vs. power density.

At a power density of 2.5 kW/L, the single-stage AC-DC DAB module achieves an efficiency of 96.6 %, the single-stage AC-DC multi-port module an efficiency of 93.5 % and the two-stage AC-DC H-bridge module connected to a DC-DC DAB an efficiency of 97.1 %.

The final optimization results predict a reasonable performance in terms of efficiency and power density for the module-level integration of galvanic isolation for a phase-modular single-stage AC-DC converter system compared to a conventional two-stage approach based on the CHB. This is especially the case for the investigated single-phase AC-DC DAB converter module. Nevertheless, in case of the AC-DC multi-port module with a complex magnetic coupling of the AC and the DC ports, substantially lower efficiencies are achievable due to the high circulating currents occurring in the semiconductor devices and the multi-winding transformer. Furthermore, from the complexity of the control point of view and also considering the mechanical assembly with coupling the modules over the three different phases, the multi-port module is not beneficial. Compared to the DAB module, the cross coupling between the different phases significantly degrades the concept of modularity as it is lost within each single phase string.

7.2 Outlook

With the focus of this thesis being on the AC-DC grid interface of an ultra-fast charging station for EVs connected to the MV AC grid, in a next step, the high power DC-DC charging converters have to be addressed. Suitable non-isolated topologies in combination with the most promising modulation schemes should be evaluated concerning the reachable efficiency and power density, the reliability and the system costs.

For the cascaded AC-DC DAB converter, partly or completely hard-switched modulation schemes could gain interest with the currently evolving new semiconductor devices based on silicon carbide or gallium nitride to reach comparable or even higher module efficiencies than with the state-of-the-art silicon technology. Furthermore, the anti-serial connection of two MOSFETs could be replaced by future semiconductor devices featuring bidirectional voltage blocking and current conduction capability.

In case of the AC-DC multi-port converter, further research could be conducted on the basic interconnection of the AC ports of a three-phase voltage system and the DC port through a single magnetic core (windings electrically/magnetically connected in series/parallel). Moreover, these investigations have a direct impact on the transformer design considerations and demand the development of suitable modulation schemes. In general, further modulation schemes for the presented AC-DC multi-port module could be developed including schemes that allow ZCS at the AC side for the use of IGBTs while maintaining ZVS at the DC side suitable for a MOSFET application, sequential schemes where only one phase transfers power while the other two are in a clamping state or schemes for a resonant converter operation.

Concerning the multi-objective optimization and the comparison of the module types, also different power operating points have to be considered in a next step. Especially the use of the converter modules in a series connection of a phase string requires an optimization conducted not only for a wide power range but also for a limited voltage range to ensure the controllability for balancing the SOCs of the batteries in case of a battery energy storage system. Moreover, the models applied in the optimization could be extended in terms of additional transformer geometries, the variation of several core materials and winding wires as well as the integration of further reference components for the MOSFETs, the IGBTs and the capacitors.

In general, phase-modular AC-DC converter systems could gain interest also for low voltage applications as the available semiconductor devices in the low voltage class segment exhibit relatively low switching and conduction losses. With the emerging semiconductor technology in the field of wide band gap devices applying silicon carbide or gallium nitride, ultra-efficient and ultra-compact converter modules could be realized.

A

DC-DC Dual Active Bridge Converter

This appendix summarizes state-of-the-art modulation schemes for DC-DC dual active bridge (DAB) converters. These are the phase shift modulation, the trapezoidal current mode modulation and the triangular current mode modulation. Based on the developed general power flow modeling in Section 5.4, a design example of a DC-DC DAB is optimized concerning the major converter losses in order to determine the optimal modulation parameters. The obtained converter efficiencies by applying the optimal modulation are compared to the efficiencies that can be reached by state-of-the-art modulation schemes.

A.1 Converter topology

Fig. A.1 shows the converter topology of a DC-DC DAB converter. The converter consists of a primary and a secondary full-bridge with unidirectional switches. The two full-bridges are connected to the windings of a two-winding transformer and generate high-frequency/medium-frequency (HF/MF) square-wave voltages with amplitudes of the DC port voltages V_1, V_2. The converter is operated by phase shift control where the control variables are the clamping intervals (where $v_1 = 0$ and/or $v_2 = 0$) and the phase shifts of the HF/MF voltages.

For the derivation of the modulation equations and the optimization of the converter, the full-bridges are modeled by HF/MF voltage sources and the transformer only by its primary referred leakage inductance L_σ. The magnetizing inductance L_m of the transformer is assumed to be relatively large, so that magnetizing currents can be neglected for the description of the modulation schemes.

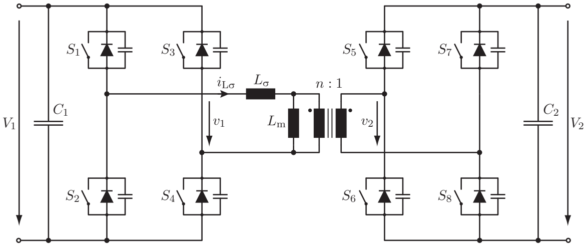


Figure A.1: Topology of the DC-DC dual active bridge (DAB) converter with a primary full-bridge with the switches S_1, S_2, S_3, S_4 and a secondary full-bridge with the switches S_5, S_6, S_7, S_8 connected to a two-winding transformer with leakage inductance L_σ and magnetizing inductance L_m.

A.2 Modulation schemes

In the following, state-of-the-art modulation schemes for a DC-DC DAB converter are summarized and their corresponding power flow equations are given.

A.2.1 Phase shift modulation

In phase shift modulation, square-wave voltages without clamping intervals are applied to the transformer windings as shown in **Fig. A.2**. The power transferred from the primary to the secondary side is controlled by the phase shift ϕ_2 between the two voltages v_1, nv_2 and given by

$$P_{12} = -\frac{V_1 n V_2 \phi_2 (\pi - |\phi_2|)}{\pi \omega_\mathrm{s} L_\sigma} \tag{A.1}$$

with $\phi_2 \in [-\pi, \pi]$. V_1, V_2 are the input and the output voltage, $\omega_\mathrm{s} = \frac{2\pi}{T_\mathrm{s}}$ the angular switching frequency, $n = \frac{N_1}{N_2}$ the turns ratio and L_σ the leakage inductance of the transformer. The maximum transferable power is

$$P_{12,\mathrm{max}} = \pm\frac{\pi V_1 n V_2}{4 \omega_\mathrm{s} L_\sigma}. \tag{A.2}$$

The soft-switching range of the modulation, where zero voltage switching (ZVS) can be achieved, is strongly dependent on the voltage ratio $\frac{V_1}{nV_2}$ as well as the power level P_{12} [142]. Especially for voltage ratios $\frac{V_1}{nV_2} \ll 1$ and $\frac{V_1}{nV_2} \gg 1$ at low loads, ZVS cannot be maintained. Disadvantages like limited soft-switching range and high RMS transformer currents can be overcome by using the trapezoidal current mode modulation explained in the next section.

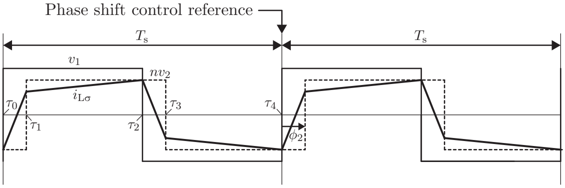


Figure A.2: Square-wave voltages v_1, nv_2 applied to the transformer windings in *phase shift modulation* and resulting leakage inductance current $i_{L\sigma}$.

A.2.2 Trapezoidal current mode modulation

In trapezoidal current mode modulation, square-wave voltages with clamping intervals are applied to the transformer windings as shown in **Fig. A.3** for the general modulation mode. By setting $\tau_0 = \tau_1$ and $\tau_4 = \tau_5$ in **Fig. A.3**, the trapezoidal current mode modulation given in **Fig. A.4** is obtained. The transferred power is then described by

$$P_{12} = -\text{sign}(\phi_2)\frac{V_1 nV_2(\pi\,|\phi_2| - 2\phi_2^2 + 2\delta_1\delta_2)}{\pi\omega_\text{s}L_\sigma} \tag{A.3}$$

with $\delta_1 = f(\phi_2) \in [0, \pi/2]$, $\delta_2 = f(\phi_2) \in [0, \pi/2]$ and $\phi_2 \in [-\pi, \pi]$. The maximum transferable power is

$$P_{12,\text{max}} = \pm\frac{\pi V_1^2 n^2 V_2^2}{2\omega_\text{s}L_\sigma(V_1^2 + n^2V_2^2 + V_1 nV_2)}. \tag{A.4}$$

The current $i_{L\sigma}$ reaches zero at the switching instants τ_0, τ_3, τ_6 where zero current switching (ZCS) is possible [138]. At τ_1, τ_2, τ_4, τ_5 ZVS is possible as far as the minimum commutation current needed for the resonant transition is reached. Nevertheless, the modulation method cannot be applied for low output power. This leads to the triangular current mode modulation with a seamless transition between the modulation methods.

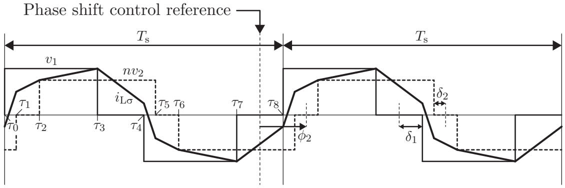

Phase shift control reference
T_s
T_s
v_1
nv_2
$i_{L\sigma}$
τ_0
τ_1
τ_2
τ_3
τ_4
τ_5
τ_6
τ_7
τ_8
ϕ_2
δ_1
δ_2

Figure A.3: Square-wave voltages v_1, nv_2 applied to the transformer windings in *general trapezoidal current mode modulation* and resulting leakage inductance current $i_{L\sigma}$.

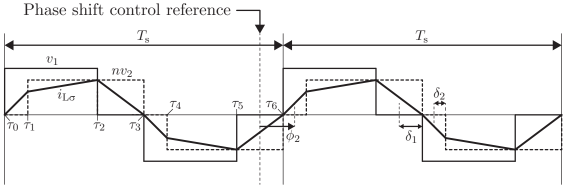

Phase shift control reference
T_s
T_s
v_1
nv_2
$i_{L\sigma}$
τ_0
τ_1
τ_2
τ_3
τ_4
τ_5
τ_6
ϕ_2
δ_1
δ_2

Figure A.4: Square-wave voltages v_1, nv_2 applied to the transformer windings in *trapezoidal current mode modulation* and resulting leakage inductance current $i_{L\sigma}$.

A.2.3 Triangular current mode modulation

In triangular current mode modulation, also square-wave voltages with clamping intervals are applied to the transformer windings as can be seen from **Fig. A.5** for the general modulation mode. Considering $\tau_3 = \tau_4$ and $\tau_7 = \tau_8$ in **Fig. A.5(a)** as well as $\tau_2 = \tau_3$ and $\tau_6 = \tau_7$ in **Fig. A.5(b)**, the triangular current mode modulation shown in **Fig. A.6** is obtained. The transferred power can then be written as

$$P_{12} = -\frac{V_1 n V_2 \phi_2 (\pi - 2\delta_1)}{\pi \omega_s L_\sigma} \qquad V_1 > nV_2, \tag{A.5}$$

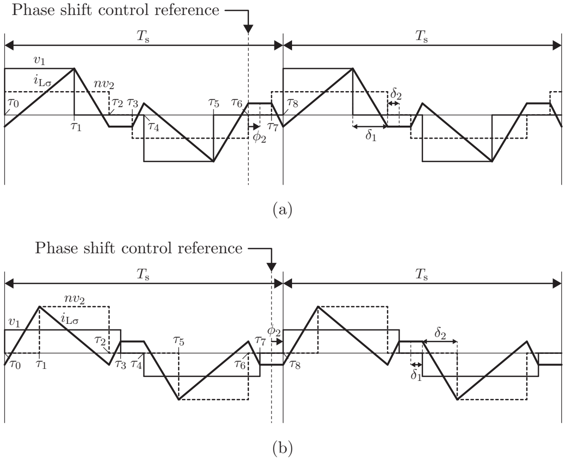
$$P_{12} = -\frac{V_1 n V_2 \phi_2 (\pi - 2\delta_2)}{\pi \omega_s L_\sigma} \qquad V_1 < nV_2 \tag{A.6}$$

with $\delta_1 = f(\phi_2) \in [0, \pi/2]$, $\delta_2 = f(\phi_2) \in [0, \pi/2]$ and $\phi_2 \in [-\pi, \pi]$. The maximum transferable power is

$$P_{12,\max} = \pm \frac{\pi n^2 V_2^2 \left(V_1 - nV_2\right)}{2\omega_{\mathrm{s}} L_\sigma V_1} \qquad V_1 > nV_2, \tag{A.7}$$

$$P_{12,\max} = \pm \frac{\pi V_1^2 \left(V_1 - nV_2\right)}{2\omega_{\mathrm{s}} L_\sigma n V_2} \qquad V_1 < nV_2. \tag{A.8}$$

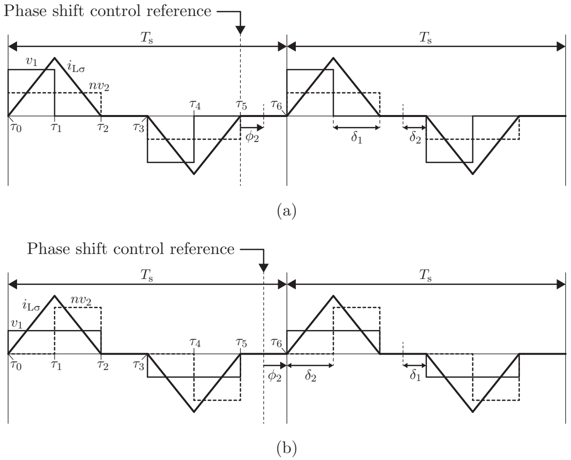
The current $i_{\mathrm{L}\sigma}$ reaches zero at the switching instants τ_0, τ_2, τ_3, τ_5, τ_6 where ZCS is possible [138]. At the instants τ_1, τ_4 ZVS is possible. Depending on the voltage ratio, the modulation shown in **Fig. A.6(a)** with $V_1 > nV_2$ or the modulation shown in **Fig. A.6(b)** with $V_1 < nV_2$ is applied. Power transfer in case of $V_1 = nV_2$ is not possible with the triangular current mode.


Phase shift control reference
T_{s}
T_{s}
v_1
$i_{\mathrm{L}\sigma}$
nv_2
τ_0
τ_1
τ_2
τ_3
τ_4
τ_5
τ_6
τ_7
τ_8
ϕ_2
δ_2
δ_1
Phase shift control reference
T_{s}
T_{s}
nv_2
v_1
$i_{\mathrm{L}\sigma}$
τ_2
τ_5
τ_7
ϕ_2
δ_2
τ_0
τ_1
τ_3
τ_4
τ_6
τ_8
δ_1

(a)

(b)

Figure A.5: Square-wave voltages v_1, nv_2 applied to the transformer windings in *general triangular current mode modulation* and resulting leakage inductance current $i_{\mathrm{L}\sigma}$ for $V_1 > nV_2$ (a) and $V_1 < nV_2$ (b).


Phase shift control reference
T_s
T_s
v_1
$i_{L\sigma}$
nv_2
τ_0
τ_1
τ_2
τ_3
τ_4
τ_5
τ_6
ϕ_2
δ_1
δ_2
Phase shift control reference
T_s
T_s
$i_{L\sigma}$
nv_2
v_1
τ_0
τ_1
τ_2
τ_3
τ_4
τ_5
τ_6
ϕ_2
δ_2
δ_1

(a)

(b)

Figure A.6: Square-wave voltages v_1, nv_2 applied to the transformer windings in *triangular current mode modulation* and resulting leakage inductance current $i_{L\sigma}$ for $V_1 > nV_2$ (a) and $V_1 < nV_2$ (b).

A.3 Converter optimization

For a DC-DC DAB converter design example, the optimal modulation scheme considering all possible degrees of freedom in control (see **Tab. 4.1**) is determined by an optimization of the converter losses. The control variables are the primary and the secondary clamping intervals δ_1, δ_2, the phase shift ϕ_2 as well as the switching frequency f_s. The general power flow equation derived in Section 5.4 is used to include all possible modulation schemes in the optimization process without the need of distinguishing between different mathematical cases for the various possible modulation schemes.

A.3.1 Design example

As a design example to find optimal control variables, a 3.3 kW electric vehicle battery charger to connect to a fixed 400 V DC link with an output voltage range of 280 V to 420 V of a lithium-ion battery is considered. The primary and secondary switching devices are chosen to be 650 V IGBTs of type IKW50N65F5 [166] for a first converter

Table A.1: Parameters of the DC-DC DAB design example.

Input voltage	V_1	400 V
Battery voltage	V_2	280 V. . . 420 V
Output power	P_2	3.3 kW
Switching frequency	f_s	20 kHz. . . 50 kHz
Transformer turns ratio	n	8/7
Transformer leakage inductance	L_σ	
Phase shift modulation	$L_{\sigma(1)}$	181 µH
Triangular/Trapezoidal modulation	$L_{\sigma(2)}$	158 µH
Optimal modulation	$L_{\sigma(3)}$	158 µH
Transformer magnetizing inductance	L_m	neglected

solution and 650 V MOSFETs of type IPW65R019C7 [165] for a second converter solution. The converter parameters are listed in detail in **Tab. A.1**.

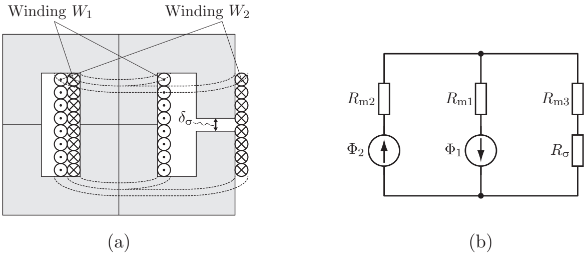


Figure A.7: 2D drawing of the transformer in (a) consisting of four U-cores with the primary winding W_1 wound around the inner leg and the secondary winding W_2 wound around the inner and the right-hand sided stray leg. By inserting an air gap of length δ_σ in the stray leg, the leakage inductance L_σ is adjusted. In (b) the corresponding reluctance model is depicted with flux sources Φ_1 and Φ_2.

The transformer of the design example including its reluctance model is depicted in **Fig. A.7** where the leakage inductance L_σ is adjusted by varying the air gap size δ_σ depending on the modulation scheme, so that the maximum power of 3.3 kW can be transferred at the lowest

Table A.2: Transformer parameters of the DC-DC DAB design example.

Magnetic core	2x AMCC-32 VITROPERM 500F
Primary winding W_1	24 turns, litz wire 945 strands, 0.071 mm
Secondary winding W_2	21 turns, litz wire 945 strands, 0.071 mm
Air gap length δ_σ	
Phase shift modulation	1.6 mm
Triangular/Trapezoidal modulation	1.8 mm
Optimal modulation	1.8 mm

switching frequency of 20 kHz and the lowest battery voltage of 280 V. Practically, distributed air gaps are used in order to reduce the losses induced by the fringing magnetic field. For the optimization, the leakage inductance is fixed at the lower value of the two values obtained for phase shift and triangular/trapezoidal modulation since the optimization algorithm is then capable of choosing from these two without the need of increasing the switching frequency. The turns ratio is set so that the average battery voltage of 350 V transforms to a primary voltage of 400 V.

The transformer is built with four U-cores of the size AMCC-32 [150] with the nanocrystalline material VITROPERM 500F [151] which exhibits a relatively high saturation flux density of 1.2 T and is therefore ideally suited for switching frequencies in the range of a few 10 kHz. For the windings, litz wire with 945 strands of diameter 0.071 mm is used. At the primary side, there are 24 turns, whereas the secondary winding consists of 21 turns. The primary winding W_1 is directly wound on the inner leg with the secondary winding W_2 around the inner leg and the outer stray leg as shown in **Fig. A.7**. The transformer parameters are summarized in **Tab. A.2**.

A.3.2 Optimization procedure

The optimal control variables in terms of the clamping intervals δ_1, δ_2, the phase shift ϕ_2 and the switching frequency f_s are numerically determined by minimizing the total converter losses subject to the power flow constraint. The converter loss model includes the main loss shares as conduction and switching losses of the semiconductor devices, skin and proximity effect losses of the transformer windings as well as the core losses of the transformer and a constant part for auxiliary losses (semiconductor losses P_{sw}, transformer losses P_{tr}, auxiliary losses P_{aux}).

For the semiconductor devices, both the IGBT and the MOSFET loss models are based on data sheet parameters and described in Section B.1.1 and Section B.1.2 respectively. The gate drive losses are modeled according to Section B.1.3. The transformer loss models are given in Section B.2.1 for the litz wire winding losses and in Section B.2.2 for the core losses. Besides the load-dependent loss shares, a constant loss share of 8 W for the control, the sensing and the fans is considered.

The optimization procedure is shown in **Fig. A.8**. For a given set of output voltage $V_2 \in [280\,\mathrm{V}, 420\,\mathrm{V}]$ and a reference output power $P_{12}^{*} \in [0.33\,\mathrm{kW}, 3.3\,\mathrm{kW}]$, the optimization routine calculates the optimal control variables. The optimization problem is stated as

$$\min_{x} \left[P_{\mathrm{sw}} + P_{\mathrm{tr}} + P_{\mathrm{aux}}\right] \tag{A.9}$$

with respect to

$$x = \begin{bmatrix} \delta_1 \\ \delta_2 \\ \phi_2 \\ f_{\mathrm{s}} \end{bmatrix} \tag{A.10}$$

with

$$x_{\mathrm{lb}} = \begin{bmatrix} 0 \\ 0 \\ -\pi \\ 20\,\mathrm{kHz} \end{bmatrix}, \; x_{\mathrm{ub}} = \begin{bmatrix} \frac{\pi}{2} \\ \frac{\pi}{2} \\ \pi \\ 50\,\mathrm{kHz} \end{bmatrix} \tag{A.11}$$

where x denotes the vector of control variables which is restricted to the lower and upper bounds x_{lb}, x_{ub} respectively. The equality constraint is given by setting the power transfer $P_{12} = P_{12}^{*}$ using the general power flow equation (5.30).

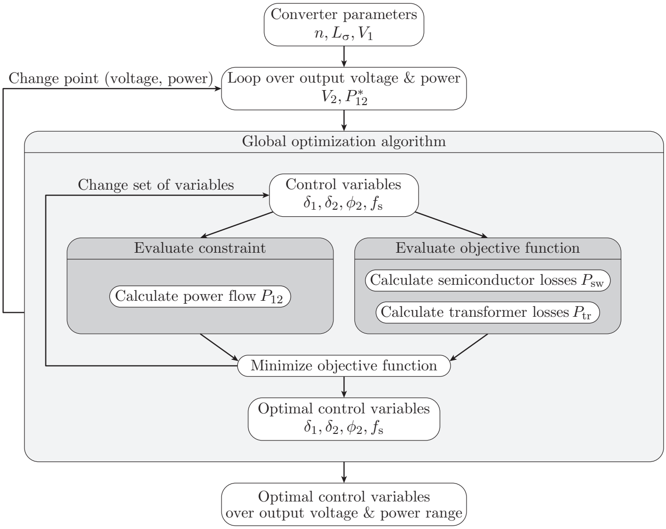

Converter parameters
n, L_σ, V_1
Change point (voltage, power)
Loop over output voltage & power
V_2, P_{12}^*
Global optimization algorithm
Change set of variables
Control variables
$\delta_1, \delta_2, \phi_2, f_s$
Evaluate constraint
Calculate power flow P_{12}
Evaluate objective function
Calculate semiconductor losses P_{sw}
Calculate transformer losses P_{tr}
Minimize objective function
Optimal control variables
$\delta_1, \delta_2, \phi_2, f_s$
Optimal control variables
over output voltage & power range

Figure A.8: Flow chart of the optimization algorithm to find the optimal control variables δ_1, δ_2, ϕ_2, f_s by minimizing the DC-DC DAB converter losses subject to the power flow constraint. P_{12}^* represents the reference value for the transferred power.

A.3.3 Optimization results

In the following, the optimization results for the IGBT and the MOSFET DAB design example with parameters from **Tab. A.1** are given and discussed. The optimization is carried out without considering modulation mode transitions. For a practical implementation, the transition phases between the modes play an important role since steps in the control variables can lead to the short-term loss of soft-switching and require special care in the switching signals state machine implementation.

IGBT solution

The relative converter efficiencies for the IGBT solution obtained from the optimization are shown in **Fig. A.9(a)** with the variation of the switching frequency depicted in **Fig. A.9(b)**. Additionally, the converter efficiencies for the phase shift and the combined triangular/trapezoidal current mode modulation are given in **Fig. A.10**.

MOSFET solution

The relative converter efficiencies for the MOSFET solution obtained from the optimization are shown in **Fig. A.11(a)** with the variation of the switching frequency depicted in **Fig. A.11(b)**. Additionally, the converter efficiencies for the phase shift and the combined triangular/trapezoidal current mode modulation are given in **Fig. A.12**.

Discussion

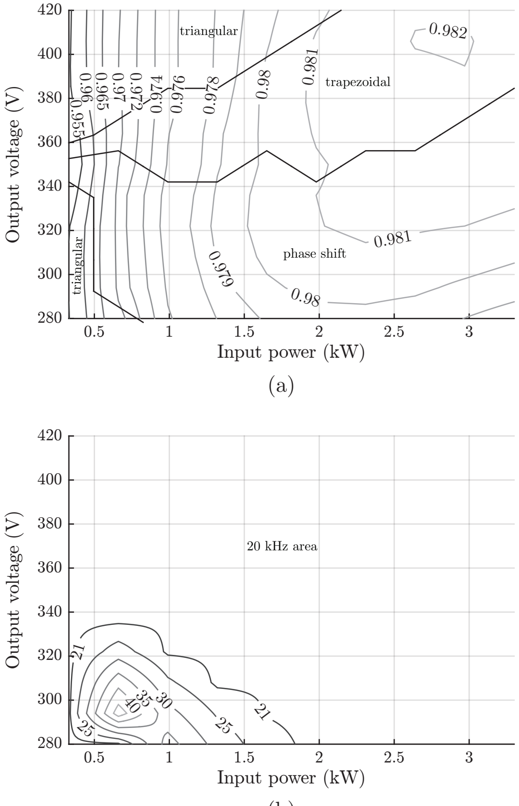
For the phase shift modulation, it can be seen that for the MOSFET solution in the soft-switching area higher efficiencies are achieved than for the IGBT solution (compare **Fig. A.12(a)** to **Fig. A.10(a)**). This is mainly due to the fact, that IGBT turn-off losses cannot be substantially reduced by using ZVS. In the hard-switching region, ZVS is lost and forced diode commutations occur. The switching losses in this region are strongly dependent on the characteristics of the antiparallel diode of the IGBT and the body diode of the MOSFET respectively.

To improve the efficiencies, especially in the hard-switching region, the combined triangular/trapezoidal current mode modulation can be used. There, also for a low output power in the areas of low and high output voltages, soft-switching (ZCS combined with ZVS) can be achieved.

Considering also the switching frequency variation, the efficiencies can be slightly increased compared to the triangular/trapezoidal current mode modulation. Soft-switching is achieved in the whole operating range: ZCS and ZVS for the IGBT solution and only ZVS for the MOSFET solution. The modulation modes, which are found by the optimization procedure, are given in **Fig. A.9(a)** and **Fig. A.11(a)**.

The resulting switching frequencies found by the optimization are shown in **Fig. A.9(b)** for the IGBT and in **Fig. A.11(b)** for the MOSFET solution.

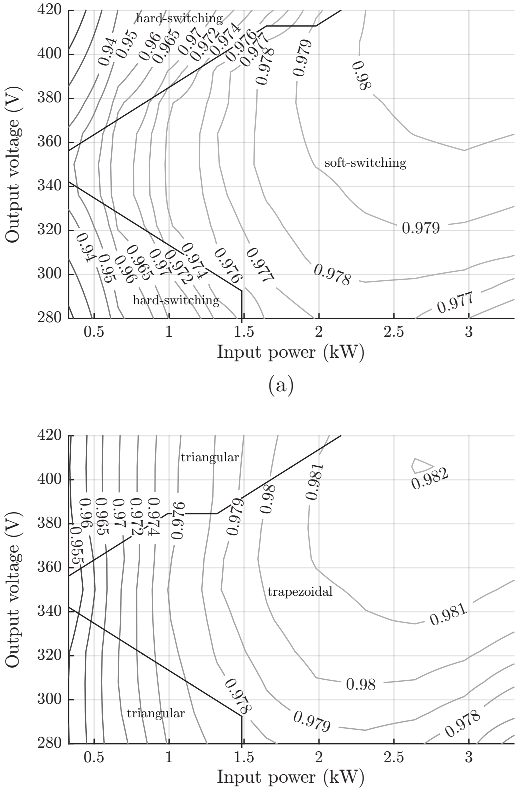
Especially for the MOSFET solution, the frequency is varied over a wide area of the operating range. With decreasing power, the frequency can be increased to lower the power transfer and to achieve high efficiencies at the same time. Nevertheless, at low input power, it is more attractive to decrease the switching frequency and change the modulation mode when necessary.



(a)

(b)

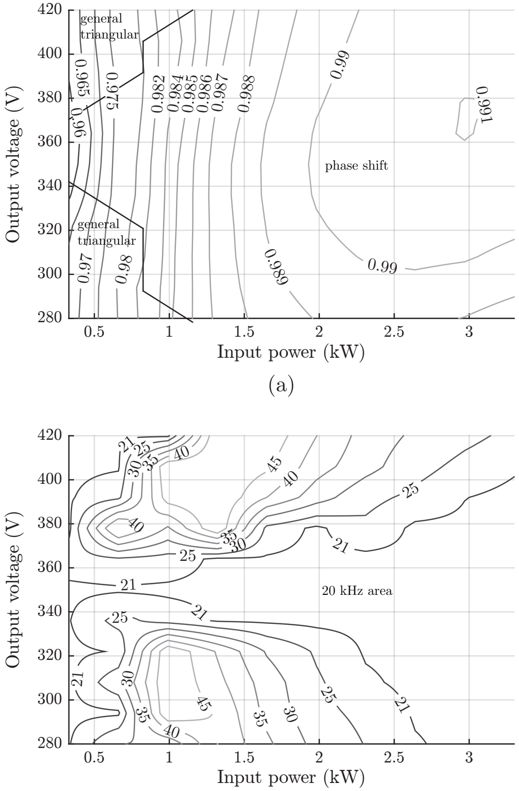
Figure A.9: Relative converter efficiencies applying IGBTs for an input power range of 10 % to 100 % of maximum input power and an output voltage range of 280 V to 420 V for the modulation with optimized control variables with variable switching frequency from 20 kHz to 50 kHz (a) where also the modulation mode found by the optimization is given (soft-switching with either ZCS or ZVS is always achieved). In (b) the switching frequencies in kHz of the optimized control variables are depicted.



(a)

(b)

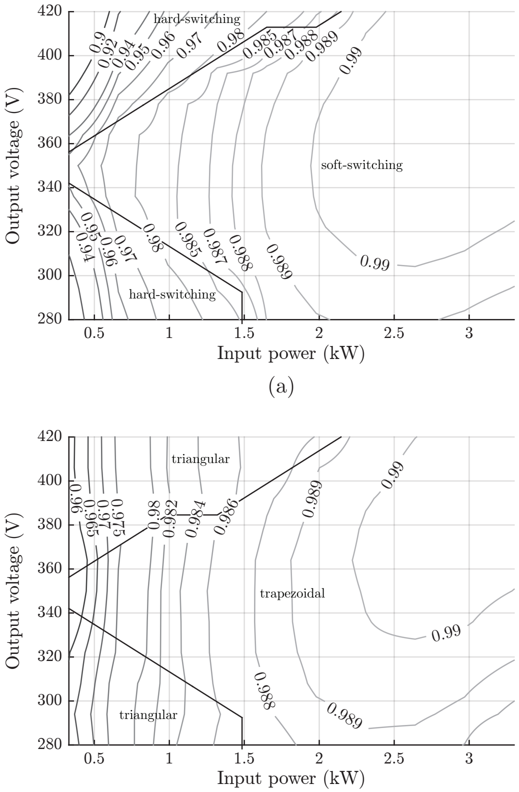
Figure A.10: Relative converter efficiencies applying IGBTs for an input power range of 10 % to 100 % of maximum input power and an output voltage range of 280 V to 420 V for the phase shift modulation (a) and the triangular/trapezoidal current mode modulation (b) both with fixed switching frequency at 20 kHz. For the phase shift modulation in (a), soft- and hard-switching areas are given, whereas with the modulation in (b) soft-switching (either ZCS or ZVS) is always achieved.



(a)

(b)

Figure A.11: Relative converter efficiencies applying MOSFETs for an input power range of 10 % to 100 % of maximum input power and an output voltage range of 280 V to 420 V for the modulation with optimized control variables with variable switching frequency from 20 kHz to 50 kHz (a) where also the modulation mode found by the optimization is given (soft-switching with either ZCS or ZVS is always achieved). In (b) the switching frequencies in kHz of the optimized control variables are depicted.



(a)

(b)

Figure A.12: Relative converter efficiencies applying MOSFETs for an input power range of 10 % to 100 % of maximum input power and an output voltage range of 280 V to 420 V for the phase shift modulation (a) and the triangular/trapezoidal current mode modulation (b) both with fixed switching frequency at 20 kHz. For the phase shift modulation in (a), soft- and hard-switching areas are given, whereas with the modulation in (b) soft-switching (either ZCS or ZVS) is always achieved.

B

Loss Models of Power Components

This appendix describes the loss models of the power components which are used in the optimizations and calculations throughout this thesis. For the semiconductor devices, the inductive components and the capacitors, the models are presented in the following.

B.1 Semiconductor devices

For the widely used semiconductor technologies of IGBTs and MOSFETs, the applied loss models are based on data sheet parameters from the manufacturers. The estimated losses are calculated with the data available at the highest junction temperature in order to allow a compact heat sink design.

B.1.1 IGBT losses

The conduction and switching losses of an IGBT device with an antiparallel diode are modeled based on the available data sheet parameters of the manufacturers and are given in the following.

Conduction losses

For calculating the conduction losses, the typical output characteristic $i_{\mathrm{C}} = f(v_{\mathrm{CE}})$ of the IGBT and the typical diode forward current as a function of the forward voltage $i_{\mathrm{D}} = f(v_{\mathrm{D}})$ of the antiparallel diode at a junction temperature of $T_{\mathrm{j,max}} - 25\,^{\circ}\mathrm{C} = 150\,^{\circ}\mathrm{C}$ from the data sheet are considered. Given the current i_{C} flowing through the IGBT and the current i_{D} through the diode over the interval $[0, T_{\mathrm{s}}]$ of a switching period T_s, the conduction losses of an IGBT co-pack device can be calculated by

$$P_{\mathrm{c,S}} = \frac{1}{T_\mathrm{s}} \int_0^{T_\mathrm{s}} i_\mathrm{C}(\tau) \cdot v_\mathrm{CE}(i_\mathrm{C}(\tau))\, \mathrm{d}\tau, \tag{B.1}$$

$$P_{\mathrm{c,D}} = \frac{1}{T_\mathrm{s}} \int_0^{T_\mathrm{s}} i_\mathrm{D}(\tau) \cdot v_\mathrm{D}(i_\mathrm{D}(\tau))\, \mathrm{d}\tau, \tag{B.2}$$

$$P_\mathrm{c} = P_{\mathrm{c,S}} + P_{\mathrm{c,D}}. \tag{B.3}$$

Switching losses

When optimizing and designing a converter system, the final layout of the gate drive circuit and the parasitics of the commutation path are usually unknown, so that only approximations of the switching losses can be performed. For estimating the switching losses of an IGBT co-pack device, the following assumptions are made: For a device which is turned on

- the diode losses at zero-voltage turn-on are neglected,
- the IGBT losses $E_\mathrm{on} = f(i_\mathrm{C})$ at turn-on including the diode reverse recovery losses are taken from the data sheet and are linearly scaled with the voltage according to the data sheet.

For a device which is turned off

- the diode losses at turn-off are neglected,
- the IGBT losses $E_\mathrm{off} = f(i_\mathrm{C})$ at turn-off including the tail current losses are taken from the data sheet and are linearly scaled with the voltage according to the data sheet.

For soft-switching in terms of ZVS at the switching instant τ_s, the switching losses of an IGBT co-pack device are approximated by

$$P_\mathrm{s} = f_\mathrm{s} \cdot E_\mathrm{off}(i_\mathrm{C}(\tau_\mathrm{s})) \frac{v_\mathrm{CE}(\tau_\mathrm{s})}{V_\mathrm{CE}} \tag{B.4}$$

whereas for hard-switching in terms of forced diode commutation, the switching losses are estimated according to

$$P_\mathrm{s} = f_\mathrm{s} \cdot E_\mathrm{on}(i_\mathrm{C}(\tau_\mathrm{s})) \frac{v_\mathrm{CE}(\tau_\mathrm{s})}{V_\mathrm{CE}} \tag{B.5}$$

with V_{CE} being the collector-emitter voltage where the switching losses were measured according to the data sheet. For soft-switching in terms of ZCS for a small $i_{\mathrm{C}}(\tau_{\mathrm{s}})$, the losses according to (B.4) and (B.5) become negligible small.

B.1.2 MOSFET losses

The two loss shares of conduction and switching losses of a MOSFET device are modeled based on the available data sheet parameters of the manufacturers and are given in the following.

Conduction losses

For MOSFETs, the typical output characteristic $i_{\mathrm{D}} = f(v_{\mathrm{DS}})$ at a junction temperature of $T_{\mathrm{j,max}} - 25\,^{\circ}\mathrm{C} = 125\,^{\circ}\mathrm{C}$ from the data sheet can be used to calculate the conduction losses. Given the current i_{D} flowing through the MOSFET over the interval $[0, T_{\mathrm{s}}]$ of a switching period T_{s}, the conduction losses are given by

$$P_{\mathrm{c}} = \frac{1}{T_{\mathrm{s}}} \int_0^{T_{\mathrm{s}}} i_{\mathrm{D}}(\tau) \cdot v_{\mathrm{DS}}(i_{\mathrm{D}}(\tau))\, \mathrm{d}\tau. \tag{B.6}$$

Switching losses

The approximation of the switching losses of a MOSFET device is based on the following assumptions: For ZVS conditions when stored energy in the output capacitance is transferred from one MOSFET to another, only the turn-off losses are considered. The turn-on of the body diode after the resonant transition is assumed to be lossless. The turn-off losses $E_{\mathrm{off}} = f(i_{\mathrm{D}})$ at the time instant τ_{s} are linearly scaled with the drain-source voltage v_{DS} and given by

$$P_{\mathrm{s}} = f_{\mathrm{s}} \cdot E_{\mathrm{off}}(i_{\mathrm{D}}(\tau_{\mathrm{s}})) \frac{v_{\mathrm{DS}}(\tau_{\mathrm{s}})}{V_{\mathrm{DS}}} \tag{B.7}$$

with V_{DS} being the drain-source voltage where the switching losses were measured according to the data sheet. For hard-switching, two loss effects are modeled, these are

- the dissipation of the energy $E_{\mathrm{oss}} = f(v_{\mathrm{DS}})$ stored in the output capacitance at turn-on,

- the body diode reverse recovery losses occurring in the turn-on device squarely scaled with the voltage and linearly scaled with the current [173].

The switching losses at the time instant τ_s are then estimated using

$$P_\mathrm{oss} = f_\mathrm{s} \cdot E_\mathrm{oss}(v_\mathrm{DS}(\tau_\mathrm{s})), \tag{B.8}$$

$$P_\mathrm{rr} = f_\mathrm{s} \cdot Q_\mathrm{rr} \left(\frac{v_\mathrm{DS}(\tau_\mathrm{s})}{V_\mathrm{R}} \right)^2 \frac{i_\mathrm{D}(\tau_\mathrm{s})}{I_\mathrm{F}} \cdot v_\mathrm{DS}(\tau_\mathrm{s}), \tag{B.9}$$

$$P_\mathrm{s} = P_\mathrm{oss} + P_\mathrm{rr} \tag{B.10}$$

with the curve $E_\mathrm{oss} = f(v_\mathrm{DS})$ and the reverse recovery charge Q_rr measured for the reverse voltage V_R and the forward current I_F from the data sheet. For soft-switching in terms of ZCS for a small $i_\mathrm{D}(\tau_\mathrm{s})$, the losses according to (B.9) become negligible small, hence the losses are mainly described by (B.8).

B.1.3 Gate drive losses

The gate drive losses per switching device can be calculated by the difference between the energy that the gate driver delivers during the charging process of the gate and the stored energy in the gate of the device at the end of the turn-on. The energy loss for a switching cycle is then given by

$$E_\mathrm{g} = 2 \cdot \left(\int V_\mathrm{g} i_\mathrm{g}(t) \, \mathrm{d}t - \frac{1}{2} Q_\mathrm{g} V_\mathrm{g} \right) = Q_\mathrm{g} V_\mathrm{g} \tag{B.11}$$

with the total gate charge depending on the gate current $i_\mathrm{g}(t)$

$$Q_\mathrm{g} = \int i_\mathrm{g}(t) \, \mathrm{d}t \tag{B.12}$$

and V_g being the gate driver voltage. With the total gate charge Q_g from the data sheet, the gate drive losses are calculated by

$$P_\mathrm{g} = f_\mathrm{s} E_\mathrm{g} = f_\mathrm{s} Q_\mathrm{g} V_\mathrm{g}. \tag{B.13}$$

B.2 Inductive components

The losses in inductive components such as inductors and transformers comprising the loss mechanisms in the windings and the magnetic core are modeled in the following. For the winding losses several types of conductors are considered.

B.2.1 Winding losses

The skin effect losses including the DC losses and the proximity effect losses are described by the state-of-the-art models presented in [174, 175]. Below, the loss models for foil and round conductor windings as well as litz wire windings are summarized.

Foil conductor

The skin effect losses including DC losses per unit length in foil conductors for each current harmonic are calculated according to [174, 175] by

$$P_\mathrm{S} = R_\mathrm{DC} F_\mathrm{F}(f) \hat{I}^2 \tag{B.14}$$

with

$$\delta = \frac{1}{\sqrt{\pi \mu_0 \sigma f}}, \tag{B.15}$$

$$\nu = \frac{h}{\delta}, \tag{B.16}$$

$$R_\mathrm{DC} = \frac{1}{\sigma b h} \tag{B.17}$$

and

$$F_\mathrm{F} = \frac{\nu}{4} \frac{\sinh \nu + \sin \nu}{\cosh \nu - \cos \nu} \tag{B.18}$$

where δ is the skin depth, f the frequency of the considered current harmonic with amplitude $\hat{I}$, h the thickness and b the width of the foil and σ the conductivity of copper.

The proximity effect losses per unit length in foil conductors for each magnetic field harmonic are calculated according to [174, 175] by

$$P_\mathrm{P} = R_\mathrm{DC} G_\mathrm{F}(f) \hat{H}_\mathrm{e}^2 \tag{B.19}$$

with

$$\delta = \frac{1}{\sqrt{\pi \mu_0 \sigma f}}, \tag{B.20}$$

$$\nu = \frac{h}{\delta}, \tag{B.21}$$

$$R_{\mathrm{DC}} = \frac{1}{\sigma b h} \tag{B.22}$$

and

$$G_{\mathrm{F}} = b^2 \nu \frac{\sinh \nu - \sin \nu}{\cosh \nu + \cos \nu}. \tag{B.23}$$

The external magnetic field strength for calculating proximity effect losses is derived by a 1D approximation according to [176] as depicted in **Fig. B.1**.

The total foil conductor winding losses are given by the sum of the described loss mechanisms

$$P_{\mathrm{W}} = P_{\mathrm{S}} + P_{\mathrm{P}}. \tag{B.24}$$

Round conductor

The skin effect losses including DC losses per unit length in round conductors for each current harmonic are calculated according to [174, 175] by

$$P_{\mathrm{S}} = R_{\mathrm{DC}} F_{\mathrm{R}}(f) \hat{I}^2 \tag{B.25}$$

with

$$\delta = \frac{1}{\sqrt{\pi \mu_0 \sigma f}}, \tag{B.26}$$

$$\xi = \frac{d}{\sqrt{2}\delta}, \tag{B.27}$$

$$R_{\mathrm{DC}} = \frac{4}{\sigma \pi d^2} \tag{B.28}$$

and

$$\begin{aligned} F_{\mathrm{R}} = & \frac{\xi}{4\sqrt{2}} \left(\frac{\mathrm{ber}_0(\xi)\mathrm{bei}_1(\xi) - \mathrm{ber}_0(\xi)\mathrm{ber}_1(\xi)}{\mathrm{ber}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2} \right. \\ & \left. - \frac{\mathrm{bei}_0(\xi)\mathrm{ber}_1(\xi) + \mathrm{bei}_0(\xi)\mathrm{bei}_1(\xi)}{\mathrm{ber}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2} \right) \end{aligned} \tag{B.29}$$

where δ is the skin depth, f the frequency of the considered current harmonic with amplitude $\hat{I}$, d the conductor diameter and σ the conductivity of copper.

The proximity effect losses per unit length in round conductors for each magnetic field harmonic are calculated according to [174, 175] by

$$P_{\mathrm{P}} = R_{\mathrm{DC}} G_{\mathrm{R}}(f) \hat{H}_{\mathrm{e}}^2 \tag{B.30}$$

with

$$\delta = \frac{1}{\sqrt{\pi \mu_0 \sigma f}}, \tag{B.31}$$

$$\xi = \frac{d}{\sqrt{2}\delta}, \tag{B.32}$$

$$R_{\mathrm{DC}} = \frac{4}{\sigma \pi d^2} \tag{B.33}$$

and

$$\begin{aligned} G_{\mathrm{R}} = - & \frac{\xi \pi^2 d^2}{2\sqrt{2}} \left(\frac{\mathrm{ber}_2(\xi)\mathrm{ber}_1(\xi) + \mathrm{ber}_2(\xi)\mathrm{bei}_1(\xi)}{\mathrm{ber}_0(\xi)^2 + \mathrm{bei}_0(\xi)^2} \right. \\ & \left. + \frac{\mathrm{bei}_2(\xi)\mathrm{bei}_1(\xi) - \mathrm{bei}_2(\xi)\mathrm{ber}_1(\xi)}{\mathrm{ber}_0(\xi)^2 + \mathrm{bei}_0(\xi)^2} \right). \end{aligned} \tag{B.34}$$

The external magnetic field strength for calculating proximity effect losses is derived by a 1D approximation according to [176] as depicted in **Fig. B.1**.

The total round conductor winding losses are given by the sum of the described loss mechanisms

$$P_{\mathrm{W}} = P_{\mathrm{S}} + P_{\mathrm{P}}. \tag{B.35}$$

Litz wire

The skin effect losses including DC losses per unit length in litz wires with N_{s} strands for each current harmonic are calculated according to [174, 175] by

$$P_{\mathrm{S}} = N_{\mathrm{s}} R_{\mathrm{DC}} F_{\mathrm{R}}(f) \frac{\hat{I}^2}{N_{\mathrm{s}}^2} \tag{B.36}$$

with

$$\delta = \frac{1}{\sqrt{\pi \mu_0 \sigma f}}, \tag{B.37}$$

$$\xi = \frac{d_\mathrm{s}}{\sqrt{2}\delta}, \tag{B.38}$$

$$R_\mathrm{DC} = \frac{4}{\sigma \pi d_\mathrm{s}^2} \tag{B.39}$$

and

$$\begin{aligned} F_\mathrm{R} = & \frac{\xi}{4\sqrt{2}} \left(\frac{\mathrm{ber}_0(\xi)\mathrm{bei}_1(\xi) - \mathrm{ber}_0(\xi)\mathrm{ber}_1(\xi)}{\mathrm{ber}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2} \right. \\ & \left. - \frac{\mathrm{bei}_0(\xi)\mathrm{ber}_1(\xi) + \mathrm{bei}_0(\xi)\mathrm{bei}_1(\xi)}{\mathrm{ber}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2} \right) \end{aligned} \tag{B.40}$$

where δ is the skin depth, f the frequency of the considered current harmonic with amplitude $\hat{I}$, d_s the strand diameter and σ the conductivity of copper.

The proximity effect losses in a litz wire are split into an external and an internal part. External proximity effect losses are caused by the magnetic field of the adjacent litz wires whereas the internal proximity effect losses originate from the magnetic field of the single strands in the litz bundle itself.

The external and internal proximity effect losses per unit length in litz wires with N_s strands and an outer diameter d_o for each magnetic field harmonic are calculated according to [174, 175] by

$$P_\mathrm{P,ext} = N_\mathrm{s} R_\mathrm{DC} G_\mathrm{R}(f) \hat{H}_\mathrm{e}^2, \tag{B.41}$$

$$P_\mathrm{P,int} = N_\mathrm{s} R_\mathrm{DC} G_\mathrm{R}(f) \frac{\hat{I}^2}{2\pi^2 d_\mathrm{o}^2} \tag{B.42}$$

with

$$\delta = \frac{1}{\sqrt{\pi \mu_0 \sigma f}}, \tag{B.43}$$

$$\xi = \frac{d_\mathrm{s}}{\sqrt{2}\delta}, \tag{B.44}$$

$$R_\mathrm{DC} = \frac{4}{\sigma \pi d_\mathrm{s}^2} \tag{B.45}$$

and

$$G_\mathrm{R} = - \frac{\xi \pi^2 d_\mathrm{s}^2}{2\sqrt{2}} \left(\frac{\mathrm{ber}_2(\xi)\mathrm{ber}_1(\xi) + \mathrm{ber}_2(\xi)\mathrm{bei}_1(\xi)}{\mathrm{ber}_0(\xi)^2 + \mathrm{bei}_0(\xi)^2} \right.$$

$$+\frac{\mathrm{bei}_2(\xi)\mathrm{bei}_1(\xi)-\mathrm{bei}_2(\xi)\mathrm{ber}_1(\xi)}{\mathrm{ber}_0(\xi)^2+\mathrm{bei}_0(\xi)^2}\Bigg). \tag{B.46}$$

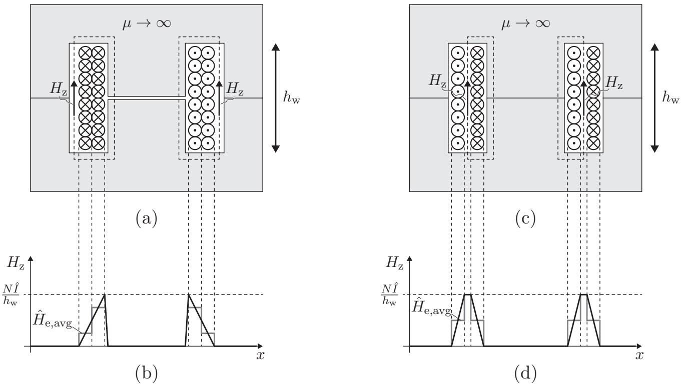
The external magnetic field strength for calculating proximity effect losses is derived by a 1D approximation according to [176] as depicted in **Fig. B.1**.

The total litz wire winding losses are given by the sum of the described loss mechanisms

$$P_\mathrm{W}=P_\mathrm{S}+P_\mathrm{P,ext}+P_\mathrm{P,int}. \tag{B.47}$$

Magnetic field approximation

For the calculation of the proximity effect losses, the external magnetic field strength $\hat{H}_\mathrm{e}$ induced by each current harmonic $\hat{I}$ has to be determined. This is done by a 1D approximation according to [176] as shown in **Fig. B.1** where it is assumed that the magnetic field exhibits only a component in the axial z-direction of the cylindrical coils. This approach leads to good approximations as long as the (distributed) air gaps are kept relatively small and the turns exhibit a certain distance from the air gaps [177].



(a)

(b)

(c)

(d)

Figure B.1: 2D drawing of an inductor consisting of two E-cores with N number of turns (a) where the 1D magnetic field approximation is given in (b). In (c) the 2D drawing of a transformer consisting of two E-cores with N number of turns per winding is shown with the 1D magnetic field approximation given in (d).

The magnetic field component H_z is approximated by a linear function in the radial x-direction inside the winding layers as depicted in **Fig. B.1(b)** and **Fig. B.1(d)**. For the proximity effect loss calculation, the magnetic field is then described by its average value per winding layer

$$\hat{H}_\mathrm{e,avg} = \frac{2m-1}{2}\frac{n_\mathrm{T}\hat{I}}{h_\mathrm{w}} \quad m = \{1,\ldots,n_\mathrm{L}\} \tag{B.48}$$

with $\hat{I}$ being the amplitude of the considered current harmonic, n_T the number of turns per layer, h_w the window height of the core and m the index of the winding layer which is iterated from 1 up to the number of layers n_L.

More sophisticated approaches use 2D magnetic field models as for instance the mirror method described in [175] or a finite element method (FEM) analysis for considering also the fringing field of air gaps.

B.2.2 Core losses

The losses occurring in the magnetic core are caused by the magnetic flux induced either by the winding current $i(t)$ as in the case of an inductor or a current-fed transformer or by the applied voltage $v(t)$ across the winding in the case of a voltage-fed transformer.

For an inductor with a given inductance value L, the flux density in the core is given by

$$B(t) = \frac{\Phi(t)}{A_\mathrm{e}} = \frac{\Psi(t)}{NA_\mathrm{e}} = \frac{L}{NA_\mathrm{e}}i(t) \tag{B.49}$$

and is directly proportional to the winding current $i(t)$ assuming an operation in the linear region of the core material (BH-curve) with a current-independent L. For a voltage-fed transformer the flux density depends on the impressed voltage $v(t)$ at the winding and can be written as

$$B(t) = \frac{\Phi(t)}{A_\mathrm{e}} = \frac{\Psi(t)}{NA_\mathrm{e}} = \frac{1}{NA_\mathrm{e}}\int_0^t v(\tau)\ \mathrm{d}\tau. \tag{B.50}$$

A_e defines the core cross section area and N is the number of turns of the winding exciting the magnetic flux.

With the time-dependent magnetic flux density $B(t)$, the core losses per volume are calculated by applying the improved generalized Steinmetz equation (iGSE) according to [178] with

$$P_\mathrm{C} = \frac{1}{T} \int_0^T k_\mathrm{i} \left| \frac{\mathrm{d}B}{\mathrm{d}t} \right|^\alpha (\Delta B)^{\beta-\alpha} \, \mathrm{d}t \tag{B.51}$$

where ΔB is the peak-to-peak flux density and

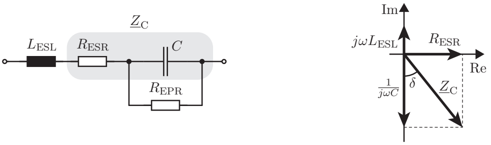
$$k_\mathrm{i} = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^\alpha \, 2^{\beta-\alpha} \, \mathrm{d}\theta}. \tag{B.52}$$

The parameters k, α, β are the same parameters as used in the conventional Steinmetz equation [178].

The losses caused by the minor and major loops [178] are calculated separately by splitting the waveform $B(t)$ into a fundamental component (mostly the 50 Hz component) and one or more medium-/high-frequency (MF/HF) components (mostly the switching frequency component). The single loss parts obtained by this procedure are summed up in the end to the total core losses.

B.3 Capacitors

In capacitors two types of losses occur: The conduction losses (or the ohmic losses) due to the flow of charge through the dielectric and the dielectric losses due to the movement of the atoms/molecules in an alternating electric field [179].



(a) (b)

Figure B.2: Basic equivalent circuit of a capacitor with an equivalent series inductance L_ESL, an equivalent series resistance R_ESR and an equivalent parallel resistance R_EPR in (a) and the corresponding phasor diagram in (b) for a simplified capacitor model with impedance $\underline{Z}_\mathrm{C}$.

Fig. B.2(a) shows the basic equivalent circuit of a capacitor with an equivalent series inductance (ESL) L_ESL, an equivalent series resistance

(ESR) R_{ESR} and an equivalent parallel resistance (EPR) R_{EPR}. The conduction and the dielectric losses are represented by the ESR whereas the EPR models the leakage current through the capacitor under AC or DC bias. In **Fig. B.2(b)**, the phasor diagram of a capacitor is depicted where the ESL is assumed to be negligible small and the EPR negligible large what leads to a simplified capacitor model with the impedance $\underline{Z}_{\mathrm{C}}$.

The capacitor losses including the conduction and the dielectric losses for each current harmonic are then given by

$$P_{\mathrm{C}} = R_{\mathrm{ESR}}(f) I^2(f) \tag{B.53}$$

with $R_{\mathrm{ESR}}(f)$ being the ESR depending on the frequency f from the manufacturers data sheet and $I(f)$ the RMS current of the considered current harmonic. From the dissipation factor $\tan\delta$ given by many manufacturers in their data sheets, the ESR can be calculated with the relation

$$\tan\delta = \frac{R_{\mathrm{ESR}}}{|X_{\mathrm{C}}|} = \frac{R_{\mathrm{ESR}}}{\frac{1}{\omega C}} = R_{\mathrm{ESR}}\omega C \tag{B.54}$$

as shown in **Fig. B.2(b)**.

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