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Hybrid Control Concept for Highly Dynamic Buck Converter Systems

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Keywords

"Current source", "DC-DC converter", "Hybrid control", "Hysteretic control"

Abstract

In this paper, a hybrid control concept for highly dynamic DC-DC buck converter systems in current regulation mode is introduced and described in detail. The controller combines the time-optimal dynamic response and excellent large signal properties of an adaptive hysteretic current controller with the reference tracking and insensitivity to parameter uncertainties of an average current controller (eg. PI control). The control concept is compared with benchmark controllers and its superior transient response as well as disturbance-rejection capability under dynamically changing loads is highlighted.

1 Introduction

Dynamic high power pulsed current sources are required in various modern applications, as for example in fusion reactors for plasma generation [1], beam deflecting equipment in accelerators [2], test equipment for future DC grids [3], or magnetic resonance imaging (MRI) [4]. For designing a flexible current source, which could meet the requirements of different applications, a challenging list of specifications must be fulfilled. In Table II, the most important requirements of a multi-purpose, modular, current source that is suitable for the aforementioned applications, are shown. The single-phase module column refers to the specifications for a single phase DC-DC converter. Parallelizing multiple modules increases the current rating, reduces the current ripple (due to interleaving) and increases the achievable current gradient. The full-scale source column refers to the final requirements with 20 paralleled multi-phase stacks. It should be highlighted that the high current gradient capability and ultra-low current ripple are conflicting specifications regarding the system's design parameters. Furthermore, the need to satisfy those specifications in a wide operating range makes both the converter as well as the controller design, extremely challenging. Therefore, not only the best converter concept must be identified

Table II: Specifications of the modular current source. The full-scale source has 20 parallel multi-phase stacks. Each multi-phase stack has 6 interleaved single phase modules.

	Full-scale source	**Multi-phase stack**	**Single-phase module**
Output current	>30kA	>1.5kA	>0.25kA
Output voltage	>10kV	>10kV	>0.6kV
Current gradient	>200A/µs	>10A/µs	>2A/µs
Flat-top ripple	<0.1%	<1%	<10%
Pulse duration	>20ms	>20ms	>20ms

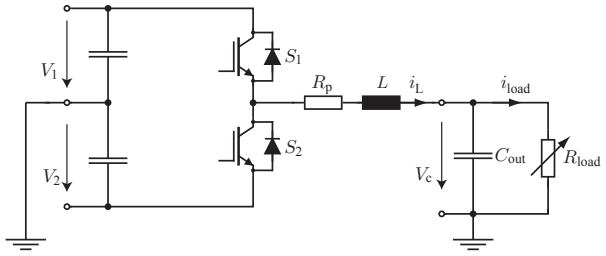

Figure 1: 2L buck converter topology with split DC link (V_1 & V_2), for improved dynamics at low output voltages.

Table I: Buck converter parameters

Output voltage	V_c	0V... 600V
Output current	I	0A ... 400A
Upper voltage level	V_1	675V
Lower voltage level	V_2	125V
Load	R_{load}	0.1Ω ... 1.5Ω
Switching frequency	f_s	20kHz
Inductance	L	230µH
Parasitic resistance	R_p	0.025 Ω
Capacitance	C_{out}	10µF

and optimized but also advanced control methods, that fully exploit the capabilities of the chosen topology, are required.

In [5], a novel current source based on an optimal interleaved current shaping buck converter was presented. The topology choice ensured ultra-low ripple operation and the low inductance provided a fast dynamic response capability. However, the relatively simple current controller limited the achievable current gradient and the robustness of the system under fluctuating loads, especially in case of arcs. Therefore, in this paper alternative control concepts are investigated for a single buck converter cell, aimed to identify the most suitable method for achieving a highly dynamic operation and enhanced disturbance rejection in a wide operating range.

The most common control approach used for buck-type converters is the average current control method that can be applied either by the use of conventional PID control [6] or more sophisticated methods like the state feedback control [7], [8], active disturbance rejection control [9] or H-∞ control [10]. These methods, although inherently different, all share some common characteristics since they rely on the information of the average current in order to provide good reference tracking capability and ensure noise immunity. However, due to the inevitable delays (e.g. sensor, filter, PWM) of the closed loop system, the bandwidth is limited and so are the system's dynamics.

The hysteretic control concept is another common solution for DC-DC converters [11], [12]. The hysteretic control combines simplicity of implementation and excellent robustness to large signal load disturbances with a time-optimal transient performance. However, its conventional digital implementation suffers from variable switching frequency and DC-regulation inaccuracy [13], [14].

Various hybrid controllers have been used successfully in order to combine the advantages of different control schemes and provide an improved performance both in transients and in steady state. A hybrid adaptive controller that uses a PID controller in combination with a sliding mode controller was introduced in [15]. The presented control concept exhibited time-optimal response and good disturbance rejection capability. Although the concept is particularly interesting, its conceptual complexity due to its non-linear nature and high implementation cost makes it impractical, as highlighted in [16]. The hybrid controller in [17] showed improved large signal disturbance rejection capability in voltage regulation mode but did not discuss the disturbance introduced by transients after the non-linear control action. Additionally, in [18] a Model Predictive Control based, constrained optimal hybrid controller was introduced, making use of look-up tables based on a sophisticated model of the converter.

In order to overcome the limitations of those concepts, the combination of a hysteretic controller with an average current control method is presented in this paper. A hybrid combination of these two benchmark control methods offers near-optimal transient behavior, excellent steady state performance and design simplicity with reasonable implementation effort.

In section 2, the operation principle of a single phase buck-type converter is briefly discussed and the topology's maximum dynamic potential is determined. In section 3, a PI control, an observer-based state feedback control and a hysteretic control are briefly described, as benchmark controllers and their limitations are noted. In section 4, the hybrid control concept is presented. Finally, in section 5, the hybrid controller is compared with a PI controller and an observer-based state feedback controller for the buck-type converter shown in Fig. 1.

2 Converter Operation and Maximum Dynamic Potential

In this section, the equations of the buck-type converter are introduced and the effects of the various parameters on the expected performance of the system are shown. There, the focus is laid on the identification of the maximum achievable current gradient in the full operation range (cf. Table I). A modified buck-type topology with split DC link is employed as shown in Fig. 1, in order to ensure current controllability around zero output current and enhanced dynamic performance at low output voltage. Applying the volt-seconds balance, the duty cycle in steady state, as well as the peak-to-peak inductor current ripple can be determined by (1).

$$D = \frac{V_2 + V_c}{V_1 + V_2} \qquad \Delta i_{L,pp} = \frac{1}{L f_s} D(1-D)(V_1 + V_2) \tag{1}$$

The system's dynamics can be described by the system of differential equations in (2), where V_{in} is either V_1 if S_1 is on or V_2 if S_2 is on.

$$L\frac{di_L(t)}{dt} = V_{in} - v_c(t) - R_p i_L(t) \qquad C_{out}\frac{dv_c(t)}{dt} = i_L(t) - \frac{v_c(t)}{R_{load}} \qquad i_{load}(t) = \frac{v_c(t)}{R_{load}} \tag{2}$$

In the frequency domain the load current i_{load} is given by (3).

$$i_{load}(s) = \frac{V_{in}}{(R_{load}C_{out}L)s^2 + (L + R_{load}C_{out}R_p)s + (R_{load} + R_p)} \tag{3}$$

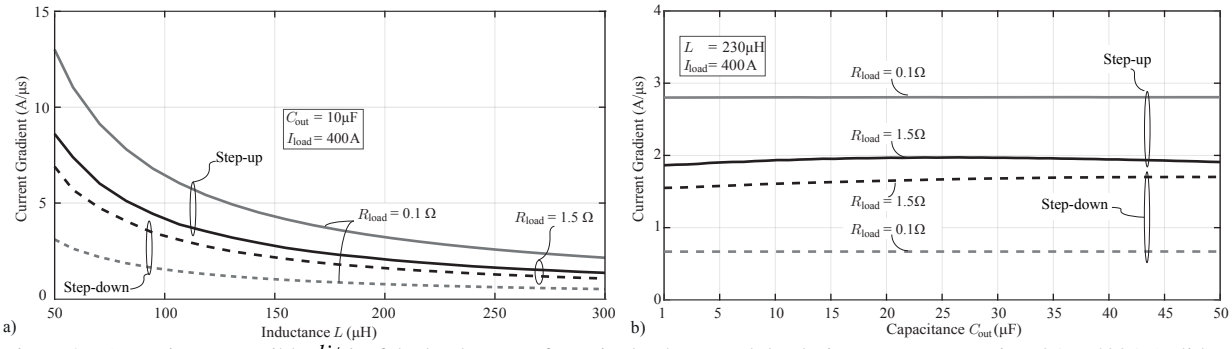

Figure 2: a) Maximum possible di/dt of the load current for a single phase module, during a step-up transient 0A→400A (solid) and step-down transient 400A→0A (dashed) as a function of L for R_{load}=1.5Ω and R_{load}=0.1Ω. b) Maximum possible di/dt of the load current for a single phase module, during a step-up transient 0A→400A (solid) and step-down transient 400A→0A (dashed) as a function of C_{out} for R_{load}=1.5Ω and R_{load}=0.1Ω.

Equation (3) represents a second order system with distinct poles. In the time domain, the load current has the general form of (4), where s_1 and s_2 are the poles of the characteristic polynomial and k_1 and k_2 are constants that have to satisfy the initial conditions (R_{p} is neglected for simplicity).

$$i_{\text{load}}(t) = k_1 e^{s_1 t} + k_2 e^{s_2 t} \qquad s_{1,2} = -\frac{L \pm \sqrt{L(L - 4C_{\text{out}}R_{\text{load}}^2)}}{2R_{\text{load}}C_{\text{out}}L} \tag{4}$$

As can be deduced from (4) an exponential change of the load current can be expected, during a step reference change. The rate of change depends on the poles of the characteristic polynomial. It can also be noted that the poles s_1 and s_2 are real, and the system is over-damped, when the condition $\frac{L}{C_{\text{out}}} > 4R_{\text{load}}^2$ is fulfilled. Based on the above dynamics, the maximum expected load current gradient that the topology can produce, can be calculated providing a benchmark for the topology's performance and the maximum frequency that can be tracked by a time-optimal controller. Fig. 2a) gives the resulting current gradient as a function of the inductance value L for the given set of design parameters. Similarly, Fig. 2b) gives the resulting current gradient as a function of the capacitance value C_{out}. The transients consider a step up/down, to/from 400A, which is considered the nominal current. It can be deduced that while the inductance L plays a significant role in the transient performance, the effect of the capacitance value C_{out} seems to be negligible, for the investigated capacitance range (1µF-50µF).

3 Overview of Benchmark Current Controllers

This section briefly discusses three conventional solutions, which form the basis for the hybrid controller that is introduced in the next section. These solutions are used in industrial applications for the control of the considered converter: i) the PI control and ii) the observer-based state feedback control and iii) the hysteretic control.

3.1 PI control

The PI controller offers precise reference tracking capability and insensitivity to parameter uncertainty along with inherent design simplicity. The detailed closed loop system with a PI controller and the considered loop delays are shown in Fig. 3. In current mode control, the average output voltage V_{c} is measured and fed-forward to the control system, so that the controller can be decoupled from the RC output network. The inevitable loop delays, however, and the feedback loop impose a maximum control bandwidth that limits the dynamic response of the system. As a result the maximum dynamic potential shown in section 2 cannot be exploited. An analysis of the control loop delays can be found in [19]. The tuning of the PI controller here is accomplished in the discrete

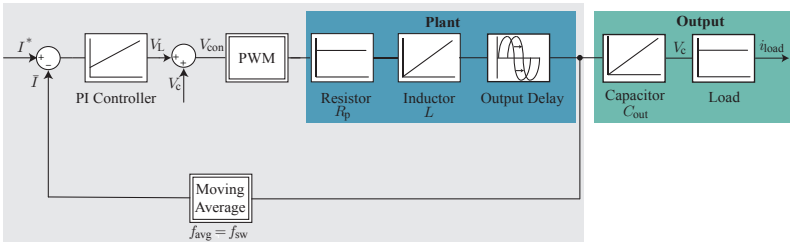

Figure 3: Closed loop of the current controlled system with a PI controller.

Table III: PI control parameters

Output delay	$0.1T_{\text{sw}}$
PWM delay	T_{sw}
Filter delay	$0.25T_{\text{sw}}$
K_{p}	1.65
K_{i}	2600
Bandwidth	7krad/s

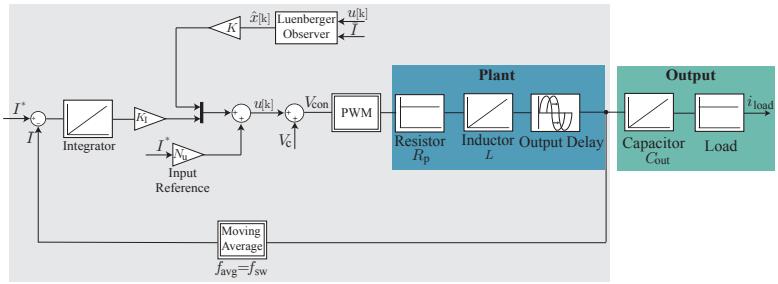

Figure 4: Closed loop controller with a state feedback controller, using a Luenberger state observer. In the schematic u[k] is the control input, $\hat{x}$[k] the three observed states (inductor current state and two additional states due to delays).

Table IV: State feedback control parameters

Output delay	$0.1T_{sw}$
PWM delay	T_{sw}
Filter delay	$0.25T_{sw}$
K	[-1.35, -4, 0.22]
K_I	27400
K_{obs}	[0.94, 0.93, 0]
Bandwidth	9.5krad/s

domain (z-domain), based on a linearized model, using optimization algorithms. The modeling considerations that are used for the derivation of the aforementioned linearized model, as well as the final control parameters for an optimized bandwidth of 7krad/s are shown in Table III.

3.2 Observer-based State Feedback Control

State space design allows the control designer to have an overview of the system and implement a control law that assigns the closed-loop poles to either pre-specified or optimized locations, in order to achieve a desired performance [7]. Using model information, the control designer is able to formulate robust controllers that achieve a better trade-off between performance and robustness. One of the advantages of state feedback control, is that it can be used when the full state is not available (e.g. due to delays) along with an observer which estimates the states based on the state space model and the measured data. The inclusion of the observer can lead to an increased bandwidth, compared to the PI controller [20].

The design of a state feedback controller in discrete time is described in [7] and the inclusion of the observer for a single input-single output system is discussed in [21]. The buck-type converter system, shown in Fig. 1, can be represented as a discrete state space model with one state (inductor current) since the output voltage is measured. The incorporation of the time delays shown in Table IV increases the order of the final state space system to three since the total delay is higher than one and smaller than two switching periods. Moreover, an integrator is augmented to increase the reference tracking capability of the controller (fourth state). Fig. 4 shows the closed loop system and Table IV the set of optimized control parameters based on the LQR design [8].

3.3 Hysteretic Control

The hysteretic control exhibits time-optimal transient response, unconditioned stability for a wide operational range due to its bounded nature and excellent large signal properties [13]. These characteristics make it suitable for applications with highly demanding dynamic requirements, since it can exploit the maximum current gradient capabilities of the topology. Fig. 5a, shows the operation of the hysteretic controller. The hysteretic band, for the studied topology, can be calculated as given in (5), for a triangular current ($i_{L,ideal}$), in order to achieve a target

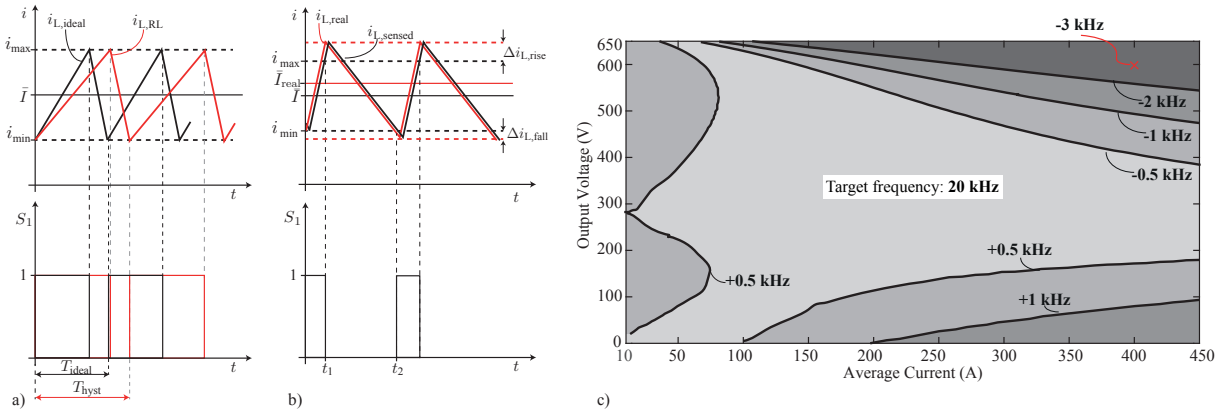

Figure 5: a) Ideal operation of a hysteretic controller (black curve) and the effect of the parasitic resistance R_p (red curve), resulting in a switching frequency error. b) DC static error of a hysteretic controller due to the effect of delays [14]. c) Switching frequency error of the hysteretic controller due to the effect of R_p=25mΩ, shown in a) including the effect of the output voltage ripple. Both higher and lower switching frequencies compared to the specified 20kHz result for the converter with the parameters of Table I. At 400A and 600V the error is -3kHz (i.e. -15% deviation).

switching frequency f_s.

$$H = \frac{1}{2}\frac{D(1-D)(V_1+V_2)}{Lf_s} \qquad i_{max} = \bar{I}+H \qquad i_{min} = \bar{I}-H \tag{5}$$

However, in certain applications (e.g. pulsed power) the semiconductor devices are often under-dimensioned with respect to their current rating (increased semiconductor switch resistance R_{on}) as they only have to operate for a limited time duration. Additionally, electrolytic capacitors with significant ESR may be used at the input of the converter, as energy storage units. As a result, the parasitic series resistance R_p can be high and its effect cannot be neglected, since it causes the current waveform to rise/fall exponentially ($i_{L,RL}$), with a time constant $\frac{L}{R_p}$.

$$i_{L,ideal}(t) = \left(\frac{V_{in}-V_c}{L}\right)t + i_{min} \qquad i_{L,RL}(t) = \frac{V_{in}-V_c}{R_p}\left(1-e^{-t\frac{R_p}{L}}\right) + i_{min}e^{-t\frac{R_p}{L}} \tag{6}$$

Furthermore, the digital implementation of the hysteretic control and the effects of various delays related to it (measurement delays, ADC delays, interlocking time, etc.) were discussed thoroughly in [14]. A possible scenario for such delays is depicted in Fig. 5b where $\Delta i_{L,rise}$ is larger than $\Delta i_{L,fall}$ and as a result a DC static error is observed with higher current than expected ($\bar{I} < \bar{I}_{real}$). Suitable adaptations are proposed in [14] and [22] in order to deal with switching frequency jittering and DC regulation inaccuracy.

Fig. 5c, shows the frequency error, as a function of the average current and the output voltage, due to R_p and the voltage ripple during the switching period. It can be noticed that the switching frequency becomes significantly lower than the target frequency of 20kHz in the high-current/high-voltage region. This effect would be enhanced if the study included the effects of finite sampling and execution times, as demonstrated in section 5 via time-domain simulations.

4 Proposed Hybrid Control Concept

In the previous section, benchmark controllers that are often employed for DC-DC converters were presented. The hysteretic control offers time-optimality in transients but suffers from inaccuracy both in reference current tracking and in switching frequency. On the contrary, the PI controller and the state feedback controller offer superior performance in steady state but limited dynamic potential. Obviously these control methods are complementary and combining them would result in a near-optimum control action, with a relatively small implementation effort. Therefore, in this section the hybrid control concept is presented and its performance under step reference changes and rapid load changes is discussed. There the focus is on minimizing the disturbance introduced by the switching between the two control schemes, as well as the early detection of load disturbances.

An overview of the proposed hybrid controller schematic is shown in Fig. 6a, where a PI controller is combined with an adaptive hysteretic controller and a supervisor. It must be noted that the PI controller could also be substituted by other average current control methods (e.g. state feedback control, etc.). Fig. 6b shows a flowchart of the hybrid controller's algorithm with the mode-shifting conditions from average mode to hysteretic mode:

i. Fast transient/step reference is detected: $|I^*[k]-I^*[k-1]| \geq \Delta I^*$

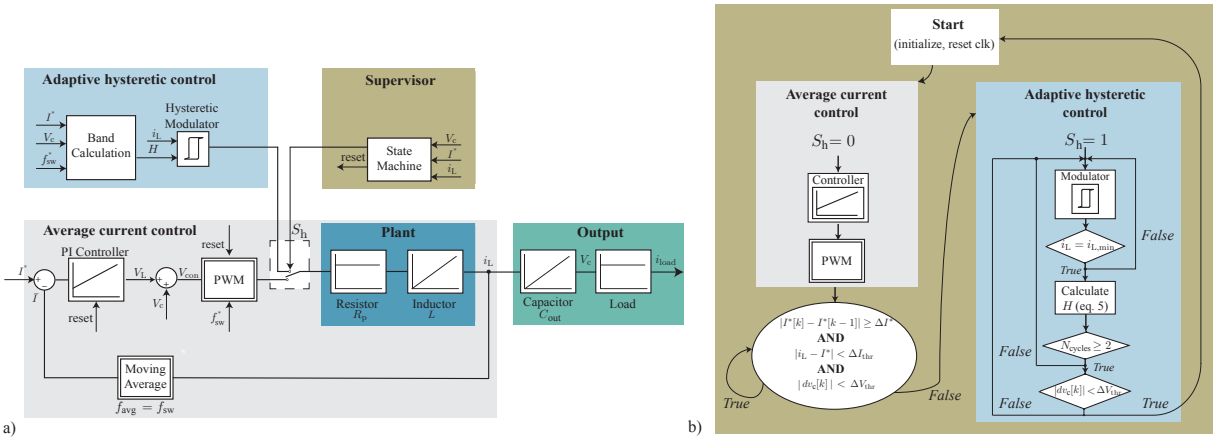

Figure 6: Proposed hybrid control scheme consisting of an average current controller (PI controller) in order to achieve constant switching frequency and accuracy in steady state and an adaptive hysteretic controller with time-optimal dynamic performance. The supervisor's state machine determines which controller is enabled. b) Flowchart diagram of the proposed hybrid controller. The conditions that need to be fulfilled in order to switch to/from the average current mode control are noted.

ii. The instantaneous current i_L surpasses a threshold value ΔI_{thr}: $|i_L - I^*| \geq \Delta I_{thr}$

iii. The weighted voltage derivative dv_c surpasses a threshold value ΔV_{thr}: $|dv_c| \geq \Delta V_{thr}$.

The fine tuning of these conditions is discussed in section 4.3. To switch back to average current control mode with minimum disturbance, three conditions must be fulfilled:

a. The inductor current should be at its minimum ($i_L = i_{L,min} = \bar{I} - H$). This condition ensures that at the mode shifting instance, the sawtooth PWM counter can be reset and a new switching cycle can start. In this way, the control input of the average current mode is immediately applied, turning on S_1 and increasing i_L.

b. The number of hysteretic cycles should be greater than 2 ($N_{cycles} \geq 2$). This condition ensures that at least one adaptation of the hysteretic band is performed before the mode-shifting occurs, so that the current ripple at the end of the hysteretic mode is close to its steady state value.

c. The output voltage should be approximately settled ($|dv_c| < \Delta V_{thr}$). This condition ensures that the system is approximately at steady state. The control output of the average mode is almost at its steady state value and only small adaptations are needed from the average mode controller.

4.1 Step Reference Change

Fig. 7a) depicts the ideal behavior of the hybrid controller under a step reference change ($0 \rightarrow I^*$). **During $t < t_0$**, the system is in steady state and the reference current is set to zero ($I^* = 0$). The average mode control is enabled as the output signal of the supervisor is $S_h = 0$. **At $t = t_0$**, the current reference is changed and mode-shifting condition i) is met. The supervisor recognizes the transient and changes the state of its output signal S_h from 0 to 1, enabling the hysteretic controller. The hysteretic band calculation block sets H to an initial value H_0 and since the instantaneous current is lower than $i_{min,0}$, the hysteretic modulator turns on switch S_1 causing the inductor current to rise until it reaches the pre-set value $i_{max,0}$, at $t = t_1$.

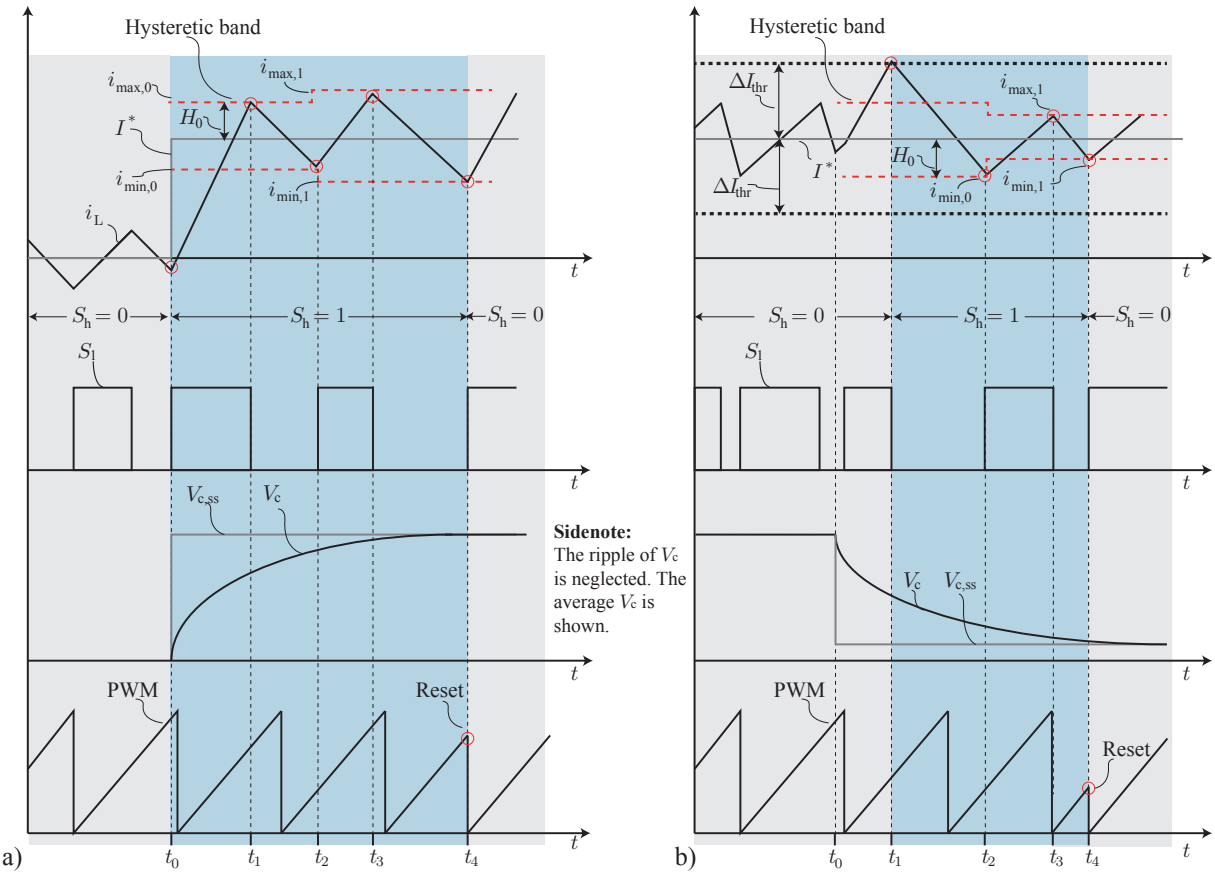

Figure 7: a) Operation principle of the hybrid controller for a current reference step up. b) Operation principle of the hybrid controller for a load transient with a violation of the current threshold. Both graphs depict idealized scenarios, neglecting the effects of non-idealities.

At $t = t_1$, the instantaneous current reaches $i_{\max,0}$ and the hysteretic modulator turns off switch S_2 causing the current to fall. No change in the hysteretic band is imposed at this stage so that the average current is equal to the reference current I^* (symmetrically placed $i_{\max,0}$ and $i_{\min,0}$ around I^*) .

At $t = t_2$, the inductor current reaches $i_{\min,0}$ and S_1 is turned on. Since the operating point of the converter has changed, the ripple current for a given switching frequency f_s has changed and the hysteretic band calculation block sends the new value of H to the modulator based on the sampled output voltage V_c and (5). The new limits $i_{\max,1}$ and $i_{\min,1}$ are calculated. The supervising controller keeps $S_h = 1$ as the minimum number of hysteretic cycles has not been reached ($N_{\text{cycles}} < 2$).

At $t = t_4$, i_L reaches $i_{\min,1}$. At this point, the converter is at steady state since the output voltage V_c has settled to its steady state value $V_{c,ss}$. In addition, the switching period of the converter is approximately equal to the desired one so that the mode-shifting conditions are fulfilled. The supervisor sets $S_h = 0$, switching back to average current control mode. Moreover, the supervisor sends a reset signal to the PWM counter and the integrator of the controller and a new switching period begins. Since t_4 is the start of the new switching period, switch S_1 is turned on (sawtooth PWM) and the current is increasing, minimizing the disturbance due to the mode shifting action.

4.2 Load Transient

Fig. 7b) depicts the operation of the controller during a rapid load change that causes the output voltage to drop and leads to the violation of the current threshold condition ii). **During $t < t_0$**, the system is at steady state and the average current control mode is active ($S_h = 0$). **At $t = t_0$**, the load changes rapidly and the output voltage decreases. **During $t_0 < t < t_1$**, the load change is not detected by the control system because the supervisor has not detected any violation of the conditions shown in Fig. 6b, so it keeps its output signal $S_h = 0$ and the duty cycle is not renewed leading to a rise of the instantaneous inductor current. This scenario assumes that the weighted voltage derivative criterion (condition iii) is not violated.

At $t = t_1$, the instantaneous current reaches its threshold $I^* + \Delta I_{\text{thr}}$, and the maximum current condition (Fig. 6b) is violated, so the supervisor sets its output signal $S_h = 1$, activating the adaptive hysteretic control. The hysteretic modulator switches off switch S_1 and i_L decreases. The hysteretic band calculation block initializes the value of the band H_0 and sets the limit $i_{\min,0}$.

At $t = t_2$, the inductor current reaches $i_{\min,0}$ and according to the algorithm, the hysteretic band value is renewed, based on the sampled output voltage V_c and (5). The condition for $N_{\text{cycles}} \geq 2$ is not fulfilled yet, so the supervisor keeps $S_h = 1$ and renews the hysteretic limits of the modulator setting them to $i_{\max,1}$ and $i_{\min,1}$.

At $t = t_4$, the inductor current reaches $i_{\min,1}$ and the listed mode shifting conditions a)-c) are fulfilled. The supervisor sets its output signal to $S_h = 0$ and sends a reset signal to the PWM clock and the integral part of the controller, switching back to average current control mode with a minimum disturbance.

4.3 Controller Design Considerations

This section discusses the tuning of the mode-shifting conditions (i-iii) for the studied converter system. The fine tuning of these conditions depends on the parameters and the control requirements but general guidelines that could be adjusted for different systems are given in the following.

As shown in Fig. 2, the maximum gradient that the topology can produce ranges from approximately $0.5\text{A}/\mu\text{s}$ to $3\text{A}/\mu\text{s}$ for the considered resistive load range. For transients faster than $0.5\text{A}/\mu\text{s}$, the hysteretic mode is enabled. Considering that the reference is read by the controller with 1MHz frequency, ΔI^* is set to 0.5. The first mode-shifting condition is therefore violated if $|I^*[k] - I^*[k-1]| \geq 0.5\text{A}$.

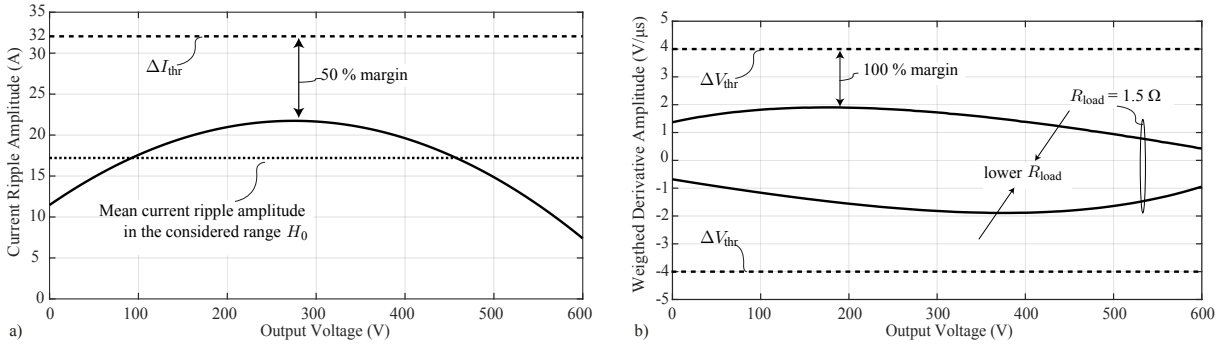

Figure 8: a) Current ripple amplitude in the operating range, based on (1). The current threshold value ΔI_{thr} is set to allow 50% margin from the maximum. The mean current ripple amplitude is used to initialize the hysteretic band H_0. b) Maximum expected output voltage weighted derivative calculated as in (7). The derivative depend on the load resistance and only the values for the maximum R_{load} are shown. The threshold value ΔV_{thr} is set to allow 100% margin from the maximum.

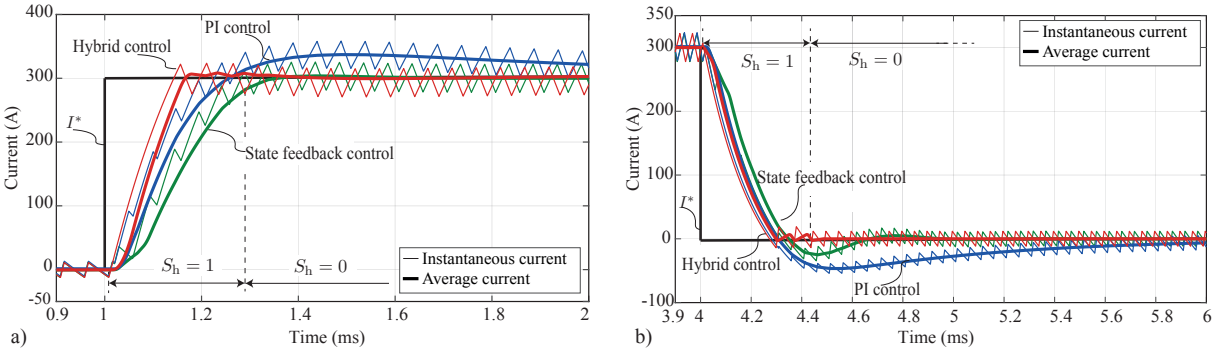

Figure 9: a) Inductor current waveforms for a 300A step up response for a 1Ω load resistance. The hybrid controller results in a current gradient of approximately 2A/µs, as calculated in Fig. 2, b) Inductor current waveforms for a 300A step down response for a 1Ω load resistance. The hybrid controller results in a current gradient of approximately 1.5A/µs, as calculated in Fig. 2.

Moreover, the maximum inductor current ripple can be calculated from (1) and is depicted for the studied converter in Fig. 8a). The threshold value for the current can then be set allowing a 50% margin. The second mode-shifting condition is therefore violated if $|i_L - I^*| \geq 32$A. For the initialization of the hysteretic band, used in the first hysteretic cycle, the mean inductor current amplitude value is used, shown in Fig. 8a) too.

Additionally, the third mode shifting condition monitors the weighted voltage derivative dv_c extracted from the sampled output voltage as in (7). The voltage derivative can be sensitive to noise and therefore its previous value is used to act as a low pass filter.

$$dv_c[k] = 0.5dv_c[k-1] + 0.5(V_c[k] - V_c[k-1]) \tag{7}$$

The expected maximum dv_c can be calculated numerically by solving the set of differential equations (2) and the result is shown in Fig. 8b for the maximum considered R_{load}, since the voltage derivative value scales with the load. A margin of 100% is allowed in the present design and condition iii) is violated when $|dv_c| \geq 4$V/µs. Mode shifting conditions ii) and iii) are important for detecting rapid load changes fast and can ensure the safe operation of the system when fluctuating loads are driven (e.g. DC-arcs). Especially in systems with a low C_{out} (e.g. current sources), the weighted derivative criterion can be particularly beneficial.

5 Simulation Results

This section compares the performance of the previously discussed controllers for the buck-type converter system shown in Fig. 1, with the set of parameters shown in Table I. Fig. 9a depicts the step up response of the current for a 1Ω load resistance. The PI controller has a faster rise time compared to the state feedback controller but presents a relatively high overshoot. On the other hand, the state feedback control scheme accounts for the time delays due to its state-observer, and minimizes the current overshoot resulting in a faster settling time. Moreover, the superiority of the hybrid controller can be seen. The adaptive hysteretic controller takes over during the transient (S_h=1) and exhibits a time-optimal response. The proposed supervisor algorithm adjusts the hysteretic band and returns to average current control mode without disturbing the current waveform, when the mode shifting conditions are fulfilled, in this case after three hysteretic periods. A slight DC static error results after the hysteretic action due to the non-idealities inserted in the simulations (e.g. sensor delays, finite sampling and execution times). This static

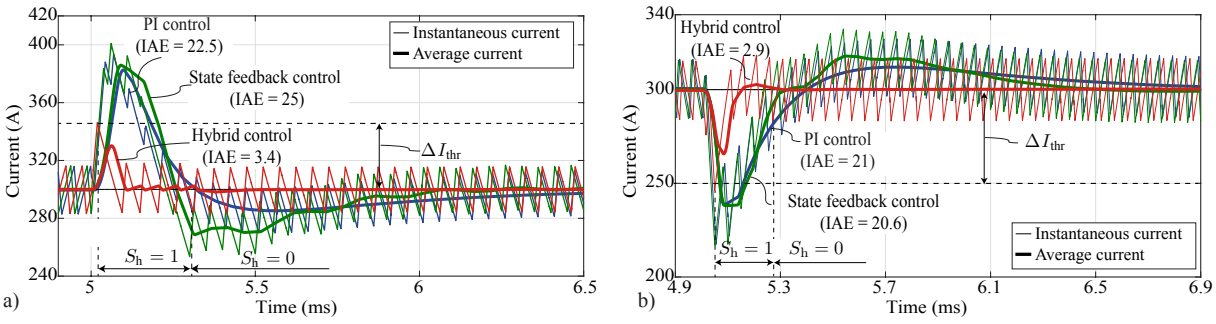

Figure 10: a) Inductor current waveforms for a step load change, at $t = 5$ ms, from 1.5Ω to 0.1Ω. b) Inductor current waveform for a step load change at t=5ms, from 0.1Ω to 1.5Ω. In both cases the ΔI_{thr} for the activation of the hysteretic controller is set to be ±10% of the reference current. The Integral of Absolute Error (IAE) index of each controller is noted on the graphs, calculated as: $\int_{t_0}^{\infty} |e(t)|dt$, where $e(t) = \bar{I}(t) - I^*$ and $t_0 = 5$ ms in the simulated case.

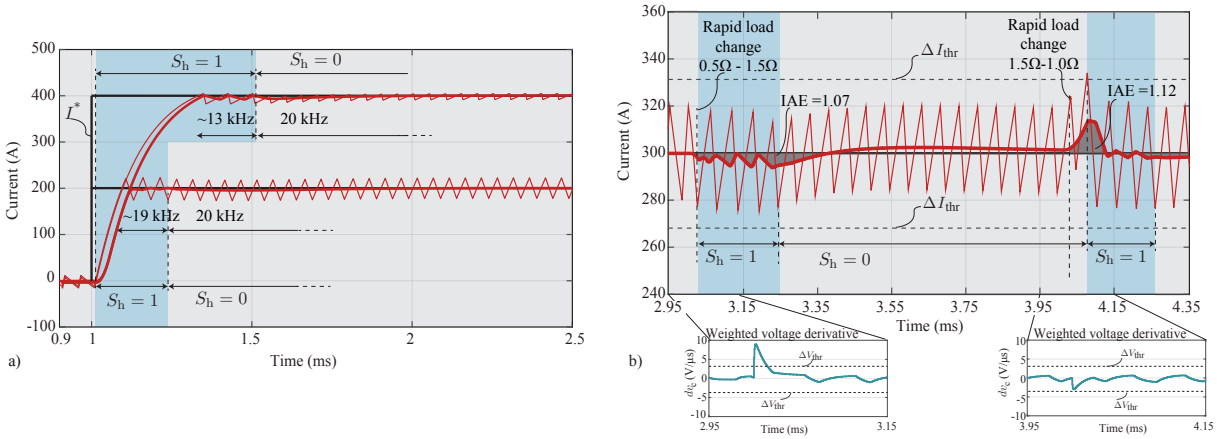

Figure 11: a) Performance of the hybrid controller under 1.5Ω load, for a reference current of 200A and 400A. In the 400A case the hysteretic mode results in a notable switching frequency mismatch that causes a disturbance after the mode-shifting. This effect was highlighted in Fig. 5 and is enhanced due to the considered delays. b) Performance of the hybrid controller under two successive load fluctuations. The first violates the voltage derivative threshold condition while the second violates the current threshold condition.

error converges to zero after the transient due to the integral action. The resulting current gradient of the hybrid controller is approximately $2\mathrm{A}/\mu\mathrm{s}$.

Fig. 9b depicts the step down response of the current. The response time of the PI controller is similar to the hybrid controller but its resulting overshoot is relatively high. Furthermore, the hybrid controller exhibits a time-optimal step response and a negligible disturbance when returning to normal operation. In this case, no static error is noted. However, during the hysteretic period, a switching frequency mismatch can be observed due to the discussed non-idealities. This frequency mismatch becomes obvious in the average current waveform where slight oscillations are observed when S_h=1. As expected the current gradient is approximately $1.5\mathrm{A}/\mu\mathrm{s}$.

Fig. 10a and Fig. 10b depict the performance of the compared controllers under an abrupt change in the load from 1.5Ω to 0.1Ω and vice-versa, respectively. In both figures, the PI controller as well as the state feedback controller exhibit similar large signal disturbance rejection capabilities, with similar recovery times, maximum current deviation and IAE indexes. However, the superiority of the hybrid controller is clearly visible. The supervisor block switches to hysteretic mode (S_h=1) as soon as the instantaneous current exceeds a threshold value ΔI_{thr}, and thus makes use of the excellent large signal properties of the hysteretic controller. Once again slight frequency mismatches and DC static errors converge to zero once the supervisor switches the control system back to average current mode (S_h=0) after 3 hysteretic periods.

Fig. 11a shows the performance of the hybrid controller under a resistive load of 1.5Ω and two different reference currents, in detail. Particularly for the 400A reference current, the hysteretic controller causes a static error due to the non-idealities of the control loop. It can be seen that the switching frequency in this case is approximately 13kHz, resulting in a higher current ripple and a notable disturbance in the mode-shifting action from hysteretic to average mode. The switching frequency mismatch could be reduced by employing the improvements of [14]. However this would increase the complexity of the algorithm and require the hybrid controller to stay longer in hysteretic mode. In the simulated case, the hybrid controller switches back to average current mode and tracks the reference current with high precision, after two hysteretic periods. With the 200A reference current, the static error and the switching frequency mismatch are comparably small. This effect was shown in Fig. 5.

Finally, Fig. 11b shows the performance of the hybrid controller under two successive rapid load changes and highlights the importance of the voltage derivative criterion in systems with low output capacitance C_{out}. The first load change occurs at t=3ms and violates immediately the voltage derivative threshold ΔV_{thr} as can be noticed in the zoomed picture. The hysteretic mode is then enabled fast and a small switching frequency mismatch is noted along with a small DC error, due to the inaccuracies of the hysteretic controller. The current disturbance is however small (IAE = 1.07). The second load change occurs at t=4ms and does not violate the voltage derivative threshold. The controller remains in average mode until the current reaches ΔI_{thr}, when the hysteretic mode is enabled. It can be noted that when the transient violates the voltage criterion the controller acts faster since the voltage derivative takes its maximum value just after the occurrence of the transient and therefore the IAE index is slightly lower despite the fact that the load disturbance in the second load change is smaller.

6 Conclusion

In this paper, a new hybrid controller that combines the hysteretic controller in transients and the average current control mode in steady state is proposed and its performance is compared with a PI controller and a state feedback controller. The comparative study reveals the superiority of the proposed control scheme as well as its ability to fully exploit the dynamic potential of the topology by generating a higher current gradient. A notable improvement in the disturbance rejection capability of the system was noted (approx. 80% reduction of the IAE index compared to the benchmark solutions). Furthermore, the simulated non-idealities of the control loop revealed the differences compared to the theoretical ideal operation of the proposed method. All in all, the proposed controller is suitable for applications with strict requirements regarding the dynamic performance of the system (e.g. highly dynamic current sources), without excessively increasing the implementation effort since it relies on the implementation of two widely known and simple control methods.

References

[1] C. Carstensen and J. Biela, "10kV/30kA unipolar arbitrary voltage source for hardware-in-the-loop simulation systems for HVDC circuit breakers," in *Proc. of the 14th European Conf. on Power Electronics and Applications (EPE)*, 2011.

[2] C. Carstensen and J. Biela, "A novel ultra precise solid state pulsed current source for kicker magnets," *Proc. of the 4th Euro-Asian Pulsed Power Conf. (EAPPC)*, 2012.

[3] C. M. Franck, "HVDC circuit breakers: A review identifying future research needs," *IEEE Trans. on Power Delivery*, 2011.

[4] F. Schmitt, "The Gradient System," in *Proc. Society of Magnetic Resonance*, 2013.

[5] C. Carstensen and J. Biela, "A three-level buck converter with a wide voltage operation range for hardware-in-the-loop test systems," *IEEE Trans. on Power Electronics*, 2016.

[6] K. J. Astrom and T. Hagglund, "PID Controllers: Theory, Design, and Tuning," *NC: Instrument Society of America*, vol. 2nd, 1995.

[7] F. H. Dupont, V. F. Montagner, J. R. Pinheiro, H. Pinheiro, S. V. G. Oliveira, and A. Peres, "Comparison of linear quadratic controllers with stability analysis for DC-DC boost converters under large load range," *Asian Journal of Control*, vol. 15, no. 3.

[8] V. F. Montagner and S. P. Ribas, "State feedback control for tracking sinusoidal references with rejection of disturbances applied to UPS systems," in *35th Annual Conf. of Industrial Electronics, IECON*, 2009.

[9] J. Han, "From PID to active disturbance rejection control," *IEEE Trans. on Industrial Electronics*, vol. 56, no. 3, 2009.

[10] H. Kwakernaak, "Robust control and H-∞ optimization tutorial paper," *Automatica*, vol. 29, no. 2.

[11] C. J. Solis and G. A. Rincon-Mora, "Stability analysis and design of hysteretic current-mode switched-inductor buck DC-DC converters," in *20th Int. Conf. on Electronics, Circuits, and Systems (ICECS)*, 2013.

[12] J. Abu-Qahouq, H. Mao, and I. Batarseh, "Multiphase voltage-mode hysteretic controlled DC-DC converter with novel current sharing," *IEEE Trans. on Power Electronics*, vol. 19, no. 6, 2004.

[13] C. Song and J. L. Nilles, "Accuracy analysis of hysteretic current-mode voltage regulator," in *20th IEEE Applied Power Electronics Conf., APEC*, vol. 1, 2005.

[14] W. Stefanutti and P. Mattavelli, "Fully digital hysteresis modulation with switching-time prediction," *IEEE Trans. on Industry Applications*, vol. 42, no. 3, 2006.

[15] A. Babazadeh and D. Maksimovic, "Hybrid digital adaptive control for fast transient response in synchronous buck DC-DC converters," *IEEE Trans. on Power Electronics*, vol. 24, no. 11, 2009.

[16] S. C. Tan, Y. M. Lai, and C. K. Tse, "General design issues of sliding-mode controllers in DC-DC converters," *IEEE Trans. on Industrial Electronics*, vol. 55, no. 3, 2008.

[17] L. Corradini, A. Costabeber, P. Mattavelli, and S. Saggini, "Time optimal, parameters-insensitive digital controller for VRM applications with adaptive voltage positioning," in *11th Workshop on Control and Modeling for Power Electronics*, 2008.

[18] T. Geyer, G. Papafotiou, R. Frasca, and M. Morari, "Constrained optimal control of the step-down DC-DC converter," *IEEE Trans. on Power Electronics*, vol. 23, no. 5, 2008.

[19] T.Nussbaumer, M.L.Heldwein, G.Gong, S.D.Round, and J.W.Kolar, "Comparison of prediction techniques to compensate time delays caused by digital control of a three-phase buck-type PWM rectifier system," *IEEE Trans. on Industrial Electronics*, vol. 55, no. 2, 2008.

[20] C. Olalla, R. Leyva, A. E. Aroudi, and I. Queinnec, "Robust LQR control for PWM converters: An LMI approach," *IEEE Trans. on Industrial Electronics*, vol. 56, no. 7, 2009.

[21] G. F. Franklin, J. D. Powell, and A. Emami-Naeini, "Feedback control of dynamic systems," *Pearson International Edition*.

[22] G. H. Bode and D. G. Holmes, "Improved current regulation for voltage source inverters using zero crossings of the compensated current errors," in *36th IAS Annual IEEE Industry Appl.Conf.*, vol. 2, 2001.