Hybrid Circuit Breaker for HVDC Grids with Controllable Pulse Current Shape

Conference Paper

Author(s):
Jehle, Andreas; Biela, Jürgen

Publication date:
2017

Permanent link:
https://doi.org/10.3929/ethz-b-000250189

Originally published in:
CFP17850, https://doi.org/10.23919/EPE17ECCEEurope.2017.8099262

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Laboratory for High
Power Electronic Systems

Hybrid Circuit Breaker for HVDC Grids with Controllable Pulse Current Shape

Jehle A., Biela J.
Power Electronic Systems Laboratory, ETH Zürich
Physikstrasse 3, 8092 Zürich, Switzerland

Hybrid Circuit Breaker for HVDC Grids with Controllable Pulse Current Shape

Andreas Jehle and Jürgen Biela
Laboratory for High Power Electronic Systems, ETH Zürich
Email:jehle@hpe.ee.ethz.ch, URL:http://www.hpe.ee.ethz.ch

Keywords

≪HVDC≫, ≪Multiterminal HVDC≫

Abstract

In this paper, two new hCB concepts for DC-grids are presented, which use a pulse current to extinguish the arc in the mechanical switch after opening. Both concepts are capable to adjust the pulse current amplitude/waveform to the fault current amplitude and so generate a slow current slope $^{di}/_{dt}$ directly before the zero current crossing without large passive components for a fast and reliable fault clearing. By improving the controllability of the hCB and with a new control concept the capacitor volume of the first concept could be reduced by 60% and the inductor volume by 88% compared to the existing solution. At the cost of more active components, the capacitor volume could be even more reduced by 98.4% compared to the first concept (99.4% compared to the existing solution).

1 Introduction

In recent years, the interest in bulk HVDC transmission has significantly increased. A reason is the increased need for offshore energy transmission from windfarms, which is limited to short distances with AC technology due to cable capacitances. Also the need to transport energy of wind or solar parks over long distances increases the interest in HVDC-transmission, which has lower losses than AC transmission. With the increasing power ratings of semiconductors using voltage source converters (VSC) in HVDC systems is significantly simplified. Such converters enable a power reversal in a transmission line without a voltage reversal, being a first step to a meshed multi-terminal DC grid with low transmission losses [1].

One of the major remaining problems of HVDC transmission is to turn lines on and off, especially in case of a fault, where currents rise quickly to high values, because of the low inductances and the high capacitances encountered in HVDC systems. Besides turning off the complete DC grid [2] or using AC circuit breaker with resonant circuits, hybrid circuit breakers (hCB) are a very interesting alternative. hCBs combine a mechanical switch (MS) of slowly opening pure mechanical circuit breakers for minimizing the conduction losses with a power electronic circuit, for enabling a fast turn off/fault interruption [3, 4].

In HVDC systems, hCBs have to fulfill three basic requirements [1]:

1. To generate a zero current crossing in the MS for interrupting the arc
2. To dissipate the stored energy in the connected lines
3. To withstand the system voltage

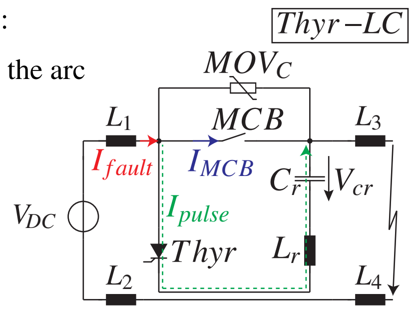

Figure 1: An unidirectional hCB with MCB and an LC circuit with a thyristor to generate a single pulse current in the MCB (Thyr-LC) [5] for turning the hCB off.

For generating a zero current crossing in the MS several possibilities exist [6, 7]. For example, some topologies use a load commutating switch (LCS) (typical semiconductors), which commutates the current to a parallel breaker branch consisting only of semiconductors [8, 9] or capacitors [10]. Topologies with LCS have the main advantage that the current commutates fast from the MS to the semiconductor branch. Therefore, the MS can open without arc, so that these topologies can use ultra fast disconnectors as MS and are able to block an increasing voltage while opening the MS[11] resulting in a faster interruption process. However, the LCS generates additional conduction losses in the on-state.

Topologies with a mechanical circuit breaker (MCB) as MS, which open under current with an arc, can operate without LCS and cause therefore no additional on-state losses. The arc in the MCB is extinguished by generating a zero current crossing in the MCB after the MCB is completely open. The zero current crossing can be achieved by superimposing a resonant current higher than the fault current [12] or by injecting a pulse current in opposite direction to the fault current [5, 13]. A successful arc extinction in the MS without reignition depends on several parameters as for example the gap distance at zero current crossing [14], the arc duration [15], the $\mathrm{d}v/\mathrm{d}t$ across the MCB shortly after the arc extinction and the $\mathrm{d}i/\mathrm{d}t$ of the current in the MCB shortly before the arc extinction [16–18]. While a large and quickly increasing gap distance and a short arcing time can be achieved by quickly opening the MCB, the $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ depend on the grid and the design of the hCB. However, the known hCB concepts allow no significant control of the pulse current and a low $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$ for all possible fault currents can be achieved only by large passive components. Depending on the used MCB, $\mathrm{d}i/\mathrm{d}t$ values between $100A/\mu s$ [17] and $20A/\mu s$ [15] are required for a successful arc extinction.

In order to overcome these limitations, two new unidirectional hCB topologies with the ability to adapt the shape and amplitude of the pulse current, the $\mathrm{d}i/\mathrm{d}t$ and the $\mathrm{d}v/\mathrm{d}t$ are presented in this paper. The unidirectional hCBs conduct currents in both directions, but are only able to interrupt currents in one direction, which decreases the required components and is sufficient for applications in grids [6]. Both topologies are derived from the basic concept shown in Fig. 1 [5], whose design, basic principle and limits are briefly explained in **section 2**. The two new topologies, which allow a much better control of the $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$ are then presented in **section 3.1** and **section 3.2**. Both presented topologies use semiconductor switches, which can be turned on and off, to adapt the pulse current and so reduce the probability of an hCB failure. Moreover, the proposed topologies can also be used to increase the performance in terms of a lower maximum fault current, as is shown in **section 3.4**. The proposed topologies are compared with existing solutions in detail in **section 4** in terms of passive components, number of semiconductors and performance. In **section 5** the main results are summarized.

2 Single pulse hCB with LC-circuit and thyristor

A relatively simple and robust concept to turn off an increasing fault current in a DC line is shown in Fig. 1 [5]. To minimize the on state losses, only a MCB is used in the main current path. A pulse current generator, consisting of capacitor C_r, inductor L_r and thyristor $Thyr$, is in parallel to the MCB (Fig. 1). Before the turn off, the capacitor C_r must be precharged. In case of a fault, the current I_{fault} through the MCB quickly increases. After detecting the fault, the MCB is opened under current resulting in an arc. While opening, the fault current increases further. After the MCB is completely open, thyristor $Thyr$ is triggered to generate a pulse current through the MCB in opposite direction to the fault current. The arc is then extinguished at the zero current crossing caused by the pulse current. After the arc extinction, the current commutates to the C_rL_r-path and charges capacitor C_r until the voltage over the varistor MOV_C has increased so much that the fault current commutates completely to the varistor. This voltage must be higher than the system voltage V_{nom} to decrease the fault current and is called transient interruption voltage (TIV). The energy in the cable inductances $L_1 - L_4$ is then dissipated by varistor MOV_C.

One advantage of this hCB is its simple topology and control. In addition, there are no additional conduction losses during normal operation since there is no LCS. However, there are several disadvantages as will be explained with the help of Fig.2:

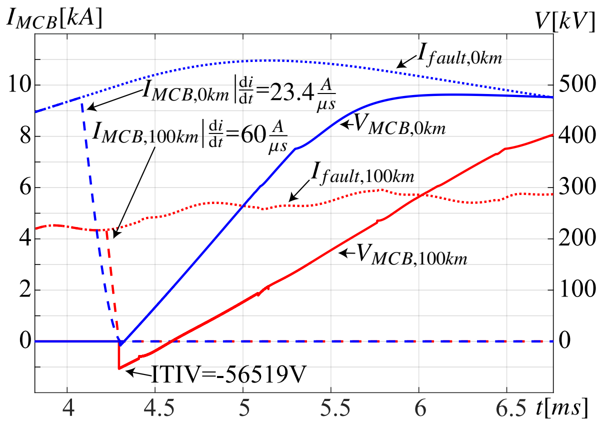

Figure 2: Two fault current turn off simulations for the hCB given in Fig.1 for a short circuit fault at t=0ms. The assumed detection time is 2ms and the MCB opening time is 2.3ms. The simulations reveal for two different distances the three disadvantages of this concept: 1) The $\mathrm{d}i/\mathrm{d}t$ at the zero current crossing is higher for low fault currents than for higher fault currents. 2) The $\mathrm{d}v/\mathrm{d}t$ across the MCB is lower for small currents resulting in a slower fault clearing. 3) The high negative initial transient interruption voltage (ITIV) after the zero current crossing generated across the MCB.

- The first disadvantage is that the shape of the pulse current is determined mainly by the capacitance value of C_r, by the precharge voltage and by the inductance value of L_r and therefore stays the same for all possible fault currents. However, the fault current amplitude and slope depend on the initial current, fault type and the fault location. Consequently, the maximum pulse current must be

 ISBN: 9789075815269 and CFP17850-USB

designed such that it exceeds the maximum possible occurring fault current $I_{MCB,0km}$. This means, that for a fast switching action, the pulse current must rise quickly to very high values. However, the arc extinction requires also for low fault currents a low $^{di}/_{dt}$ shortly before the extinction, to reduce the possibility of a reignition [18]. Therefore, the design of the pulse circuit is a trade-off between the rise time to the maximum current $I_{MCB,0km}$ and the $^{di}/_{dt}$ of the lowest fault current $I_{MCB,100km}$ and/or of the nominal current during normal turn off, resulting in a high capacitance value of C_r and a high inductance value of L_r.

- A second disadvantage is that the $^{dv}/_{dt}$ of the TIV V_{MCB} across the MCB depends on the capacitance value of C_r, which is charged by the fault current I_{fault}. The maximum allowed $^{dv}/_{dt}$ across the MCB after the arc extinction must not be exceeded in order to prohibit a reignition. Therefore, the capacitance value of C_r must be designed for the fast increasing $V_{MCB,0km}$ of the maximum fault current. However, by designing the capacitance value of C_r for the highest fault current, the voltage $V_{MCB,100km}$ after the arc extinction rises only slowly for a low fault current $I_{MCB,100km}$, resulting in a longer time until the fault current decreases and therefore also in a higher fault current and a longer turn off time.

- A third disadvantage is the series connection of L_r and $L_1 - L_4$ after the arc extinction. Before the arc is extinguished, the complete source voltage is shared by the line inductances $L_1 - L_4$. After the arc extinction, inductor L_r must have the same $^{di}/_{dt}$ as the line inductances. This results in an initial transient interruption voltage (ITIV) across the MCB directly after the arc extinction, and could lead to a reignition. Therefore, the inductance value of L_r in the pulse current circuit should be low, which contradicts the need for a low $^{di}/_{dt}$.

To avoid these three disadvantages, two new circuits which allow to adapt the pulse current for decreasing the current slope at the zero current crossing are presented in the next section.

3 Hybrid DC circuit breaker with adaptable pulse current and partially controllable MCB voltage

3.1 Single pulse hCB with adaptable pulse current

An extended hCB with partially adaptable pulse current shape without using a high number of passive components is shown in Fig. 3. Instead of thyristors, IGBTs in series are used in this circuit. In parallel to each IGBT and to the $R_rC_rL_r$ circuit are varistors $MOV1 - MOVn, MOV_C$. Again, capacitor C_r has to be precharged by a charging circuit (see section 3.3).

In case of a fault, the hCB is turned off in five steps as shown in Fig. 4:

- Fig. 4-1: First the fault current through the MCB increases until the fault is detected and the MCB is opened resulting in an arc.

- Fig. 4-2: Shortly before the MCB is completely open, a pulse current is triggered by turning the IGBTs on. The ideal timing is that the current in the MCB becomes zero when the MCB just has reached its maximum contact distance/ is fully open.

- Fig. 4-3: After the arc is extincted, diode D_A starts to conduct until the pulse current becomes lower than the fault current.

- Fig. 4-4: After diode D_A blocks, the current in the MCB branch remains zero and the fault current continues to charge capacitor C_r while the MCB regains its full blocking capability.

- Fig. 4-5: As soon as the capacitor voltage is high enough to commutate the fault current to MOV_C, the energy of the lines is dissipated in MOV_C and varistors $MOV_1 - MOV_n$.

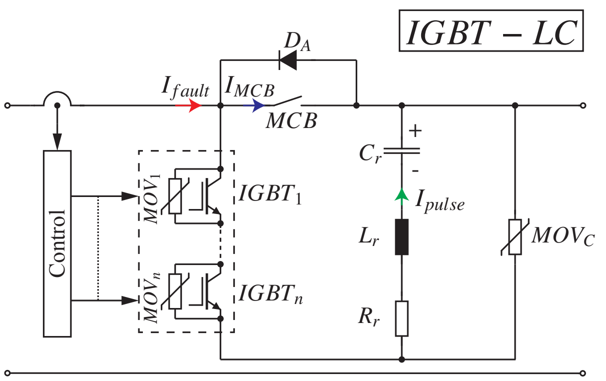

Figure 3: hCB with MCB and an LC circuit with IGBTs (IGBT-LC). By using IGBTs for generating the pulse current, the voltage after the arc extinction can be controlled. In addition, by turning on not all IGBTs for generating the pulse current, the pulse current can be adapted to the fault current. A further adaptation of the pulse current could be achieved by changing the number of IGBTs also during the pulse.

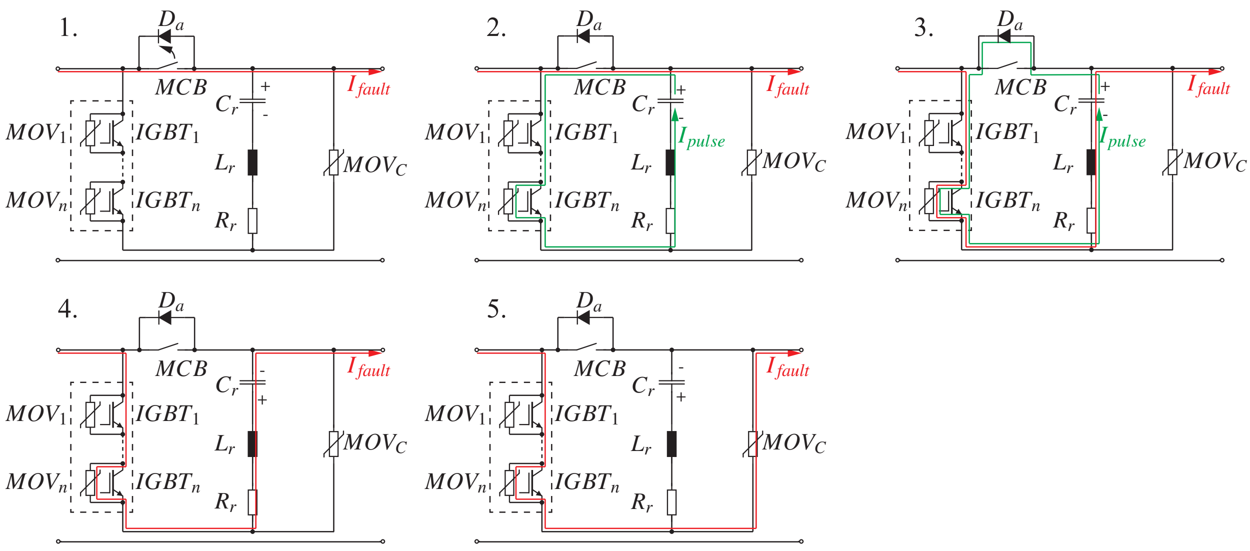

Figure 4: Operation principle of IGBT-LC with adaptable pulse current and partially controllable MCB voltage.

For generating the pulse current, all IGBTs can be turned on (IGBT-all), resulting in the same pulse current as with the system based on thyristors. However, since the IGBTs can be turned off, the IGBTs can block part of the TIV. The TIV increases then faster and can be partially controlled, resulting in a faster decreasing fault current.

However, the topology has the advantage, that the pulse current amplitude and shape can be adapted (IGBT-APC1) to the fault current by varying the number of turned off IGBTs with paralleled varistors. By using more series connected varistors in the pulse current path for generating the pulse current (i.e. turn on less IGBTs), the voltage across the inductor L_r is decreased, resulting in a slower current increase and a lower peak current. Therefore, a pulse current with a peak value only slightly higher than the fault current can be generated, which has a relatively low ${}^{di}/_{dt}$before its maximum. This leads to a low ${}^{di}/_{dt}$ at the zero current crossing in the MCB. Due to the low ${}^{di}/_{dt}$ before the pulse current peak, the inductance value of L_r can be reduced, leading to a faster rise time of the pulse current, and thus also allows to decrease the capacitance value of C_r.

A second, more advanced adaptation of the pulse current (IGBT-APC2) is to change once the number of varistors, which are in the current path during the pulse current. First, a relatively high number of IGBTs are turned on, which results in a fast increase of the pulse current. After a defined time, several IGBTs are turned off, which leads to a lower current slope before the zero current crossing. This second control strategy allows even lower inductance and capacitance values and a faster pulse rise time.

In Fig. 5a), the three possible zero current crossings of the MCB currents for the three control methods IGBT-all, IGBT-APC1 and IGBT-APC2 are shown for hCBs, which generate a maximum ${}^{di}/_{dt} \leq 70{}^{A}/_{\mu s}$. The corresponding pulse currents are given in Fig. 5b). The improved controllability allows to decrease the time until the zero current crossing is generated and therefore to de-

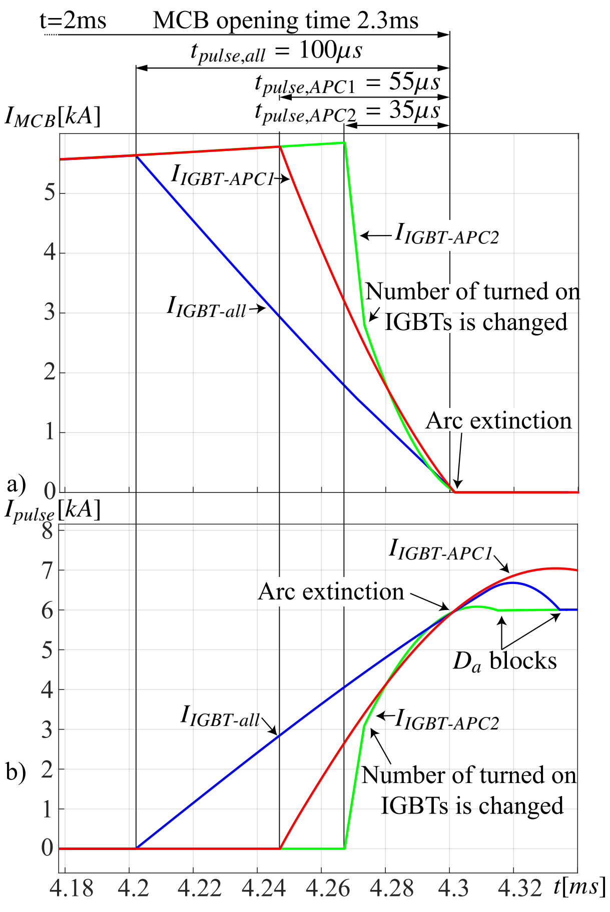

Figure 5: MCB currents (a) and pulse currents (b) for the hCB in Fig.3 for three different control methods. There, a fault at t=0ms, a detection time of 2ms and an opening time of the MS of 2.3ms are assumed. The waveform $I_{IGBT-all}$ is generated by turning on all IGBTs. Waveform $I_{IGBT,APC1}$ is generated by only turning on a part of the IGBTs and inserting varistors instead of the IGBTs in the current path during the pulse. The waveform $I_{IGBT-APC2}$ is achieved by additionally changing the number of IGBTs/varistors in the current path once during the pulse.

crease the values of C_r and L_r (Tab.I). In addition to decreasing the capacitance values, also the initial capacitor voltage can be decreased.

Table I: Capacitance and inductance values of the pulse circuit for the different control approaches in Fig.5.

	IGBT-all	IGBT-APC1	IGBT-APC2
$C_r[\mu F]$	27	11	11
$L_r[\mu H]$	950	300	120

Of course, the topology allows more than only these presented switching strategies, e.g. varying the number of varistors several times during the pulse generation. However, the number of switching operations are limited since the switching time of high voltage IGBTs is in the range of several μs and the switching losses are high. Therefore, with the presented strategies the IGBTs are turned on at the beginning of the pulse current and then individual IGBTs are sequentially turned off during the pulse current.

As additional possibility to reduce the $^{di}/_{dt}$ around the zero current crossing a saturating inductor could be used in series to the MCB (Fig.6). The inductor saturates at relatively small currents and therefore only influences the MCB current around the zero current crossing.

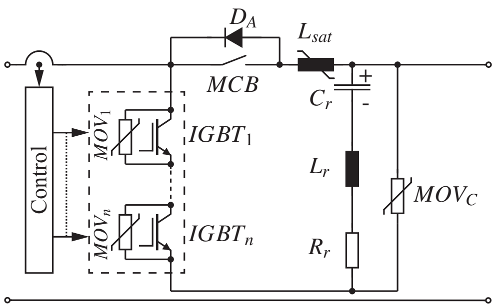

Figure 6: IGBT-LC with saturating inductance L_{sat}.

For generating the pulse current, it must be taken into account that the fault current amplitude and waveform in the MCB cannot be predicted exactly since it depends on the grid structure, the line impedances and the fault type and location. In addition, the pulse current cannot be immediately adapted to these disturbances. Therefore, the amplitude of the pulse current must be at least as high as the maximum possible fault current to which the fault current could change after turning the IGBTs on. However, the fault current can also be lower and lead to an earlier zero current crossing. Therefore, the generated pulse current must generate a zero current crossing with an acceptable $^{di}/_{dt}$ for the full range of possible fault currents. Thus, the inductance value of L_r is also a trade-off between the time to the zero current crossing from the last switching operation of an IGBT (and the resulting possible current change) and the limitation of the $^{di}/_{dt}$ at the zero current crossing due to the inductance.

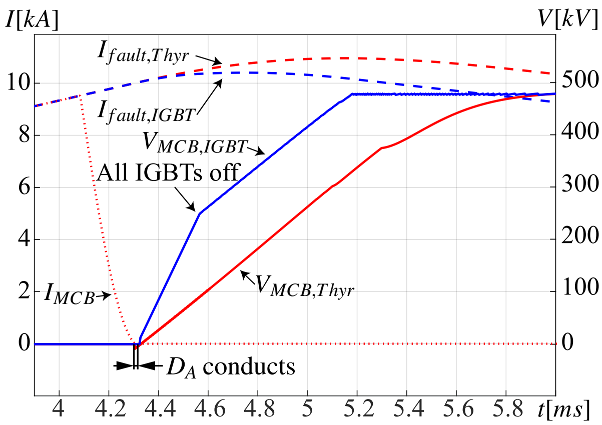

Figure 7: By turning on all IGBTs, the pulse current and $^{di}/_{dt}$ of control method IGBT-all is the same as with a Thyr-LC system. After the zero current crossing, diode D_A starts to conduct and prohibits a negative voltage across the MCB (ITIV in Fig.2). After diode D_A blocks, the IGBTs are turned off to increase the voltage over the MCB faster.

As already mentioned in section 2, the capacitor is designed to achieve the maximum allowed $^{dv}/_{dt}$ of the MCB at the maximum fault current and in case of lower fault currents, the TIV is therefore increasing slower. Here, the IGBTs yield another advantage beside varying the pulse current. Since they can be turned off individually and commutate the fault current to their parallel varistors, the IGBTs can increase the TIV while capacitor C_r is charged (Fig.7). The fault current starts to decrease earlier and the remaining energy in the line inductances is dissipated faster. In addition, the maximum voltage across the MCB can be controlled. After the capacitor is completely charged and as long as the current is still high, the voltage across the MCB is high. Here, IGBTs can be turned on in order to decrease the voltage. As soon as the fault current decreases and the voltage over the varistors decrease, additional IGBTs can be turned off so that additional varistors are added in the fault current path. The additional varistors maintain the high TIV and so decrease the fault current as fast as possible. Another advantage of using IGBTs is that the TIV across the MCB is distributed to the capacitor and the IGBTs. Therefore, neither the capacitor nor the IGBTs must be able to block the TIV. An additional advantage of the new concept is diode D_A so that the ITIV after the zero current crossing is prohibited, since the diode starts to conduct.

For the control of the pulse current, the fault current in the line needs to be measured. While the MCB is opening, the controller estimates the fault current for the time when the MCB is completely opened. With this estimation, the point in time for starting the pulse current and the number of IGBTs to turn on are determined. For control method IGBT-APC2, where the number of IGBTs is changed during the pulse current, the updated number of IGBTs and the point in time for updating are also calculated. However, the point in time for changing the number of IGBTs or even the updated number of IGBTs to turn off could be changed in an advanced control method depending on the fault current development during the pulse.

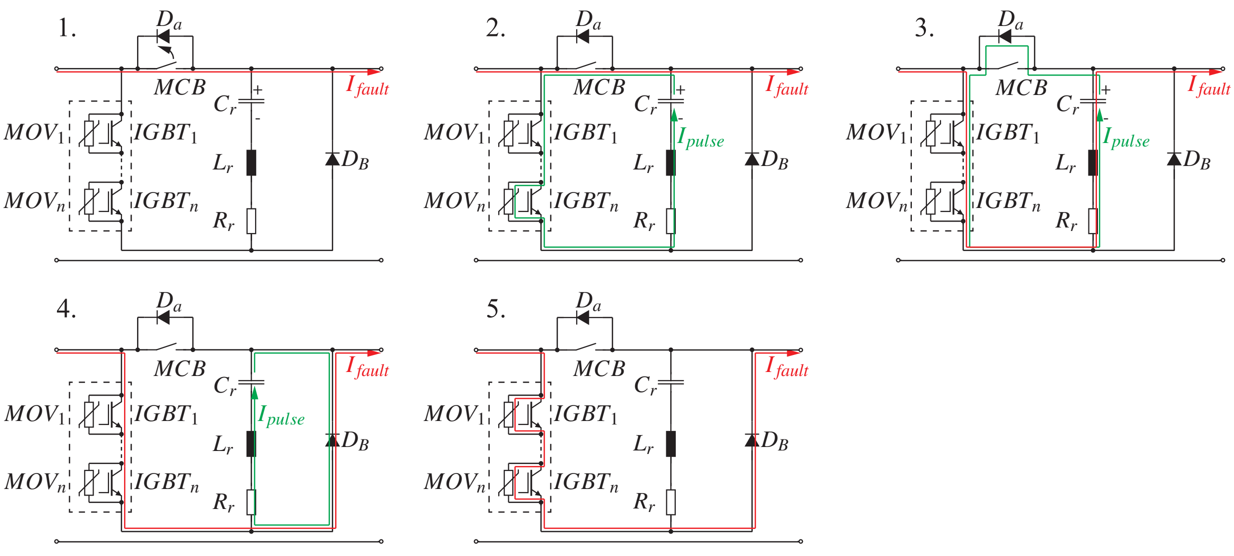

Figure 8: Operation principle of $IGBT - D_B$ with adaptable pulse current and controllable MCB voltage.

3.2 Single pulse hCB with adaptable pulse current and controllable MCB voltage

The IGBT-LC given in Fig. 3 is able to adapt the pulse current shape and to control to some degree the voltage across the MCB. However, the voltage across the MCB still significantly depends on the voltage of capacitor C_r, which therefore requires a value high enough to limit the maximum allowed dv/dt of the MCB. Additionally, for low fault currents, the dv/dt of the TIV is still lower than the maximum allowed dv/dt and thus the fault current starts to decrease later. This could be avoided by the bypass diode D_B parallel to the $R_rL_rC_r$ circuit instead of the varistor MOV_C as shown in Fig. 9.

With bypass diode D_B, the fault clearing of the hCB can be divided into five steps:

- Fig. 8-1: In case of a fault, the current rises until the fault is detected. Then, the MCB is triggered to open.
- Fig. 8-2: As soon as the MCB is completely open, the pulse current is generated by turning on all or part of the IGBTs.
- Fig. 8-3: After the zero current crossing of the current in the MCB, diode D_A starts to conduct until the pulse current decreases and D_A blocks again.
- Fig. 8-4: As soon as D_A blocks, bypass diode D_B starts to conduct and the current of the $R_rL_rC_r$ circuit oscillates (Fig.10) until it decreases to zero. During this step, further IGBTs are turned off and the parallel varistors of the IGBTs already start to dissipate the stored energy of the line.
- Fig. 8-5: When all IGBTs are turned off, the complete stored energy of the line is dissipated is varistors $MOV_1 - MOV_n$.

A main advantage of the additional diode D_B is that the MCB voltage after the zero current crossing is independent of the $R_rL_rC_r$ circuit. Directly after the zero current crossing diode D_A starts to

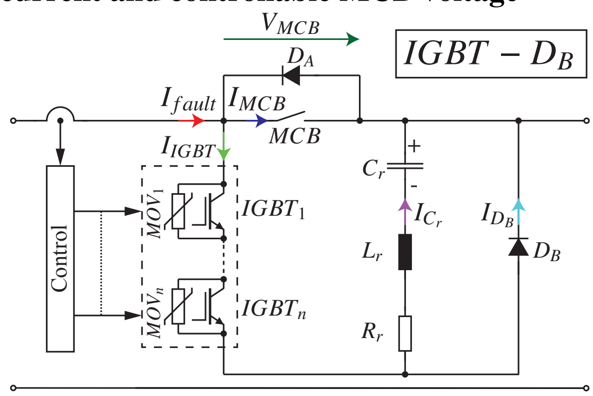

Figure 9: IGBT-D_B: hybrid CB topology with bypass diode D_B. The pulse current waveform amplitude and the MCB voltage can be adapted.

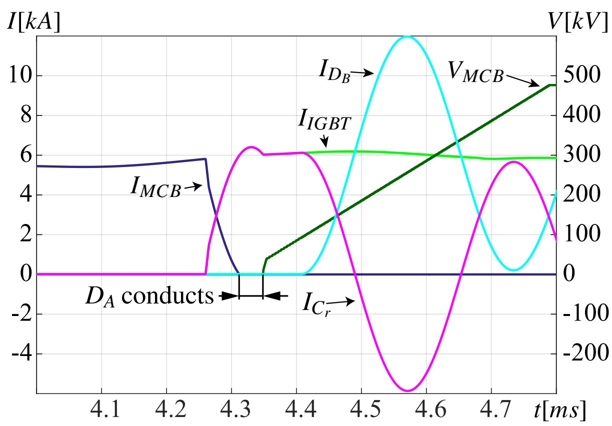

Figure 10: Zero current crossing in the topology $IGBT - D_B$ for a short circuit fault at t=0ms. The zero current crossing is generated after the MCB is completely open after a detection time of 2ms and an opening time of 2.3ms. After the zero current crossing in the MCB, the MCB voltage remains zero until diode D_A blocks again and diode D_B bypasses the $R_rL_rC_r$ circuit. Due to D_B, the voltage across the MCB is equal to the voltage across the turned off IGBTs and thus is controlled increased.

conduct and the voltage across the MCB is zero. As soon as D_A blocks, the MCB voltage is solely defined by the number of varistors in the fault current path respectively by the number of turned off IGBTs. Therefore, the voltage across the MCB can be directly controlled during the fourth and fifth step. Another effect of D_B is that capacitor C_r is not charged by the fault current after the zero current crossing, because C_r is not used to block a part of the TIV as in topology IGBT-LC. Therefore, the maximum voltage across capacitor C_r is much smaller. However, this results in a higher number of semiconductors have to be increased, because they need to block the maximum TIV. An advantage of blocking all the TIV with the semiconductors is the possibility to conduct the line current with the IGBTs and D_B before a turn on of the MCB, so that the MCB can be turned on without arc and the disturbances in the grid at the turn on of the hCB are lower.

3.3 Charging circuit

For charging capacitor C_r, the circuit given in Fig. 9 can be enhanced with a charging circuit as depicted in Fig. 11. For keeping capacitor C_r charged when the hCB is closed, a resistor R_{CC} is connected between the capacitor and the return conductor of the line. However, capacitor C_r must be precharged before the MCB can close in order to allow an immediate turn off after the turn on of the MCB.

To charge C_r before the MCB closes, $IGBT_1 - IGBT_n$ and thyristor T_{ch} are turned on to generate current I_{L_r} in L_{ch} (Fig. 11). First, the current I_{L_r} is increased in the inductors L_r and L_{ch}. Diode D_B blocks here after capacitor C_r is slightly charged via D_B. Current I_{L_r} increases further until $IGBT_1 - IGBT_n$ are turned off or the resistor R_{ch} limits the maximum current. As soon as the IGBTs $IGBT_1 - IGBT_n$ are turned off, the current is commutated to $MOV_1 - MOV_n$ and the current in L_r decreases (Fig. 12). Therefore, the current in L_{ch} commutates to the freewheeling diode D_{ch} (I_C) and charges capacitor C_r. By turning a part of the IGBTs on again, the current in L_{ch} and L_r increases again. The number of IGBTs, which are not turned off is such that capacitor C_r is not discharged over diode D_A. This charging process is repeated several times until capacitor C_r is charged and the MCB can be closed.

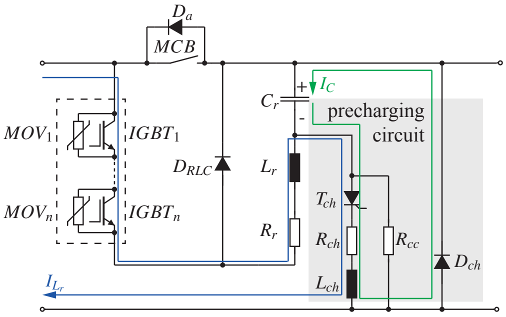

Figure 11: Circuit of Fig. 9 with charging circuit.

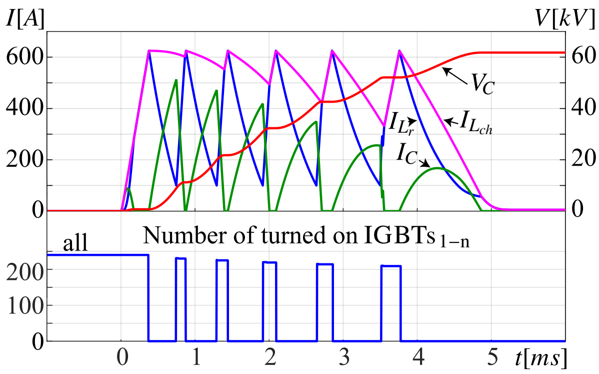

Figure 12: Precharging of C_r with the circuit given in Fig.11: The IGBTs and the thyristor are turned on generating a current in L_{ch}. By turning the IGBTs off, a part of the current in L_{ch} commutates to D_{ch} and charges C_r.

3.4 Early turn off at low fault currents

So far, topologies with an MCB first open the MCB completely and then extinguish the arc with the pulse current. The main reason to wait until the MCB is completely open before triggering the pulse current is to reduce the risk of a reignition. However, a secure arc extinction is also possible for the same current with smaller gap distances if the maximum $^{di}/_{dt}$ at the zero current crossing is decreased [14].

This early arc extinction can be used for reducing the arcing time and the energy, which improves the life time of the MCB [19]. A second advantage is the possibility to increase the TIV while the MCB is still opening. This results in a decreased maximum fault current and a lower energy to dissipate in the hCB.

For performing always an early turn off, the $^{di}/_{dt}$ for all possible fault currents would have to be decreased. This would result in higher values for the passive components. However, the IGBT-LC with a pulse circuit designed for generating a specific

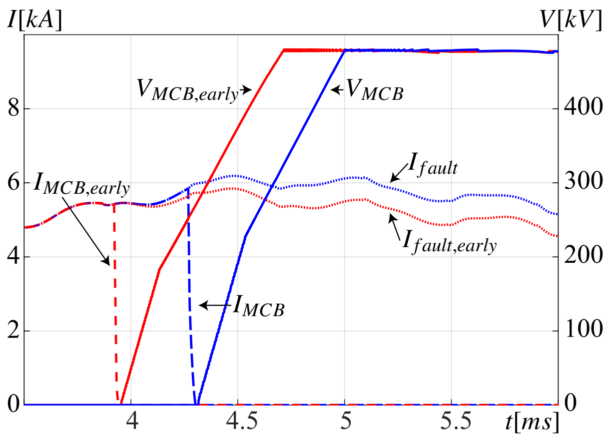

Figure 13: Fault and MCB current as well as MCB voltage during a conventional turn-off with IGBT-APC2 (blue) and an early turn off with IGBT-APC2 (red) for a short circuit fault at t=0ms in 60km distance. Due the early arc extinction, the TIV rises earlier and the fault current starts already to decrease before the MCB is completely open.

Table II: Maximum fault current and dissipated energy from the grid for normal/early turn off at different distances

	0km	20km	40km	60km	80km
$\hat{I}_f$ [kA]	10.38 /10.38	8.43/8.05	7.13/6.86	6.19/5.85	5.59/5.15
E_{grid} [MJ]	24.8/ 24.8	20/18.2	17/15.6	15/13.2	13.7/12

maximum $^{di}/_{dt}$ at the zero current crossing experi-
ence this maximum $^{di}/_{dt}$ only for high fault currents. The reason is that the generation of a pulse current for high fault currents needs the turn on of most of the IGBTs and therefore the turn on or off of one additional IGBT changes the pulse current significantly. For low fault currents only a low number of IGBTs are turned on, which allows to adapt the pulse current much easier. Thus for low fault currents, the $^{di}/_{dt}$ can be decreased, the arc earlier extinguished and therefore the performance increased (Tab.II). Two exemplary turn off processes of a CB designed for a maximum $^{di}/_{dt} = {}^{70A}/_{\mu s}$ are shown in Fig.13. Since the zero current crossing can be achieved with a low $^{di}/_{dt} = {}^{24A}/_{\mu s}$, the arc is extinguished 0.35ms earlier with a maximum current of 5850A instead of 6190A.

4 Comparison

In this section, the simulation results of the two presented topologies are compared in terms of passive components, required semiconductors and performance with the existing concept discussed in section 2. The different concepts have been designed for a DC-grid according to the parameters in Tab.III with the line parameters given in Tab.IV. The main design criteria are to minimize the size of the passive components and the required semiconductors, while being able to generate a zero current crossing as soon as the MCB is completely open.

The components of the concepts are compared in terms of the maximum stored energy in the inductors and the capacitors, which is approximately equivalent to the component volume, the maximum energy to dissipate and the required ratings of the semiconductors. The performance of the hCBs is compared based on the maximum occurring fault current in the line, the interruption time and the energy drawn during the fault from the grid.

Table III: Design parameters of the monopolar DC grid

Nominal direct voltage V_{DC}	320 kV
Rated power P	200 MW
Length of line	100 km
Maximum overvoltage	480kV
Maximum $^{dv}/_{dt}$ of MCB	1 kV/μs
Assumed detection time	2.0 ms
Opening time of the MCB	2.3 ms
Maximum $^{di}/_{dt}$ for arc extinction	$^{70A}/_{\mu s}$
Maximum TIV	480 kV
Current limiting inductances	146.8μH

Table IV: Parameters of the 320kV HVDC OHL [20], which is assumed in the simulations.

Line inductance	L_{line}	935.6 μH/km
Line resistance	R_{line}	0.0114 Ω/km
Line capacitance	C_{line}	12.3nF/km

The results of the simulations (Tab.V) show that the change from Thyr-LC to IGBT-all already allows to decrease the maximum fault current in the line and therefore also decreases the maximum stored energy in the inductances. This is achieved by turning IGBTs off after the arc extinction to increase the TIV across the MCB faster. The faster increase of the TIV and keeping the TIV constant at the maximum allowed MCB voltage results also in a shorter time to zero current and therefore a lower energy to dissipate in the varistors. Additionally, the stored energy in the capacitor is decreased since the maximum voltage of varistor MOV_C is decreased, since varistors $MOV_1 - MOV_n$ parallel to the IGBTs block a share of the TIV.

Thyr-LC and IGBT-all achieve the low $^{di}/_{dt}$ of the zero current crossing with comparably high values of inductance L_r and capacitance C_r, which results in a high current in diode D_A and therefore

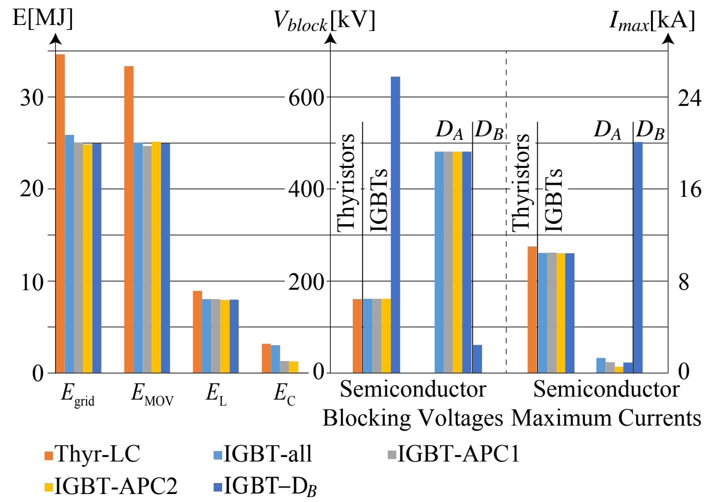

Figure 14: Comparison of required semiconductor blocking voltage, volume of passive components and maximum dissipated energy of the grid.

Table V: Comparison of required semiconductor blocking voltage/passive components and the performance of the CB in terms of maximum current, maximum time from start of the fault until clearing and dissipated energy.

	Unit	Thyr-LC	IGBT -all	IGBT-APC1	IGBT- APC2	$IGBT - D_B$
Inductive energy storage E_L	[MJ]	8.88	7.99	7.99	7.91	7.92
$\mapsto$ in current limiting inductances	[MJ]	8.82	7.94	7.98	7.9	7.9
$\mapsto$ in the pulse circuit	[kJ]	56.6	51.4	16.3	6.45	11.2
Capacitive energy storage E_C	[MJ]	3.15	2.99	1.26	1.25	0.02
Energy dissipation E_{MOV}	[MJ]	33.3	25	25.5	25.1	24.9
IGBTs blocking voltage	[kV]	-	161	161	161	643
Diode D_A blocking voltage	[kV]	-	480	480	480	480
Diode D_B blocking voltage	[kV]	-	-	-	-	60
Thyristors blocking voltage	[kV]	160	-	-	-	-
Maximum IGBT current	[kA]	-	10.4	10.43	10.38	10.38
Maximum diode current of D_A	[A]	-	1300	1000	500	900
Maximum diode current of D_B	[kA]	-	-	-	-	20
Maximum thyristor current	[kA]	10.96	-	-	-	-
Stress of IGBTs $\int I_{IGBT}dt$	[As]	-	32.7	36	35.5	24.28
Stress of Diodes D_A $\int I_{diode}dt$	[As]	-	0.04	0.04	0.011	0.036
Stress of Diodes D_B $\int I_{diode}dt$	[As]	-	-	-	-	54.4
Stress of Thyristors $\int I_{thyr}dt$	[As]	86.56	-	-	-	-
Peak fault current $\hat{I}_f$	[kA]	10.96	10.4	10.43	10.38	10.38
Time to zero t_{fault}	[ms]	32.5	16.22	15.2	15.2	15.2
Dissipated energy from grid E_{grid}	[MJ]	34.6	25.8	25	24.8	24.9

a long time until D_A blocks. IGBT-LC with the advanced control methods IGBT-APC1 and IGBT-APC2, which adapt the pulse current, result in a lower current in D_A with shorter duration and with lower values of inductance L_r and capacitance C_r. Due to the earlier blocking of D_A, the TIV across the MCB starts to increase earlier. However, due to the smaller inductances, the maximum fault current decreases only slightly in case of IGBT-APC2. This lower current also results in a decreased stored inductive energy, especially in L_r with its decreased inductance value. Additionally, the decreased inductance value and the shorter rise time of the pulse current in L_r decreases the required energy for the pulse current and therefore allows to decrease the capacitance value of C_r.

The additional diode D_B in $IGBT - D_B$ allows to control the MCB voltage completely with the number of turned off IGBTs and leads to the same maximum fault current. Additionally, the capacitor does not have to block a share of the TIV across the MCB, which decreases the maximum capacitive stored energy. However, the number of IGBTs must be designed to withstand the maximum TIV and the currents in D_B are very high.

5 Conclusion

In this paper, a new hCB topology using a pulse current to extinct the arc in the MCB at the turn off is presented. The proposed topology uses a series connection of IGBTs with parallel varistors in the pulse circuit, which allows to adapt the pulse current to the fault current amplitude. With the adaptation of the pulse current, the capacitor volume could be decreased by 60% and the inductance volume in the pulse circuit by 88% while a low ${}^{di}/_{dt}$ at the zero current crossing in the MCB could be maintained. Another advantage is that the IGBTs only need to block a part of the TIV and therefore the number of IGBTs is comparably low. A variant of the proposed hCB concept, uses an additional diode and therefore allows full control of the MCB voltage after the arc extinction. Additionally, the diode enables the hCB to precharge the line before the MCB is closed and so avoids grid disturbances. This concept allows to decrease the capacitor volume by 98.4% compared to the first concept, but has four times more IGBTs. It has been also shown, that the increased controllability of the pulse current shape and MCB voltage allows to decrease the ${}^{di}/_{dt}$ at the zero current crossing for low fault currents, which enables to extinguish the arc earlier and therefore results in smaller fault currents without increasing the number and volume of components.

Acknowledgments

The authors would like to thank SCCER-FURIES for their financial support of the research work. The authors would also like to thank T. Schultz and Ch. Franck of the HVL ETH Zurich for valuable discussions.

References

[1] C. Franck, "HVDC Circuit Breakers: A Review Identifying Future Research Needs," *IEEE Trans. on Power Delivery*, vol. 26, no. 2, pp. 998–1007, April 2011.

[2] D. Schmitt, Y. Wang, T. Weyh, and R. Marquardt, "DC-side fault current management in extended multiterminal-HVDC-grids," in *9th Int. Multi-Conf. on Systems, Signals and Devices (SSD)*, March 2012.

[3] J.-B. Curics, J. Descloux, S. Nguefeu, P. Rault, L. Violleau, F. Colas, X. Guillaud, W. Grieshaber, and B. Raison, "DEMO 3 testing results from DC network mock-up and DC breaker prototype status report for European Commission Deliverable: D11.3," *Twenties Deliverable*, Feb 2013.

[4] M. Bucher and C. Franck, "Fault current interruption in multiterminal HVDC networks," *IEEE Trans. on Power Delivery*, no. 99, 2015.

[5] C. D. M. Oates, E. K. Chukaluri, and W. R. Crookes, "Circuit breaker apparatus," WO Patent 2 012 100 831, Aug. 2, 2012.

[6] A. Jehle, D. Peftitsis, and J. Biela, "Unidirectional hybrid circuit breaker topologies for multi-line nodes in HVDC grids," in *18th European Conf. on Power Electronics and Applications (ECCE Europe)*, Sept 2016.

[7] D. Peftitsis, A. Jehle, and J. Biela, "Design considerations and performance evaluation of hybrid DC circuit breakers for HVDC grids," in *18th European Conf. on Power Electronics and Applications (ECCE Europe)*, Sept 2016.

[8] J. Häfner and B. Jacobson, "Proactive hybrid HVDC breakers–A key innovation for reliable HVCD grids," in *Symposium on the electric power system of the future–Integrating supergrids and micro-grids*, Sept 2011.

[9] R. Sander, M. Suriyah, and T. Leibfried, "A Novel Current-Injection Based Design for HVDC Circuit Breakers," in *Conf. for Power Electronics, Intelligent Motion, Renewable Energy & Energy Management (PCIM)*, May 2015.

[10] W. Grieshaber, J.-P. Dupraz, D.-L. Penache, and L. Violleau, "Development and test of a 120 kV direct current circuit breaker," in *45th CIGRE Session*, Aug. 2014.

[11] F. B. Effah, A. J. Watson, C. Ji, E. Amankwah, C. M. Johnson, C. Davidson, and J. Clare, "Hybrid HVDC circuit breaker with self-powered gate drives," *IET Power Electronics*, vol. 9, no. 2, pp. 228–236, 2016.

[12] L. Ängquist and S. Norrga, "Arrangement, system, and method of interrupting current," WO Patent 2 016 003 357, Jan. 7, 2016.

[13] Y. Wang and R. Marquardt, "A fast switching, scalable DC-Breaker for meshed HVDC Super Grids," in *Conf. for Power Electronics, Intelligent Motion, Renewable Energy & Energy Management (PCIM)*, May 2014.

[14] Y. Shan, T. C. Lim, B. W. Williams, and S. J. Finney, "Successful fault current interruption on DC circuit breaker," *IET Power Electronics*, vol. 9, no. 2, pp. 207–218, 2016.

[15] J. Kaumanns, "Influence of the arcing time on the interruption behaviour and current zero conditions of vacuum circuit breakers," in *Proc. 8th Int. Symposium on Discharges and Electrical Insulation in Vacuum (ISDEIV)*, Aug 1998.

[16] R. P. P. Smeets and V. Kertesz, "Evaluation of high-voltage circuit breaker performance with a validated arc model," *IEE Proc. - Generation, Transmission and Distribution*, vol. 147, Mar 2000.

[17] K. Arimatsu, Y. Yoshioka, S. Tokuyama, Y. Kato, and K. Hirata, "Development and interrupting tests on 250KV 8kA HVDC circuit breaker," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-104, no. 9, Sept 1985.

[18] T. Schultz and C. M. Franck, "Interruption capability investigation of a model gas circuit-breaker for HVDC switching applications," in *21st Int. Conf. on Gas Discharges and their Applications*, Sept 2015.

[19] H. Zhihui, D. Xiongying, W. Huiming, and Z. Jiyan, "Improvement of breaking capability of vacuum circuit breaker using controlled fault interruption," in *2nd Int. Conf. on Electric Power Equipment - Switching Technology (ICEPE-ST)*, Oct 2013.

[20] F. B. Ajaei and R. Iravani, "Cable surge arrester operation due to transient overvoltages under DC-side faults in the MMC-HVDC link," *IEEE Trans. on Power Delivery*, vol. 31, no. 3, June 2016.