

RISC-V Meets 22FDX: an Open Source Ultra-low Power Microcontroller Platform for Advanced FDSOI Technologies

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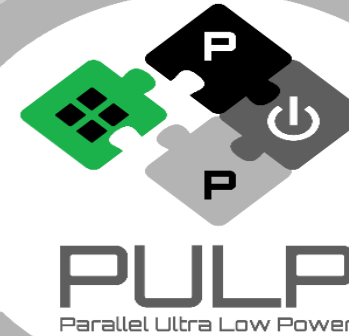
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RISC-V Meets 22FDX: an Open Source Ultra-low Power Microcontroller Platform for Advanced FDSOI Technologies

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³GLOBALFOUNDRIES



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ETH zürich

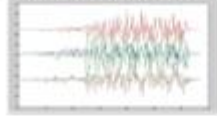
²Integrated Systems Laboratory

09.05.2018

Near Sensor (aka Edge) Processing

Sense

MEMS IMU



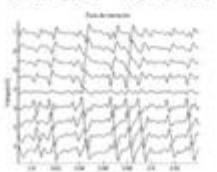
MEMS Microphone



ULP Imager



EMG/ECG/EIT



100 μ W \div \sim 10 mW

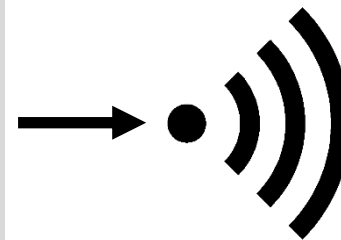
Onchip Processing



1 \div 3 GOPS
1 \div 30 mW

Battery + Harvesting powered
 \rightarrow a few mW power envelope

Transmit



Idle: \sim 1 μ W
Active: \sim 50mW

- ✓ Smart Architecture
- ✓ Parallel Processing
- ✓ Power-saving Design
- ✓ Near-Threshold
- ✓ Low Power Technology



PULP is Open-Source & Free

Releases

1

February 2016

First release of **PULPino**, our single-core microcontroller

2

May 2016

Toolchain and compiler for our RISC-V implementation (**RI5CY**), DSP extensions

3

August 2017

PULPino updates, new cores Zero-riscy and Micro-riscy, **FPU**, toolchain updates

4

Begin February 2018

PULPissimo
ARIANE: 64-bit RISC-V core

5

End February 2018

OPEN-PULP



Community Contributions

June 2017

Porting of **Verilator** and **BEEBS** benchmarks to PULPino

<https://github.com/embecosm/ri5cy>



1

September 2017

Porting of **ARM CMSIS** to PULPino

<https://github.com/misaleh/CMSIS-DSP-PULPino>



2

November 2017

Numerous **Bug fixes** to RiscV in PULPino

<https://github.com/pulp-platform/riscv>



3

December 2017

STING: Open-Source Verification Environment for PULPino

<http://valtrix.in/programming/running-sting-on-pulpino>

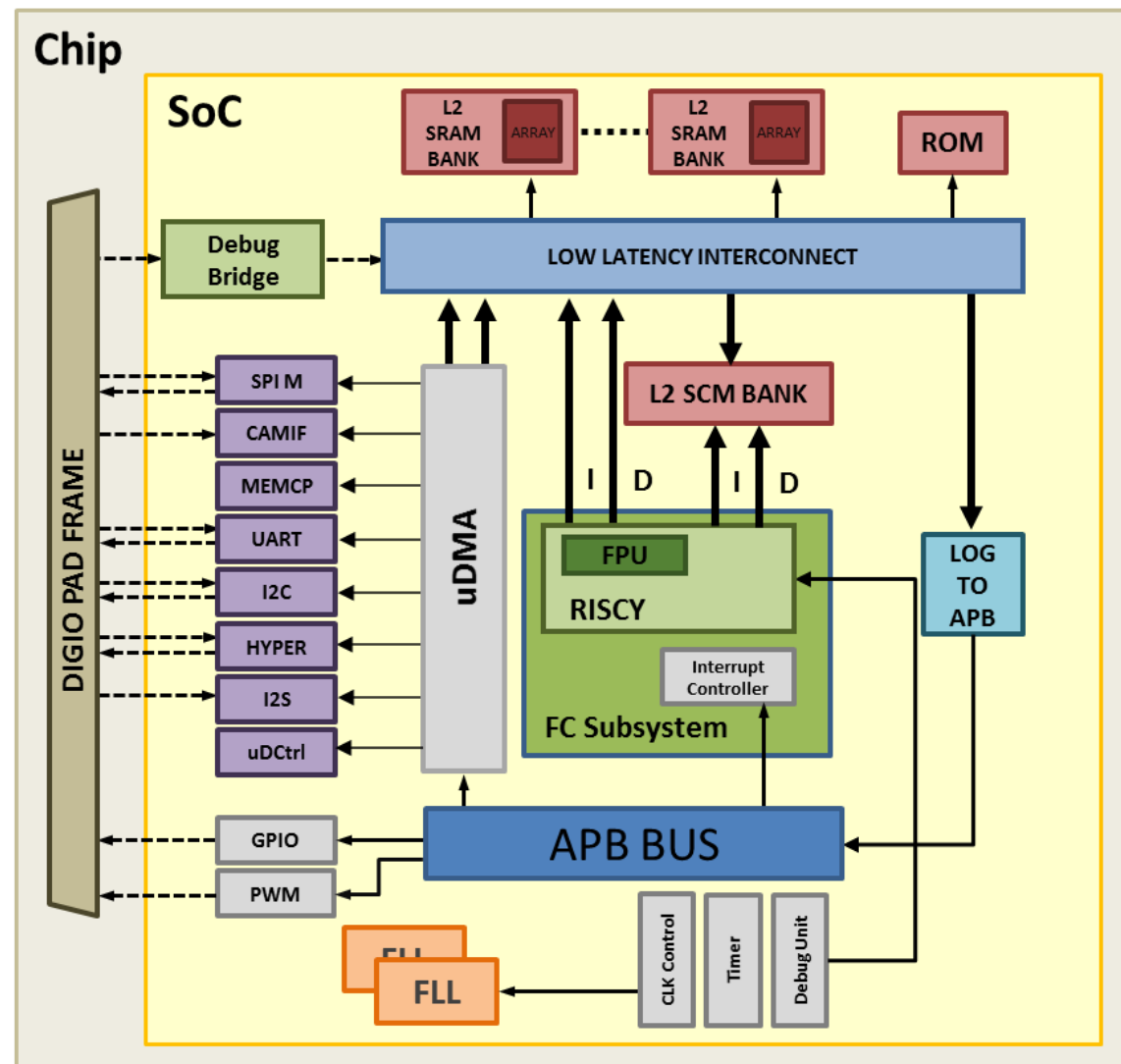


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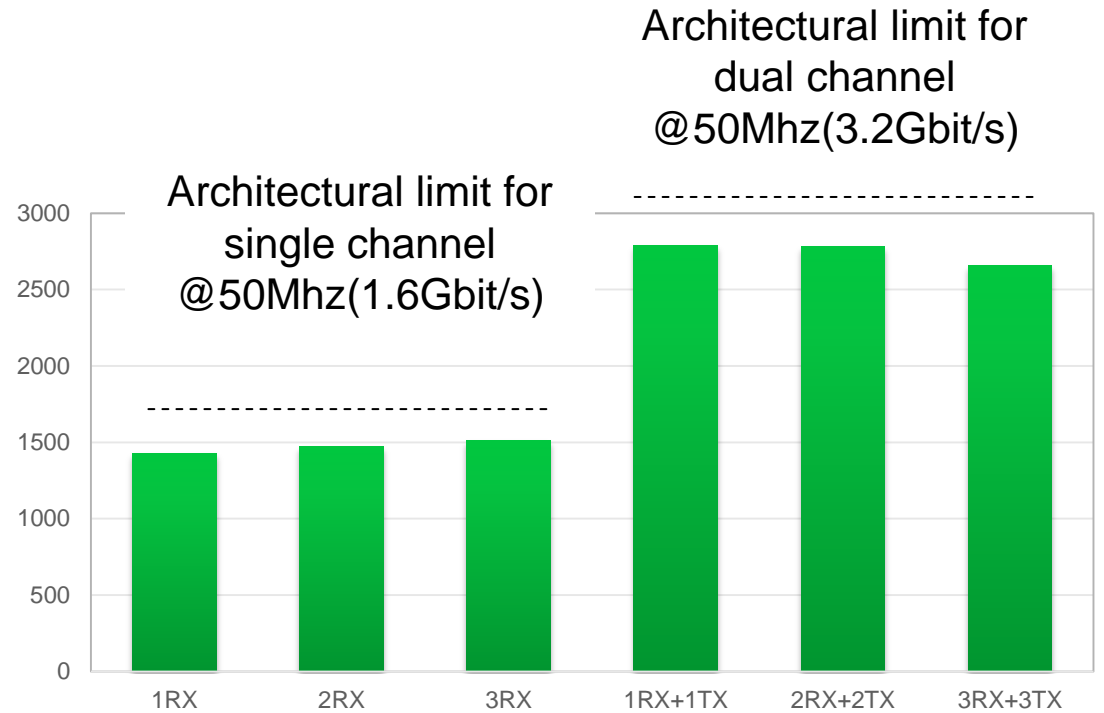
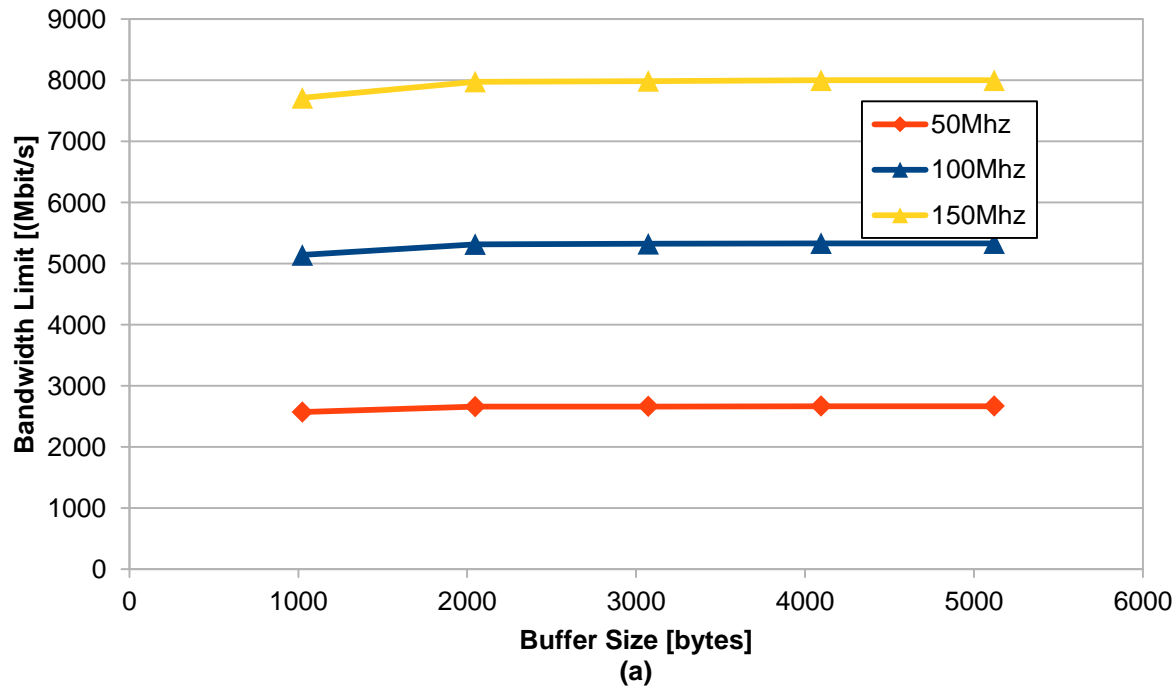
Download PULP @ <https://github.com/pulp-platform>

Quentin: GF22FDX PULPissimo Implementation

- RISC-V based advanced microcontroller
 - 512kB of L2 Memory
 - 16kB of energy efficient latch-based memory (L2 SCM BANK)
- Rich set of peripherals:
 - QSPI (up to 280 Mbps)
 - HyperRam + HyperFlash (up to 100 MB/s)
 - Camera Interface (up to 320x240@60fps)
 - I2C, I2S (up to 4 digital microphones)
 - JTAG (Debug), GPIOs,
 - Interrupt controller, Bootup ROM
- Autonomous IO DMA Subsystem (μ DMA)
- Power management
 - 2 low-power FLLs (IO, SoC, ...)

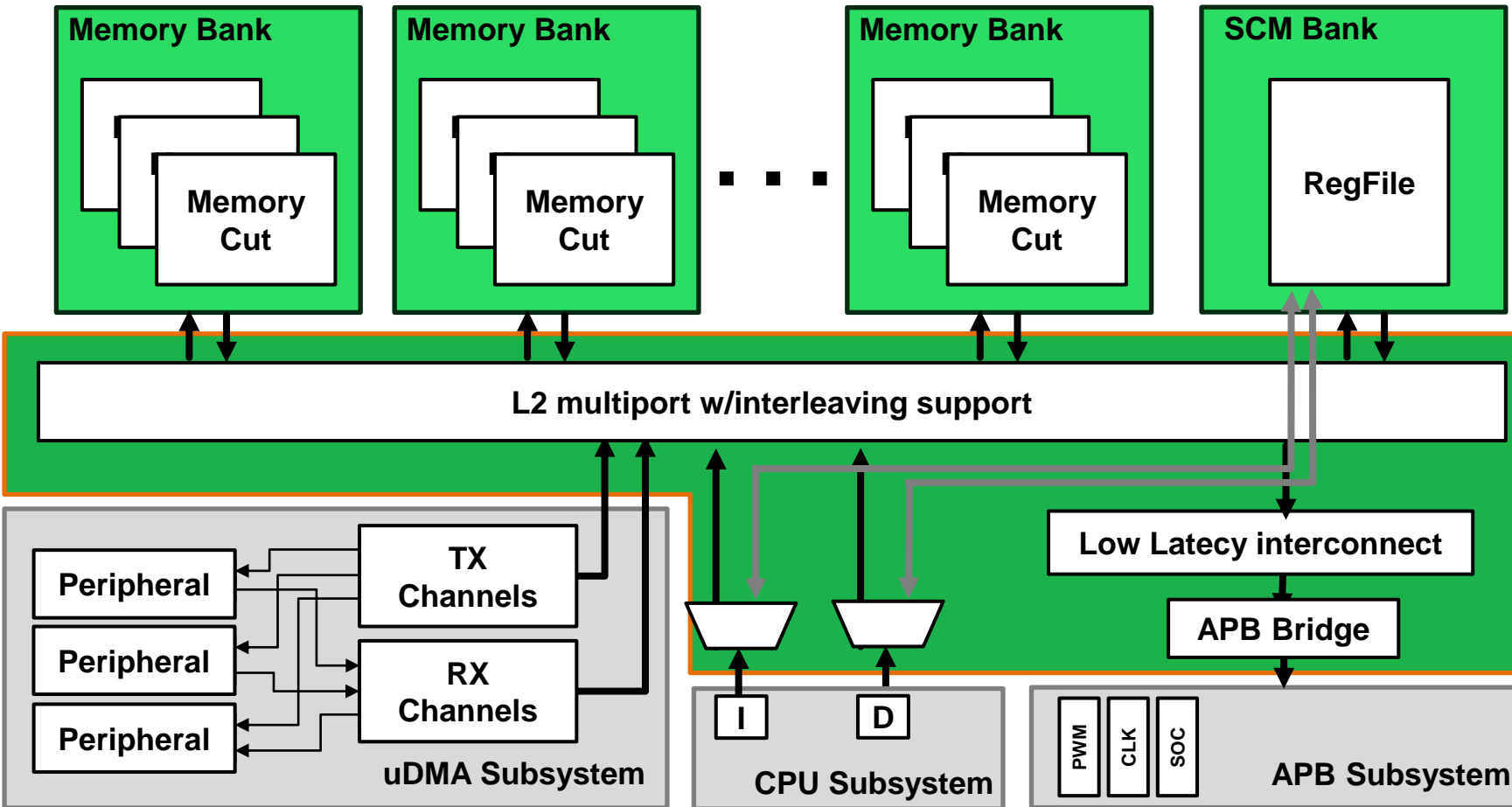


Efficient I/O subsystem: the μ DMA



- Transfers bandwidth close to the physical limit of the architecture
- A single channel can saturate the memory port (can work at full BW)
- Bandwidth is not affected by peripherals buffer size

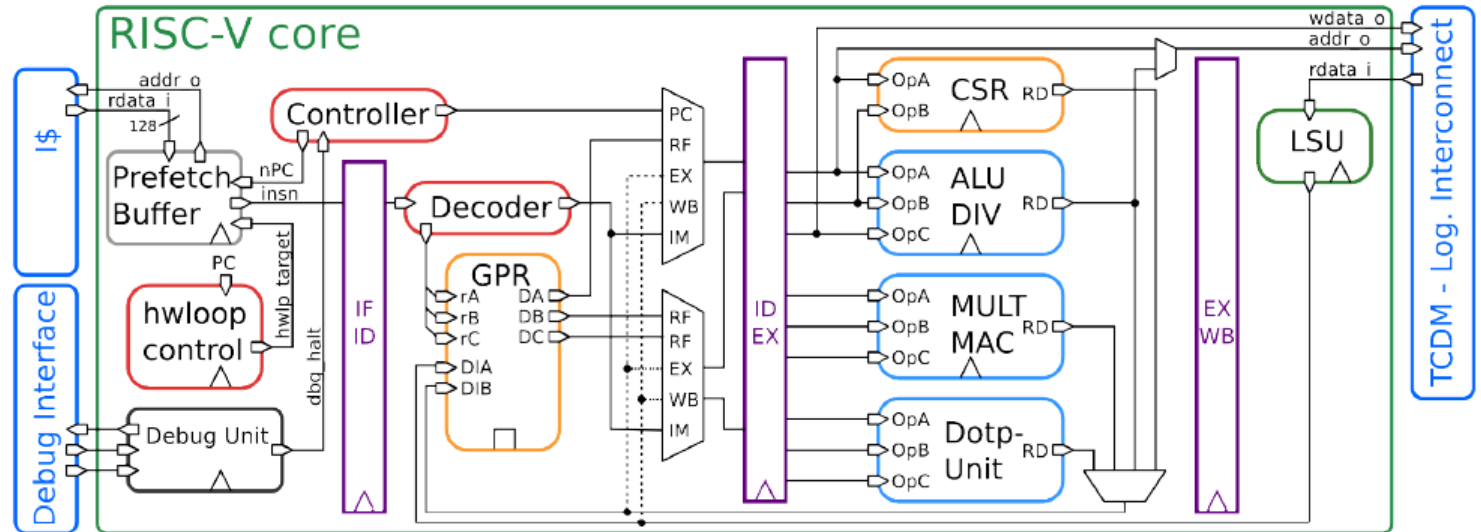
Efficient Interconnect



- ✓ Interleaving to reduce contention: 4 Banks
- ✓ 2 Banks non interleaved for private data and code
- ✓ 1 SCM Bank for NTC

RI5CY Processor

- 4-stage pipeline
 - RV32IMFCXpulp
 - 70K GF22 nand2 equivalent gate (GE) + 30KGE for FPU
 - Coremark/MHz 3.19
- Includes various extensions
 - pSIMD
 - Fixed point
 - Bit manipulations
 - HW loops



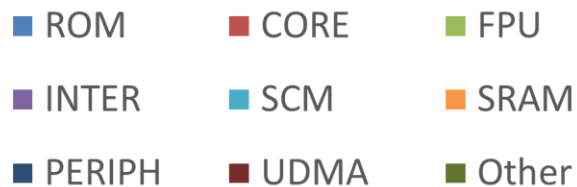
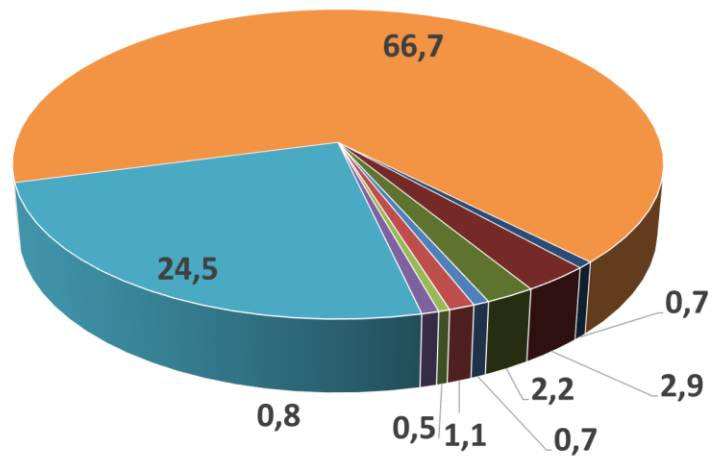
- Floating Point Unit:
 - IEEE 754 single precision
 - Iterative DIV/SQRT (7 cycles)
 - Pipeline MAC, MUL, ADD, SUB, Cast
 - Single cycle load, store, min, max, cmp etc

Thanks for all the external users bugs report!

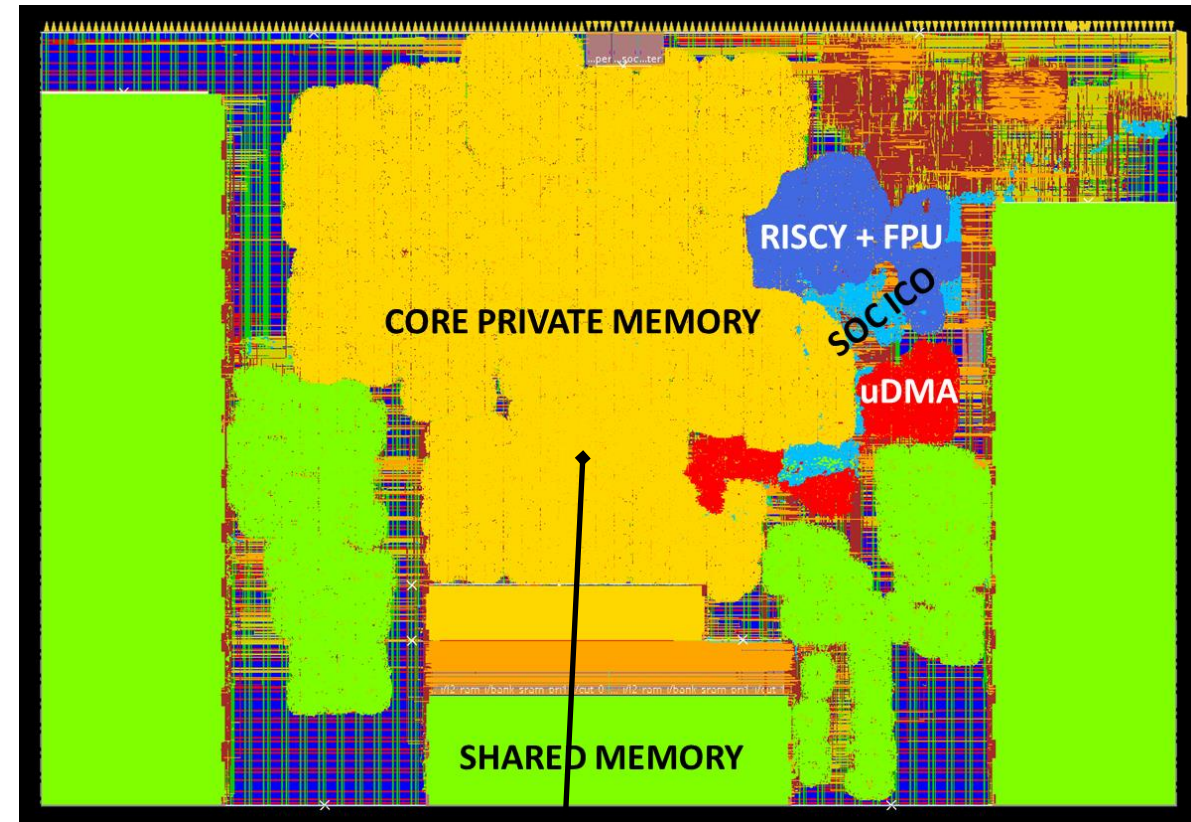
Implementation Results

- Floorplan Area: 2,31 mm²
- Effective Area: 1,22 mm²

Area Breakdown

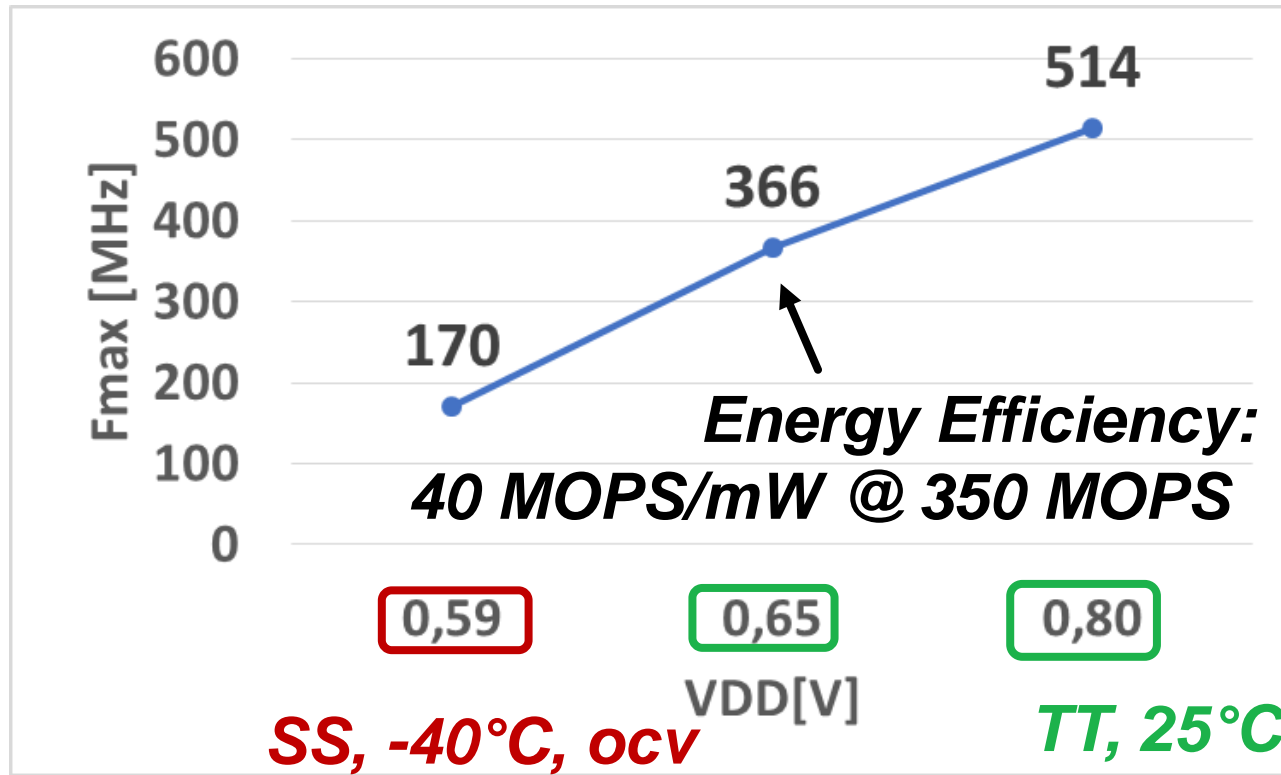


Quentin SoC layout

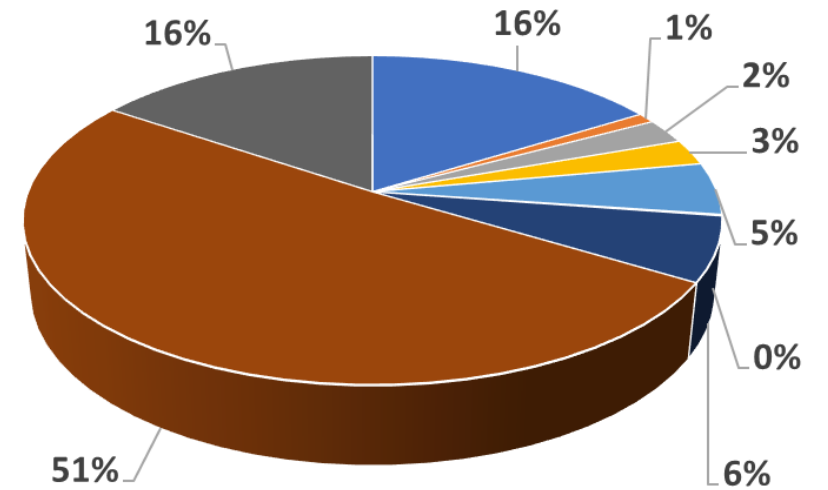


Peak Density: 90%

Estimated Energy Efficiency



Total Power @ 350 MHz, 0.65V = 8,5 mW

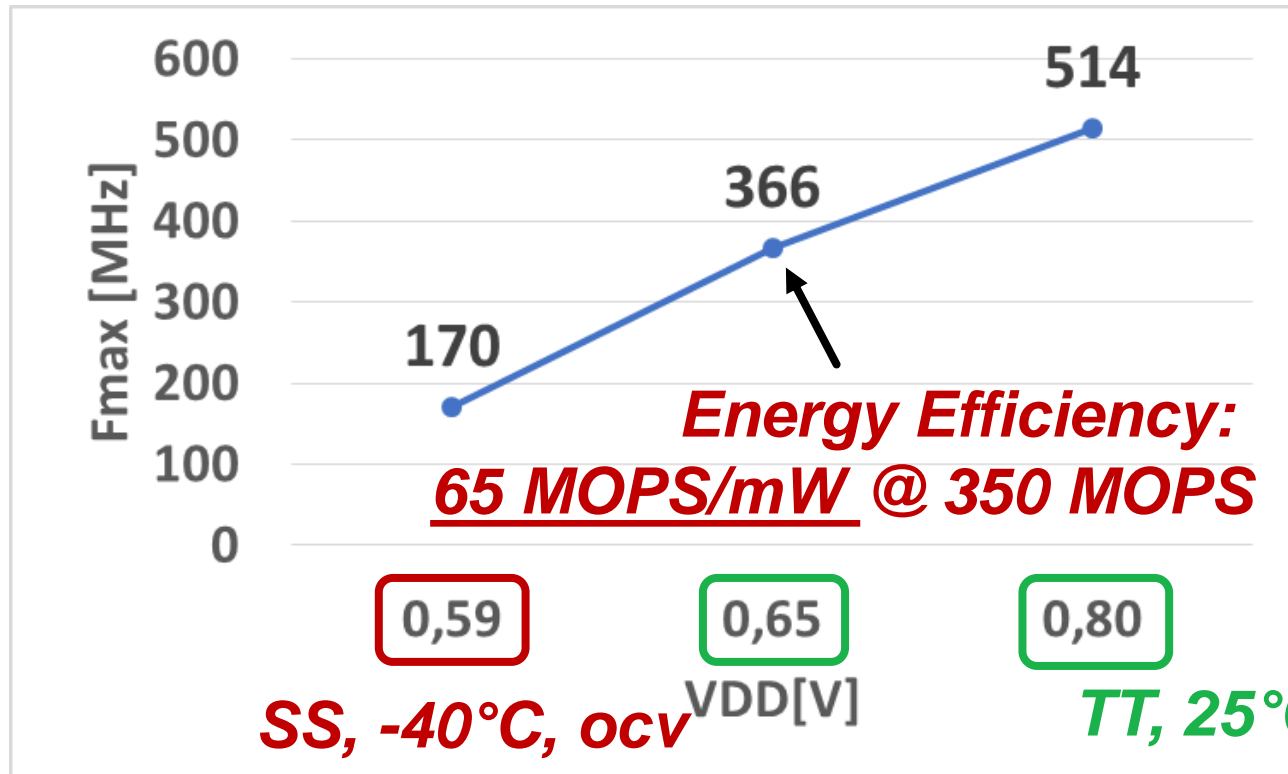


- CORE ■ FPU ■ INTERC
- PERIPH ■ uDMA ■ ROM
- SCM ■ SRAM ■ OTHER

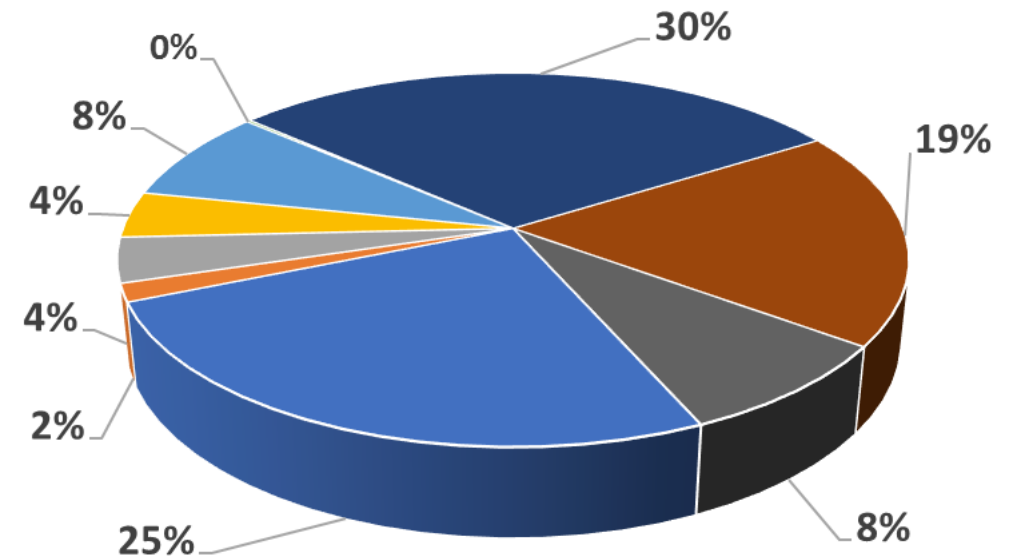
Leakage Power @ 0.65V = 1,2 mW

1.4x better performance (350MHz vs. 250 MHz)
4x better energy efficiency (40 vs. 14 MOPS/mW)
Than our previous design in 40nm technology

Execution on Energy-Efficient SCM



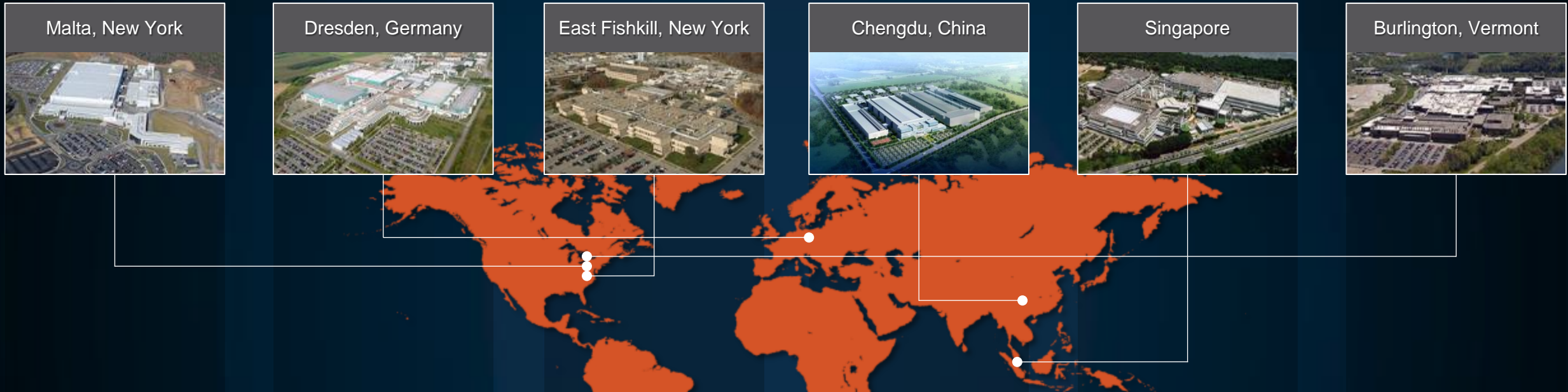
Total Power @ 350 MHz, 0.65V = 5,5 mW



- CORE ■ FPU ■ INTERC
- PERIPH ■ uDMA ■ ROM
- SCM ■ SRAM ■ Other

1.5x better energy efficiency than execution from SRAM

GF – Global Presence in Semiconductor Manufacturing



TECHNOLOGY NODES

14, 12, 7nm

28, 22, 12nm

90–22nm

180–22nm

180–40nm

350–90nm

CAPACITY (WAFERS / MONTH)

Up to 60k
(300mm)

Up to 80k
(300mm)

Up to 20k
(300mm)

Up to 85k
(300mm)

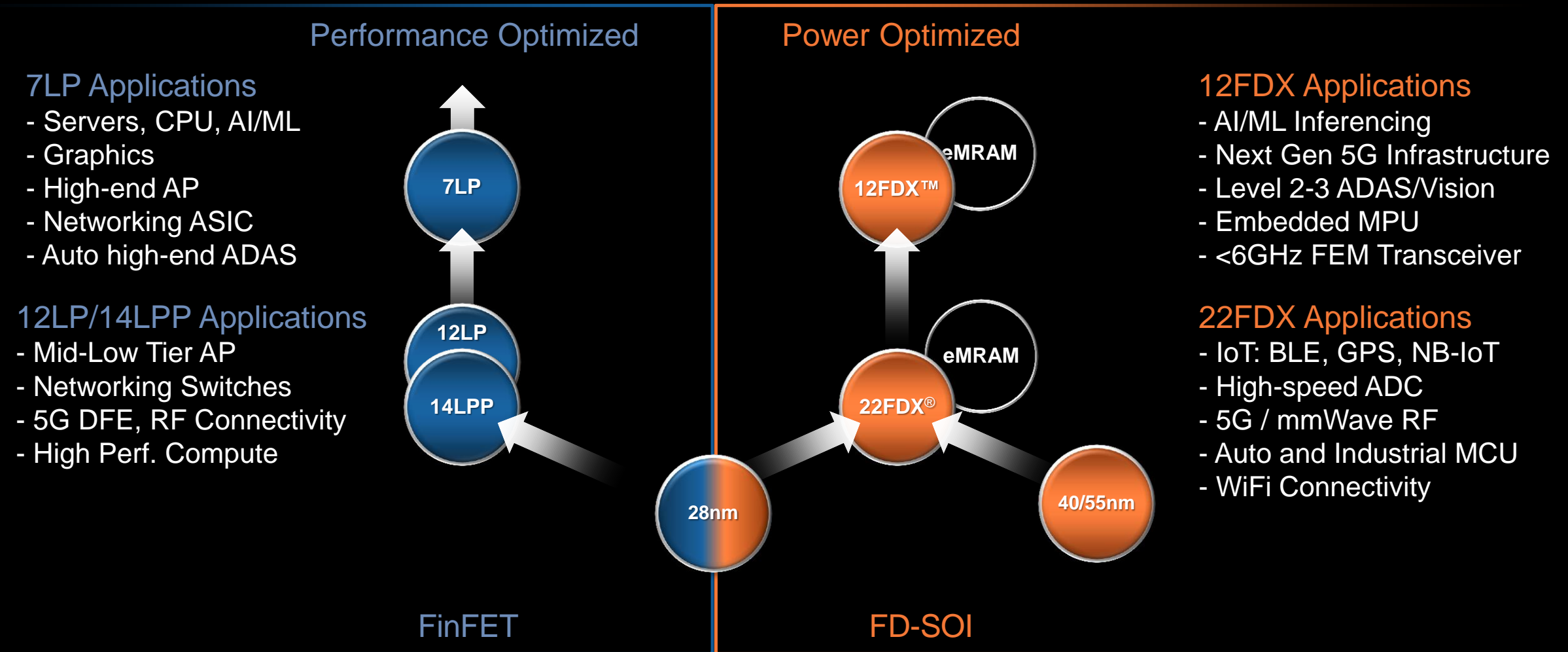
68k (300mm)
93k (200mm)

40k
(200mm)

Up to 10M Wafers / Year

200mm equivalents

GF Has the Industry's Best Dual-Track Roadmap





22FDX[®] for IoT, Automotive and RF

Compelling

- FinFET-like performance for customer who still want to use planar devices
- Ultra-low voltage (0.4V)
- Ultra-low leakage (1pA/μm)
- MRAM integration for IoT and Auto-MCU
- Automotive grade 2 and 1, mmWave / Radar
- Benchmark RF performance (>400GHz), and PA integration

Relevant

- IoT - ARM, RISC-V processors for NB-IoT and AI – ML functions
- Automotive - ADAS /Vision, Infotainment, Body Electronics MCU, Radar
- RF - <6GHz: Connectivity (BLE, Wi-Fi, Zigbee), Cellular (3G, 4G LTE, 5G)
- RF – mmWave >26GHz, 5G infrastructure, ADC/DAC integration

FDXcelerator™ Accelerating RISC-V Developers and Partners

Reduce time to market and facilitate FDX™ SoC product design

- Enabling Universities driving RISC-V innovations
 - ETH-Zurich / University of Bologna – PULP Architecture
 - Berkeley Labs, IIT Chennai
- SiFive Core IP targeting Data Center, ML, Automotive and Embedded applications
 - E31, E51 Configurable RISC-V Cores
- Reduced Energy Microsystems - Drones, Robotics, Camera Applications
 - RISC-V IP hardware validated on 22FDX platforms
 - 32bit, 64bit Cores with Neural network IP solutions
- ANDES Cores for IoT, RF Connectivity applications
 - 32bit IP cores for 22FDX platform
 - Power efficient, smaller foot print designs



Conclusion

- **Challenges for next generations IoT End-Nodes:**
 - Energy Efficiency → Near Threshold Computing
 - Performance → FDX 22nm technology offers HP at low VDD
 - PVT Variations → Body Biasing
- **We presented Quentin: FDX 22 Implementation of PULPissimo open-source architecture**
 - Optimized IO subsystem for efficient data transfers
 - Processor optimized for energy efficient near-sensor data analytics
 - Up to 500 MOPS @ 0.8V
 - 45 MOPS/mW @350 MOPS, 0.65V
- ***First step towards silicon-qualified free-open-source RISC-V IPs on GF FDX22 process.***