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A More Accurate Electromagnetic Modeling of WBG Power Modules

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***Abstract*—A major requirement for further development of wide-band gap (WBG) power devices and their applications is the optimization of packages and PCB layouts to enable fast-switching capabilities. Electromagnetic modelling allows the prediction of parasitic inductances, capacitances, and resistances of the current paths within power modules, which cannot be easily approached in measurements. As a result, electromagnetic-circuit-coupled modeling enables the optimization of package layouts and interconnections before manufacturing actual power modules. The accuracy and limitations of present numerical techniques for three-dimensional (3D) electromagnetic modeling of power modules is still neither well understood nor verified. This paper presents the extraction of parasitics of power semiconductor packages using two electromagnetic modelling approaches. The first approach is based on a well-established 3D electromagnetic quasi-static solver, ANSYS Q3D Extractor. For the second approach, a numerical solver based on the Partial Element Equivalent Circuit (PEEC) method is developed and assessed in terms of modelling accuracy required by fast switching WBG-based power converters. The PEEC method is presented as a promising numerical technique, which can potentially be used to overcome the limitations of the EM modeling based on the ANSYS Q3D Extractor.**

I. Introduction

Wide band-gap (WBG)-based power converters operate at higher switching frequencies and produce current and voltage waveforms with much faster slopes than Si-based power electronic systems. Therefore, small parasitic inductances and capacitances have a more severe impact on the electromagnetic (EM) behavior of WBG-based power converters. As the stray inductances seen from the device terminals have different impact on the switching properties of power converters, potentially hampering the utilization of WBG power semiconductor devices, it is highly useful to have the information on these inductances and minimize them in an optimal design. EM-circuit coupled, i.e. multi-physics, modeling enables the optimization of package layouts and interconnections before fabricating actual power modules. The circuit modelling is related to the development of compact device models, while the EM modelling of the power semiconductor packages is closely related to the procedures for the extraction of parasitics in electrical circuits. The accuracy and limitations of present numerical techniques for three-dimensional (3D) electromagnetic modeling of power modules are not well explored in literature. First, the capability of the ANSYS Q3D Extractor, a well-established 3D EM modelling tool used to estimate the parasitics within power semiconductor packages, is comprehensively analyzed in terms of accuracy. Second, the Partial Element Equivalent Circuit (PEEC) method is presented as a promising numerical technique for 3D EM-circuit coupled modeling for future power electronics.

II. Modelling for Package Parasitic Prediction

Electromagnetic modelling relies on numerical techniques used to solve Maxwell's equations in terms of unknown electric and magnetic field distributions and/or current and charge distributions in space. The selection of a numerical technique mainly depends on the application and, hence, only relative (dis)advantages of the specific method can be discussed. In this paper, the limitations of the existing modeling approach implemented in ANSYS Q3D Extractor for an accurate extraction of parasitics within WBG power modules are described. Then, the Partial Element Equivalent Circuit (PEEC) method is introduced as a promising numerical technique that can be used to overcome these limitations. In this section, the physical background of the Q3D-based modeling and PEEC-based modelling is described in order to provide a better understanding of the modelling challenges coming along with these two numerical solvers.

A. ANSYS Q3D Extractor

The well-known ANSYS tool, Q3D Extractor, has frequently been used for the extraction of parasitics by power electronics engineers both in academia and industry. Additionally, ANSYS provides the EM-circuit-coupled modeling capability using Q3D and the ANSYS Simplorer circuit simulator. The power of the ANSYS Q3D Extractor in comparison to other commercial 3D quasi-static EM solvers used for EM compatibility analysis of power electronics systems is its capability to directly extract the stray inductances, parasitic capacitances and resistances. Furthermore, ANSYS Q3D calculates the mutual inductive couplings between current paths and the capacitive couplings of conductive areas inside of packages. The Q3D Extractor is based on two numerical techniques: the Finite Element Method (FEM) and the Method

of Moments (MoM). The modelling is based on dividing the solution in two parts, the low frequency (dc, $f<f_{\mathrm{dc}}$) and high frequency (ac, $f>f_{\mathrm{ac}}$). For the dc solution, a uniform current distribution across the cross sections of conductors is assumed and modelled using the FEM, i.e. skin depth higher than the conductor thickness. For the ac solution, the assumption that the skin-effect is fully developed, i.e. skin depth $\approx$ three times smaller than the conductor thickness, and the currents are distributed only on the surface of conductors, is exploited using MoM, which leads to the ac resistances increasing as $\sqrt{f}$. In the mid-frequency range ($f_{\mathrm{dc}}<f<f_{\mathrm{ac}}$), the resistance and inductance are approximated based on the dc and ac solutions.

The parasitic extraction in Q3D is based on placing the equi-potential surfaces, referred to $source$ and $sink$ contacts, defining the current paths. When calculating the commutation loop inductance of power modules, $L_{\sigma,\mathrm{loop}}$ in Q3D, the semiconductor devices have to be modeled as conductive blocks, e.g. typically copper blocks, in order to simulate the current path. On the other hand, for the calculation of the distributed commutation loop inductance in Q3D, i.e. $L_{\sigma,\mathrm{loop}}=\sum_{ij} L_{\mathrm{p},ij}$, the actual current loop has to be divided into partial current segments ($L_{\mathrm{p},i}$) by removing the 3D models of the devices and setting up the corresponding $source$ and $sink$ contacts. As these contacts are equi-potential, the cut current path approximates the actual current path accurately to some extent, which mainly depends on the modelled geometry, as shown in [1].

B. A quasi-static PEEC solver

The PEEC method was introduced in the 1970s, and since then, different formulations have been developed: quasi-static and full-wave formulations, formulations for including electric and/or magnetic field effects, and dielectric and/or magnetic material properties [2]. The PEEC method provides a circuit interpretation of the Maxwell's equations in terms of partial elements, namely resistances, partial inductances and coefficients of potential. The resulting equivalent circuit can be then analyzed in both time and frequency domain in a circuit environment such as SPICE-like circuit solvers. In the frequency range of interest for modern PE applications (from kHz to GHz range), the current has to be represented as a 3D vector in order to accurately capture the skin and proximity effects, which can significantly increase the number of unknowns, and thus, the computational cost of the PEEC method. Exactly this has been an obstacle for exploiting the PEEC modeling in a wide range of PE applications. Therefore, most efforts today are directed towards an acceleration of the PEEC solvers in order to allow the analysis of more complex circuits in a wide-frequency range [3], [4]. In power electronic applications, there is a strong requirement to simultaneously take into account Ohmic losses (R matrix), as well as magnetic (L matrix) and electric (P matrix) field effects within a unique modeling environment. A PEEC-based tool for multi-physics modeling, which can take into account all design aspects (resistive, inductive, capacitive, and additionally thermal) is still under research [5], [6]. The advantage of the PEEC method for 3D EM modeling of power modules has been described in literature [7], [8]; however, a detailed verification of PEEC solvers for 3D EM modeling of power modules in terms of accuracy is missing, particularly the impact of the PEEC mesh and modeling of non-orthogonal geometries, e.g. bond-wires. This paper summarizes for the first time the required conditions for accurate and computationally efficient PEEC modeling of power semiconductor packages using a (R, L, P) PEEC solver.

III. Modeling Results and Verification

The first results are demonstrated for a $1.2\,\mathrm{kV}$ $80\,\mathrm{m\Omega}$ SiC power MOSFET in TO-247-3 package (C2M0080120D). Fig. 1 and 2 describe the corresponding 3D PEEC-modeling. A non-uniform PEEC mesh (number of unknowns $n_{\mathrm{sys}} = n_{\mathrm{edges}} + n_{\mathrm{nodes}} = 14896 + 2325 = 17221$) is applied to discretize the TO-247-3 package. For the modelling the drain-source (D-S) current path, the package can be represented with 4 pins corresponding to drain and source package terminals and the internal drain and source contacts for the die, as shown on Fig. 2. The size of the extracted 4-pins PEEC system (17221×17221) can be further reduced to e.g. a (576×576) system by applying a Model Order Reduction (MOR) technique [9], which enables to calculate both transient and frequency response of the package in a circuit domain at a lower computational cost. Further improvements of the PEEC-MOR solver with respect to the required memory storage and computational speed could be achieved as suggested in e.g. [10]. The modeling methods are verified by the D-S impedance, Z_{DS}-Θ_{DS}, measurements using a Keysight Impedance Analyzer E4990 ($20\,\mathrm{Hz}$-$120\,\mathrm{MHz}$). The high frequency (HF) D-S loop inductance $L_{\mathrm{DS,loop}}$ (relevant in the switching transients) is calculated from the measured Z_{DS}-Θ_{DS} for the MOSFET switched on and off, as described in [1]. In comparison to Q3D, the PEEC $L_{\mathrm{DS,loop}}$ perfectly matches the loop inductance calculated from the extracted partial inductances $\sum_{ij} L_{\mathrm{p},ij}$ as shown in Fig. 3. The internal node was placed at the central position of the die. As the modelled geometry cannot fully replicate the actual geometry since the shape of the bond wires is only approximated, a mismatch of less than 8% between the measured and modelled $L_{\mathrm{DS,loop}}$ is present. From Fig. 3 and Table I, it can be further concluded that the accuracy of Q3D is similar to the accuracy of the PEEC solver for modelling the D-S loop inductance of a TO-247-3 package in the frequency range up to $50\,\mathrm{MHz}$. However, in comparison to the PEEC method, Q3D Extractor introduces an error for the estimation of partial inductances and does not include the parasitic self-capacitance of the current path, which can become influential at higher frequencies, i.e. above several hundred MHz.

A similar comparison was performed for a 3^{rd}-Gen $1.2\,\mathrm{kV}$ $75\,\mathrm{m\Omega}$ SiC power MOSFET in four-lead TO-247-4 package (C3M0075120K), as shown in Fig. 4. As previously described, the prediction of the partial package inductances is performed without and with cutting the current path using the PEEC

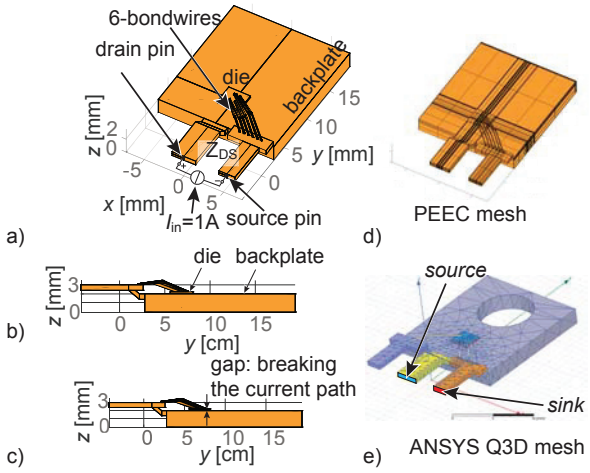

Fig. 1. 3D PEEC model of a TO-247-3 package for the estimation of L_{DS}: a) 3D structure before meshing, b) a YZ view showing the PEEC modeling without, and c) with breaking the loop into two current paths to extract drain and source inductances, d) non-uniform PEEC mesh, and e) ANSYS Q3D mesh.

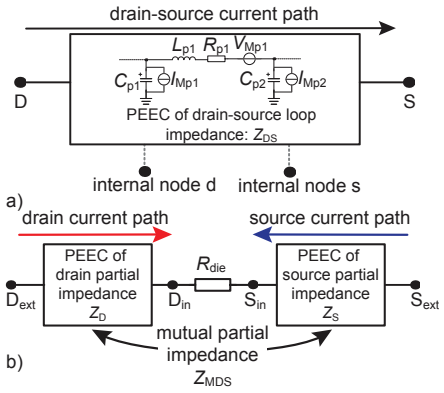

Fig. 2. PEEC modeling of Z_{DS} and constituting partial impedances: a) without, see Fig. 1b, and b) with, see Fig. 1c, breaking the current path. The PEEC method enables solving 3D PEEC models together with lumped circuit elements, which directly simplifies the coupling between the circuit and EM domains.

solver and Q3D Extractor, respectively. Two current loops, the D-S and D-Kelvin source (D-KS) loops are modelled and measured using the Keysight E4990 Impedance Analyzer. The results are summarized in Table II and illustrated for the D-S current loop example in Fig. 4. Here, it should be noted that the mismatch between the modelled and measured current loop inductances also comes from the limitation to fully accurately extract the actual shape and position of the

TABLE I
L_{DS} OF A TO-247-3 PACKAGE AT 50 MHz, WHERE THE MEASURED INDUCTANCE $L_{\mathrm{meas}} = 5.54$ nH.

L [nH]	L_{D}	L_{S}	M_{DS}	$L_{\mathrm{tot,eq}} = \sum L_{\mathrm{partial}}$	L_{tot}
Q3D	3.53	5.39	-1.58	5.76	5.98
PEEC	4.06	5.37	-2.0	5.42	5.42

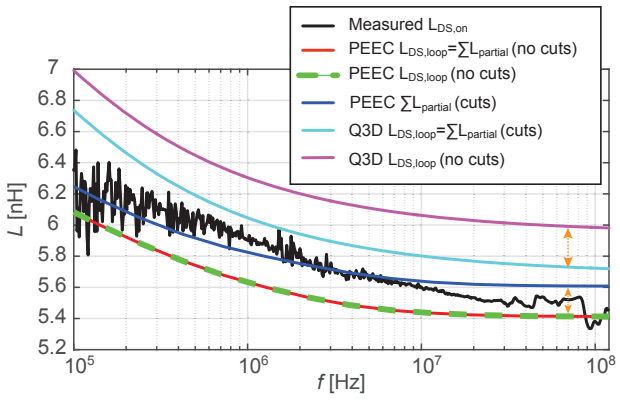

Fig. 3. Verification of PEEC and Q3D modelling of TO-247-3 package for the configurations with and without cutting the current path. The errors introduced by dividing the current path into sub-paths to extract partial inductances are marked.

TABLE II
$L_{\mathrm{D-S}}$ AND $L_{\mathrm{D-SK}}$ OF A TO-247-4 PACKAGE AT 10 MHz.

L [nH]	L_{S}	L_{D}	M_{DS}	$L_{\mathrm{tot,eq}} = \sum L_{\mathrm{partial}}$	L_{tot}
Drain-Source current loop: $L_{\mathrm{D-S,meas}} = 8.16$ nH					
Q3D	5.58	5.55	-1.56	8.00	8.45
PEEC	6.61	6.23	-2.43	7.98	7.98
Drain-Kelvin Source current loop: $L_{\mathrm{D-KS,meas}} = 11.32$ nH					
Q3D	6.93	5.55	-1.08	10.33	11.47
PEEC	8.178	6.23	-1.18	10.86	10.86

bond wires. Therefore, in Q3D, the loop inductance calculated from the partial inductances, $L_{\mathrm{tot,eq}} = \sum L_{\mathrm{partial}}$, is different from the total loop inductance calculated without breaking the loop into the current segments L_{tot}. However, L_{tot} represents the actual current path more accurately. This difference depends on the loop geometry and the definition of Q3D *source* and *sink* equipotential ports. With certain surface areas of the equipotential ports, $L_{\mathrm{tot,eq}}$ can be equal to L_{tot} at high frequencies ($f > f_{\mathrm{ac}}$); however, finding such areas is not straightforward. This is further demonstrated on an *all-SiC* half-bridge(HB) power module with planar interconnections.

The *all-SiC* half-bridge power module based the planar interconnection technology and the corresponding PEEC model are shown in Fig. 5a-b. In order to measure the low-inductance loop between DC+ and DC- ($L_{\mathrm{DC+,DC-}}$) without the contribution of the bus-bars, the Keysight E4990 Impedance analyzer with a 42941 impedance adapter and a pin probe was used. The comparison between the PEEC-based, Q3D results and the measurements of $L_{\mathrm{DC+,DC-}}$ is shown in Fig. 5d and Table III and IV. Here, a difference between the modelled and measured $L_{\mathrm{DC+,DC-}}$ is due to a difficulty to accurately represent the excitation points, DC+ and DC-, marked in Fig. 5a.

IV. Conclusion

This paper presents the EM modelling of power semiconductor packages using the well-established ANSYS Q3D

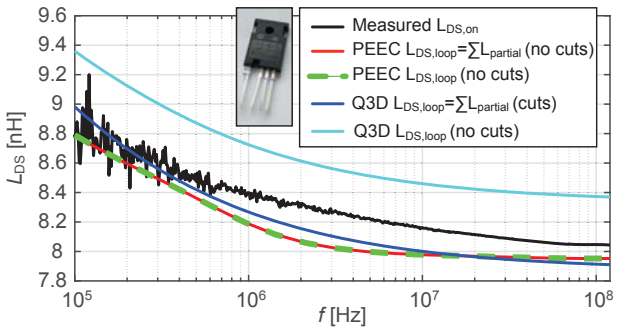

Fig. 4. Verification of PEEC and Q3D modelling of TO-247-4 package for the configurations with and without cutting the current path. The number of unknowns $n_{\text{sys}} = n_{\text{edges}} + n_{\text{nodes}} = 9960 + 1988 = 11948$.

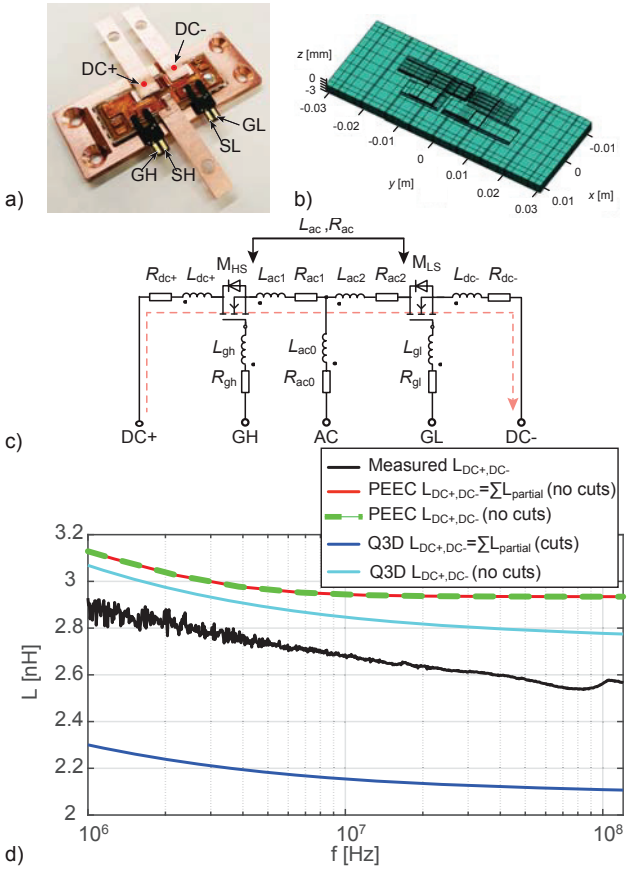

Fig. 5. *All-SiC* HB power module package: a) a photo, b) the PEEC mesh with $n_{\text{sys}} = n_{\text{edges}} + n_{\text{nodes}} = 26256 + 4411 = 30667$ unknowns, c) the equivalent circuit, and d) the verification of PEEC and Q3D modelling for the configurations with and without cutting the current path.

Extractor tool, and a self-developed quasi-static (R, L, P) PEEC-based solver. The verification of both modelling approaches are verified using the examples of two TO-247 packages and an *all-SiC* half-bridge power module. Analyzing the modelling challenges and limitations of two modelling tools, the PEEC method is shown to be a promising numerical technique enabling a more accurate prediction of package parasitics, and additionally, allowing EM-circuit coupled modelling in a wide-frequency range. However, further improvements of the PEEC method with respect to computational speed and memory requirements are required in the future.

TABLE III
$L_{\text{DC+,DC-}}$ OF THE *all-SiC* HB POWER MODULE AT 10 MHz, THE MEASURED INDUCTANCE $L_{\text{DC+,DC-,meas}} = 2.69$ nH.

L [nH]	$L_{\text{tot,eq}} = \sum L_{\text{partial}}$	L_{tot}	rel.diff
Q3D	2.12	2.84	-25 %
PEEC	2.94	2.94	0 %

TABLE IV
PARTIAL INDUCTANCES OF THE *all-SiC* HB POWER MODULE AT 10 MHz.

L [nH]	$L_{\text{dc+}}$	L_{ac}	$L_{\text{dc-}}$	$L_{\text{dc+,ac}}$	$L_{\text{dc+,dc-}}$	$L_{\text{ac,dc-}}$
Q3D	0.80	1.51	0.88	-0.219	-0.187	-0.127
PEEC	1.08	2.09	1.89	-0.207	-0.461	-0.397

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