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Time-Resolved Short Circuit Failure Analysis of SiC MOSFETs

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***Abstract*—High-speed optical imaging is used in conjunction with fast electrical measurements to advance the understanding of the development of short circuit failures in silicon carbide power MOSFETs. Special samples are manufactured, which are compatible and comparable to TO-247 packages, but do not have any encapsulation. This allows optical observation of die surface during the test. The information on visible processes on the die allows for a better understanding of the sequence of events leading up to a failure. Imagery of destructive drain-source failures is also obtained, as well as post-failure images of surface and cross-sections. Aluminum metal melting is observed even for very short tests, before electrical indications of damage. The onset and completion of melting are used as information on the temperature of the die surface. Using this data for calibration, a detailed electro-thermal model is then used to simulate the temperature distribution and evolution during the short circuit.**

I. Introduction

Silicon carbide (SiC) MOSFETs offer fast switching of high voltages with high efficiency, leading to smaller and cheaper converters. In the event of a short circuit, the high power density quickly leads to extreme temperatures. This rapid heating above $1000\,^{\circ}\mathrm{C}$ leads to an often catastrophic failure within less than $10\,\mu\mathrm{s}$ at typical operating voltages [1]. It also makes understanding the process difficult, as any measurement needs to be very fast. Simulation is doubly difficult, as neither high temperature material parameters nor the temperatures reached are known. As short circuit behavior is a critical device characteristic in some applications, precise knowledge of the process is desired. This is necessary not only for optimizing device design and improving the robustness of future devices, but also for implementing protection features and diagnosing possible device damage. Electrical measurements of SC testing and simulation of the process have been shown by several authors [2]–[7]. The suspected failure mode is hot-spot formation with local thermal runaway as cause of drain-source failures. There is some uncertainty about the occurring temperatures and the sequence of events, also due to use of low temperature material parameters and simplified models. IR thermography can give an insight into surface temperature distribution, but slow cameras necessitate low V_{DS} and use of equivalent time sampling across many devices [2], [3], [8].

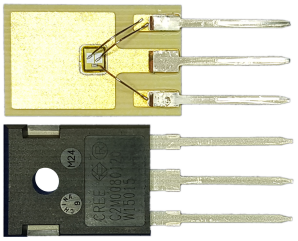


Fig. 1. Finished sample with DCB, die, bond wires and leads, side by side with a commercial TO-247 packaged device housing the same die.

II. Approach

During short-circuit, a high-speed camera is used to record the visible processes on the die. This allows imaging the sequence of events during a single test and correlating it with the electrical data for this specific test and device. High frame rates even allow observing highly dynamic tests at $V_{\mathrm{DS}} = 800\,\mathrm{V}$. After the test, optical and electrical analysis as well as imaging of cross-sections is performed. Simulation is used to further investigate the failure process.

A. Test setup

The short circuit test setup consists of a low inductive capacitor bank, an array of auxiliary switches and a mounting space for the TO-247 DUTs. The gate driver and the measurement connections are placed as close as possible to the DUT. A $400\,\mathrm{MHz}$ shunt is used to measure the drain current I_{D}, $500\,\mathrm{MHz}$ voltage probes record V_{DS} and V_{GS}. Measurements are run at $10\,\mathrm{GS/s}$ and $10\,\mathrm{bit}$. I_{D} is recorded with two channels to get optimum resolution both before ($<300\,\mathrm{A}$) and during failure ($<3500\,\mathrm{A}$). High-speed images are taken at up to 2.1 million frames per second (FPS); lower speeds are used to improve image resolution. Using a macro lens, observation of the whole die or parts of it is possible.

B. Sample manufacturing

Cree 2nd generation $1200\,\mathrm{V}$, $80\,\mathrm{m\Omega}$ dice are soldered to TO-247 sized DCBs using SAC 305 solder paste. They are then wire-bonded using $300\,\mu\mathrm{m}$ aluminium wire, resulting in a $33\,\%$ larger cross-section of the source wires compared to the commercial devices. Finally, the samples are equipped with

TO-247 leads, see Fig. 1. The construction allows using the same characterization and test setups as for the commercially packaged devices with the same dice. The differences in construction and the lack of encapsulation can be shown not to result in different short circuit behavior, as the heating is confined to the die for the short duration of the test.

C. Sample verification

To verify the samples indeed behave the same as the commercial, TO-247-packaged equivalents, characterization and short-circuit tests are compared. IV-characterization after fabrication shows results equal to the reference devices. In all samples, the breakdown voltage in air is above 1000 V, confirming that encapsulation is not necessary for the tests. Nevertheless, some samples are covered with a clear conformal coating to observe the effect of an organic layer on top of the die. Several short circuit tests show that behavior before and during failure as well as short-circuit withstand time (SCWT) are equivalent for all devices.

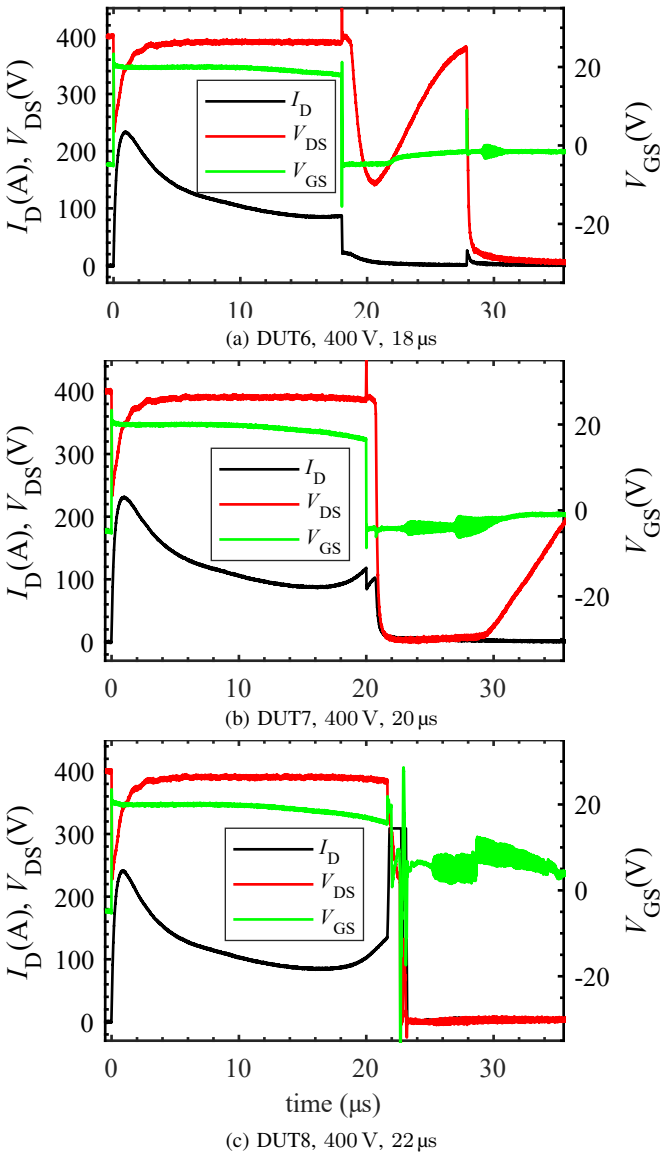
III. Testing

A. Electrical measurement

Short circuit tests of 19 samples plus reference devices are run at V_{DS} = 400 V and V_{DS} = 800 V. At 400 V, gate damage is observed starting around 14 µs SC duration, becoming stronger with SC duration. At 18 µs there is significant gate leakage, but delayed drain-source failure has also been observed in Fig. 2a. Up to 20 µs however, the device often does not experience drain-source failure, see Fig. 2b. At 22 µs, drain-source breakdown is likely to occur before turn-off and the current quickly rises beyond 1 kA, see Fig. 2c. Packaged devices are usually destroyed at this point. At 800 V, the curves are very similar, but gate damage happens from 3.5 µs and failures occur already at 4.5 µs.

B. High-speed imaging

For all non-encapsulated samples, high speed camera footage is obtained, which can be compared to the electrical measurement for each test. All surface events can be seen, which includes the progression of melting of the top metalization and the explosive failure if drain-source breakdown occurs. Fig. 3 and 4 show the same tests as Fig. 2 b and c, respectively. The onset of melting (Fig. 3b) is visible as small change in surface structure, a liquid surface of the source pads (Fig. 3c) can be recognized from their dark appearance, as the light is reflected away from the camera. Further heating again results in a rougher surface (Fig. 3d) and bulging polyimide passivation. The surface then becomes so hot it appears white (Fig. 3e), around the time the power is turned off. After the test, the pads again appear black, as the metal re-solidifies with a smooth surface (Fig. 3f). If a failure occurs, hot metal fragments immediately cover the surface of the die (Fig. 4d) and rapidly expand outwards (Fig. 4e). To see more details of the failure instant, several tests are done without lighting and reduced aperture, but the brightness of the hot metal is



(a) DUT6, 400 V, 18 µs

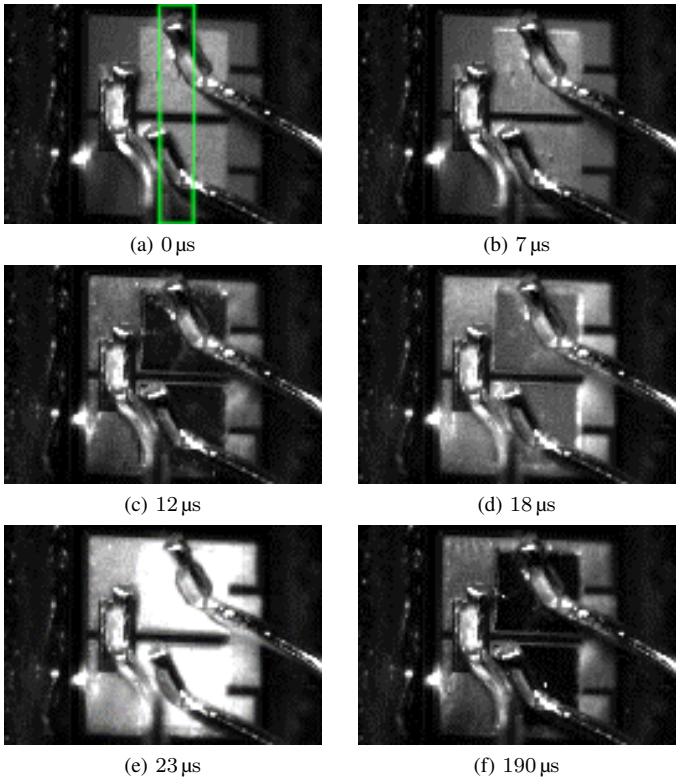
(b) DUT7, 400 V, 20 µs

(c) DUT8, 400 V, 22 µs

Fig. 2. Electrical measurements of SC tests at 400 V with progressively longer duration. After a peak of 240 A, the current decreases, then starts to rise again. (a) shows successful turn-off, gate damage and, unusually, delayed failure without current. (b) shows partial turn-off, the auxiliary switch then interrupts the current and V_{DS} rises, indicating intact drain-source isolation but damaged gate. (c) shows gate damage and drain-source failure with high current (clipped at 300 A).

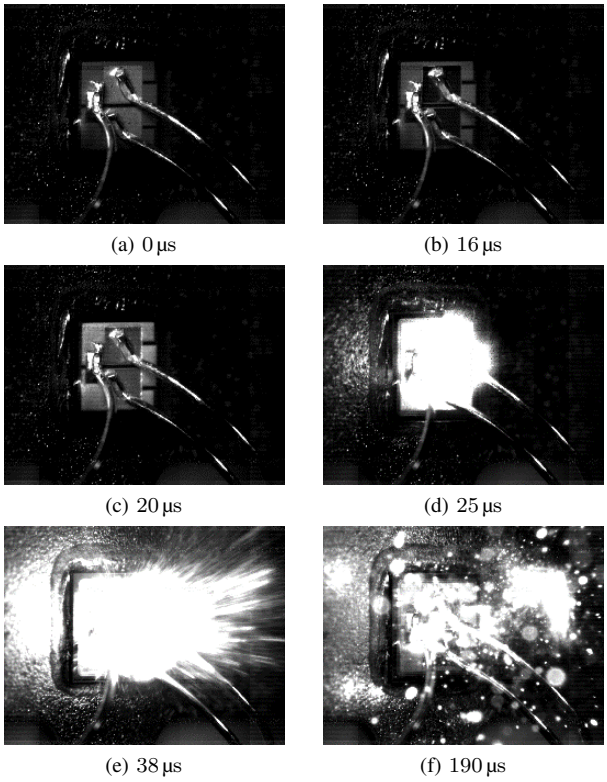
so high that the localized origin of the failure is immediately overexposed.

To accurately capture the melting process and allow conclusions on the surface temperature over time, additional tests are conducted with the maximum possible frame rate, imaging a small section of the source pads. Fig. 5 and 6 show the results for 400 V and 800 V, respectively. For 400 V, the onset of melting is found at 5.7 µs, when the first significant change in brightness is measured on the source pad. After 12.4 µs, the surface appears dark, as it is smooth and reflects the light away from the camera, indicating it has completely melted. For 800 V, the same is observed at 2.4 µs and 8.6 µs.



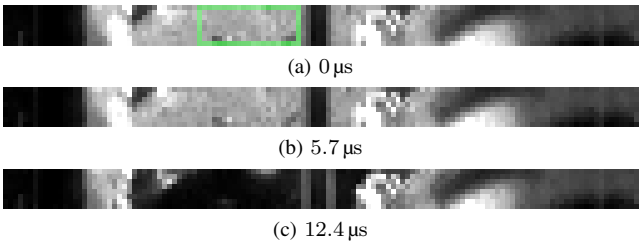
(a) 0 µs (b) 7 µs (c) 12 µs (d) 18 µs (e) 23 µs (f) 190 µs

Fig. 3. Images of DUT7 during a test at 400 V for 20 µs, 450 kFPS, corresponds to Fig 2b. (a): beginning of test. Marked area is shown in Fig. 5 and 6. (b): pad surface starts melting. (c): surface is molten. (d): Surface begins to bulge. (e): rough surface, a few small Al fragments are ejected. (f): Ejection has stopped.



(a) 0 µs (b) 16 µs (c) 20 µs (d) 25 µs (e) 38 µs (f) 190 µs

Fig. 4. Images of DUT8 during a test at 400 V for 22 µs, 225 kFPS, corresponds to Fig 2c. (a): beginning of test. (b): pad surface is molten. (c): surface is bulging. (d): explosive failure starts. (e): Current is off, Al fragments are ejected. (f): Ejection has stopped, one bond wire is loose.



(a) 0 µs (b) 5.7 µs (c) 12.4 µs

Fig. 5. Images of DUT9 tested at 400 V for 10 µs, 2100 kFPS. Source pads and bond wires shown, see Fig. 3a. Brightness measurement on marked source pad area. (a): beginning of test, brightness 65.2 %. (b): pad surface starts melting, brightness 63.3 %. (c): surface is smooth and reflective, brightness 7.0 %.

C. Post mortem analysis

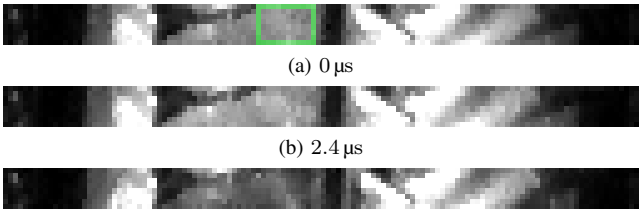
After the tests, the pad surfaces are found to be smooth and highly reflective, as can be seen in Fig. 7. If explosive failure occurred, a localized crater measuring some 100 µm is found (Fig. 7d,e). Typically, the crater forms under or close to a bond wire, detaching it from the pad. Cross-sectioning of such a crater as seen in Fig. 8 shows a depth of 70 µm, exposing the highly doped substrate under the ∼17 µm thick active layers.

IV. Simulation

A detailed 2D structure of the MOSFET's active cell is generated, including over-layers of dielectrics and 4 µm source aluminum layer, which is necessary for accurate electro-thermal (ET) simulations. 2D ET simulations are done in Sentaurus Device using the "Thermodynamic" model, full anisotropy and temperature dependence of thermal material properties. Aluminum melting (933 K) is accounted for by increasing its heat capacity at higher temperatures. The simulation results can be compared to measurements and observation of the beginning of melting, see Fig. 9. The simulated melting of aluminium begins at 5.97 µs, closely matching the 5.7 µs observed in Fig. 5b. The same is true at 800 V, with 2.48 µs matching 2.4 µs from Fig. 6b. This validates the temperature simulation, which further shows above 1400 K at the time of drain-source failure. The difference between simulation and measurement close to failure can be explained by deficiencies in the the pn-junction leakage model, as well as individual cells deviating from simulated average behavior.

V. Conclusion

High-speed optical images allow determination of surface events affecting the source metal. The combination of optical imaging and electrical measurements, both during and after the test, shows when which damage occurs. At 400 V, the source metal begins melting at 5.7 µs, it is completely molten at 12 µs and material is ejected at 23 µs. At 800 V, the aluminium melts earlier, starting at 2.4 µs. If the short-circuit is maintained, an explosive drain-source failure, accompanied by very high currents, will occur. Permanent drain-source failure can also

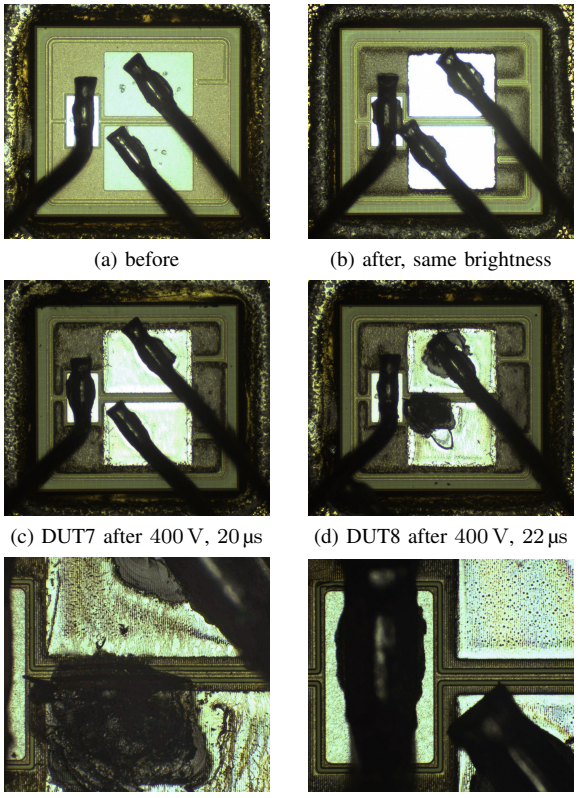


(a) 0 µs

(b) 2.4 µs

(c) 8.6 µs

Fig. 6. Images of DUT14 tested at 800 V for 3.5 µs, 2100 kFPS. Source pads and bond wires shown, see Fig. 3a. Brightness measurement on marked source pad area. (a): beginning of test, 55.9 % brightness. (b): pad surface starts melting, peak brightness at 61.6 %. (c): surface is smooth and reflective, remains this way permanently, brightness 33.9 %.



(a) before (b) after, same brightness

(c) DUT7 after 400 V, 20 µs (d) DUT8 after 400 V, 22 µs

(e) closeup of (d) (f) closeup of pads

Fig. 7. (a) shows a device before testing. (b) shows the high reflectivity of the source pads after melting, the images below are taken at lower brightness. (c) and (d) show reflective, uneven metal surface, with (d) also exhibiting an explosion crater. (e) shows more closely the crater on (d), while (f) shows the surface features of source (melted) and gate (not melted) pads.

occur with delay, triggered not by active current and heating but by heat spreading to sensitive regions. This failure creates a localized, highly conductive path between substrate (drain) and top metalization (source). The failure location is visible as bright spot on the die; it cannot be determined if molten metal or plasma in the form of an electrical arc create the conductive path. If catastrophic failure does not occur, the devices sustain gate damage, but retain drain-source isolation. A detailed simulation matches the observed timing of the metal melting and shows the temperature of an average cell at failure reaches 1400 K.

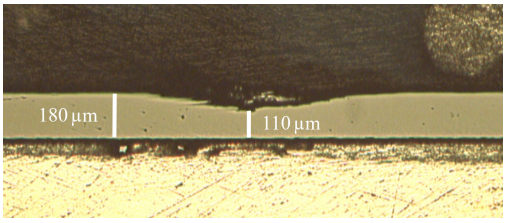


Fig. 8. Cross-section through the crater shown in Fig. 7(e). The die is in the center, with solder and DCB below. The crater is 70 µm deep, allowing current flow from source metal to substrate.

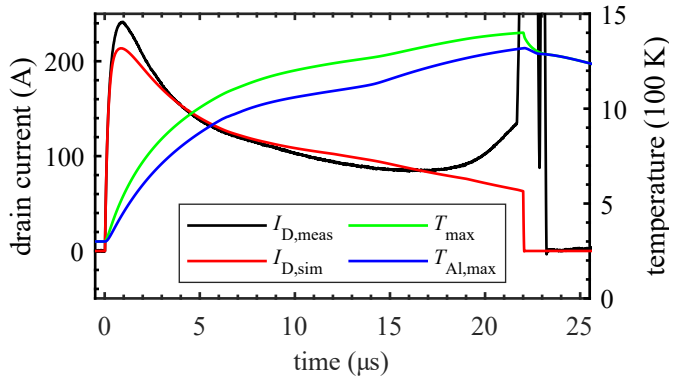


Fig. 9. Simulation of SC in the investigated MOSFET at 400 V. The maximum temperature in the aluminium reaches melting point at the time observed in Fig. 5b. At failure, the temperature of an average cell reaches 1400 K.

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