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Low-Noise InP High Electron Mobility Transistors

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presented by

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This thesis is dedicated to my son Stefan. Becoming a mother made me realize that I can do almost anything one-handed…even finish writing this thesis.

A Mother's Wisdom
Sleep when the baby sleeps.
Write the PhD thesis when the baby writes the PhD thesis.

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ABSTRACT

Indium phosphide high electron mobility transistors (InP HEMTs) represent the state-of-the-art technology for both room and cryogenic temperature low noise amplifiers. For years they have been playing a central role in the most demanding niche applications such as radio astronomy and deep space communications, and they are expected to significantly contribute to communication networks of the future. Modern lithography tools have enabled straightforward processing of transistors with sub-100 nm gate lengths, however, the improved RF performance did not result in the expected advancement of noise behavior. The physical limits of noise performance are currently motivating research into this subject, with indications that a significant decrease of minimum noise figure from reducing the gate length cannot be expected. Nevertheless, there is room for improvement in transistor noise behavior with further development of epitaxial growths and bandgap engineering.

This work centers on the optimization of InP HEMTs epitaxial layers by bandgap engineering, small-signal modeling and characterization. A common approach in improving carrier confinement and mobility with narrow bandgap materials used for the channel results in impact ionization taking place even at a relatively low drain bias. The small-signal model was extended to account for the effects of impact ionization and now features excellent agreement between simulated and measured S-parameters at lower frequencies at both room and cryogenic temperatures: we are now able to resolve in which material impact ionization takes place in a composite channel. The noise model proposed in this work including the impact ionization effects shows good agreement with noise measurements performed at room temperature. Achieving the best possible transistor gain and noise behavior depends highly on the quality of contacts: epitaxial structures were therefore optimized in order to reduce contact resistance and improve channel transport properties. Composite channel structures with narrow and wide bandgap materials were implemented to reduce the effects of impact ionization. Further refining of the channel layers in combination with vertical device scaling should allow improvement of both the device bandwidth and minimum noise figure.

ZUSAMMENFASSUNG

Indiumphosphid-HEMTs (Feldeffekt-Transistoren, in deren Kanal Elektronen mit sehr hoher Beweglichkeit auf elektrische Felder reagieren) repräsentieren sowohl bei normalen als auch extrem tiefen Arbeitstemperaturen den Stand der Technik aktiver Bauelemente für rauscharme Verstärker. Seit Jahren spielen diese Komponenten eine zentrale Rolle bei anspruchsvollsten Nischenanwendungen, beispielsweise in der Radioastronomie oder Deep-Space Kommunikation. Weiterhin wird ein wesentlicher Beitrag dieser Komponenten für künftige leistungsfähigere Kommunikationsnetze erwartet. Moderne lithographische Methoden erlauben die unkomplizierte Herstellung von Halbleitern mit Gate-Längen von weniger als 100 nm, wobei die verbesserten Eigenschaften bei höchsten Frequenzen keinesfalls das erwartete verbesserte Rauschverhalten beinhalten. Die physikalischen Grenzen des Rauschverhaltens sind gegenwärtig Gegenstand der Forschung, mit der daraus resultierenden Erkenntnis, dass eine Reduzierung der minimalen Rauschzahl durch Reduktion der Gate-Länge nicht erwartet werden kann. Dennoch bestehen Möglichkeiten der Verbesserung des Rauschverhaltens dieser Transistoren mittels Weiterentwicklung der Epitaxie und sogenanntes Bandgap-Engineering.

Diese Arbeit beinhaltet im Wesentlichen die Optimierung der epitaktischen Schichten von Indiumphosphid-HEMTs durch Bandgap-Engineering, der Erstellung von Kleinsignal-Modellen resultierender Transistoren und deren weitergehende Charakterisierung. Eine allgemein gebräuchliche Methode zur Verbesserung der Eingrenzung und Beweglichkeit der Ladungsträger durch Verwendung von Materialien mit schmaler Bandlücke innerhalb des Kanals ergibt Stossionisationsprozesse bei relativ niedrigen Drainspannungen. Das Kleinsignalmodell wurde um die Darstellung der durch Stossionisation bedingten Effekte erweitert und ermöglicht nun eine hervorragende Übereinstimmung zwischen simulierten und gemessenen S-Parametern bei niedrigen Frequenzen und sowohl kryogenen Bedingungen als auch bei Raumtemperatur. Wir können deshalb nun unterscheiden, in welchem Material innerhalb eines aus mehreren Materialien zusammengesetzten Kanals Stossionisation stattfindet. Bei Raumtemperatur vorgenommene Rauschmessungen zeigen gute Übereinstimmung mit dem die Effekte von Stossionisationspro-

zessen einschliessenden vorgeschlagenen Rauschmodell. Der höchstmögliche Gewinn eines Transistors und dessen bestmöglichstes Rauschverhalten hängt in hohem Masse von der Qualität seiner Kontakte ab. Deshalb wurden die epitaktischen Strukturen hinsichtlich der Reduktion des Kontaktwiderstands und der Transporteigenschaften des Kanals optimiert. Es wurden aus Materialien mit kleiner und grosser Bandlücke zusammengesetzte Kanäle implementiert, um die Effekte der Stossionisation zu reduzieren. Die Weiterentwicklung der Schichtstruktur des Kanals in Kombination mit einer vertikalen Skalierung der Transistoren sollte zu einer Verbesserung hinsichtlich minimal möglicher Rauschzahl und Bandbreite führen.

CONTENTS

1

INTRODUCTION

1.1 BACKGROUND

Data of interest in deep space communication networks and radio astronomy is carried by ultra low-power electromagnetic signals as a consequence of the astronomical distances between the signal source and the receiver. The exceptionally low amplitude of these signals, as low as $6.3 \cdot 10^{-19}$ W, often tends to make them indistinguishable from surrounding interference such as radiation emitted from other celestial objects or noise generated by the receiver itself. To be able use these extremely weak signals without significantly degrading them, special attention needs to be paid to the design of the low-noise receiver. The major bottleneck of the receiver is the first amplifying element in the signal path – Low Noise Amplfier (LNA). Besides amplification of the received signal, the LNA degrades total Signal-to-Noise Ratio (SNR) by the amount of its internally generated noise. For deep space missions, amount of science data returned to Earth is limited by capacity of the space-to-Earth network, with maximum downlink data rate determined by the receiver's SNR. As deep space missions often have limited amount of time to explore their targets, increasing the volume of returned data is a high priority considering both scientific and economical reasons. In the field of radio astronomy, the resolution of image acquired by the radio telescope highly depends on the noise contribution of the receiver, primarily on its first stage the LNA. By cryogenically cooling the LNA, thermal noise will be significantly reduced compared to the room temperature operation due to reduction in resistances and improved transport characteristics [1]. Therefore, with the cooled LNA, the receiver's SNR can be improved considerably, which is followed by the increase of the maximum transferable data rate or the enhanced radio image resolution. InP-based High Electron Mobility Transistors (HEMTs) as the key components of LNAs proved to be very attractive due to their superior channel transport properties such as high electron mobility and high saturation velocity at both room and cryogenic temperatures.

Since the invention of the first HEMT based on the AlGaAs/GaAs heterostructure [2], much effort was invested in improving the original design including modifications of the epitaxial layers and progresses in manufacturing technology. One of the first major steps was introduction of a thin GaInAs layer as the channel in AlGaAs/GaAs structure, improving electron transport, carrier confinement and allowing higher sheet charge density [3]. From there it did not take long to develop the first pseudomorphic $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As/InP$ HEMT [4], and a year later, the first HEMT with increased In content in the channel [5]. Introduced strain in previously lattice matched $Ga_{0.47}In_{0.53}As$ channel resulted in a decrease of the electron effective mass and a rise of the low field mobility followed by additional gain in terms of microwave performance. AlInAs/GaInAs/InP heterostructures excelled over previously used AlGaAs/GaInAs/GaAs due to higher conduction band discontinuity, enhanced transport properties and better carrier confinement, however at a cost of having lower breakdown voltage and more pronounced impact ionization effects. The advancements in bandgap engineering, further revisions of the AlInAs/GaInAs/InP layer structure, and reduction of the transistor parasitics by gate, source, and drain scaling made the InP-based HEMT a key component of today's high-speed, high-gain and low-noise applications such as THz transmitters, receivers, LNAs and frequency multipliers. Figure 1.1 shows the improvement of cut-off and maximum oscillation frequencies with the gate length scaling over the years for some benchmarked InP HEMTs.

Cryogenic noise performance of InP HEMTs has also made an immense progress in the last few decades, allowing construction of ultra low-noise amplifiers implemented as Hybrid Microwave Integrated Circuits (HMICs) or Monolithic Microwave Integrated Circuits (MMICs). Table 1.1 shows reported performance in terms of minimum noise temperature and gain per stage for today's state of the art cryogenic InP HEMT LNAs MMICs.

The present work indicates there is however a limit to the continuous improvement of InP HEMT capabilities, particularly regarding noise performance. While aggressive transistor scaling and increasing channel In content to the point where it consists of pure InAs can improve its bandwidth, transistor noise performance will suffer due to the Short-Channel Effects (SCEs), reduced quality of pinch-off and increased impact ionization in the channel. Assumption that an improvement in $f_{\max}$ under constant drain current should result in a corresponding improvement in minimum noise figure is

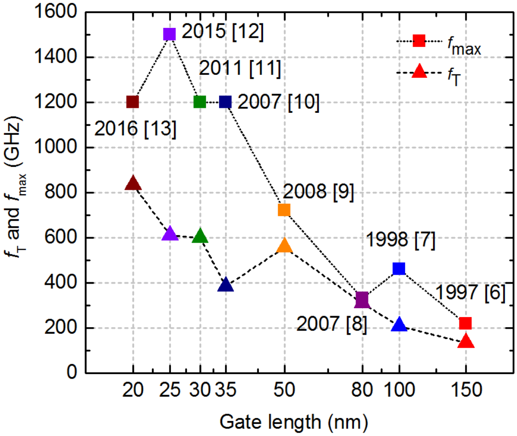

FIGURE 1.1: f_{max} and f_{T} increase with gate length reduction.

Freq. band (GHz)	T_{min} **(K)**	L_{g} **(nm)**	**Gain/stage (dB)**	**Year**
4-8[1]	1.4	130	14.7	2012 [14]
4.6-13.8	2.6	100	14	2017 [15]
24-40	7	100	9.7	2017 [16]
25.5-32.3[1]	9.8	100	8.3	2015 [17]
26-40	8	80	9	2012 [18]
28-52	6.7	100	8.5	2017 [16]
50-75	18	35	9	2017 [19]
65-116	18.6	100	6	2017 [20]
67-114	22	35	not reported	2017 [21]
70-100	23	35	not reported	2017 [21]
85-116	26	35	8.5	2017 [22]

TABLE 1.1: Overview of performance for today's state of the art cryogenic LNAs.

not valid for sub-100 nm gate lengths due to the large increase in drain noise countering the desired f_{max} enhancement [23]. Therefore, for HEMTs that

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[1] Implemented as HMIC

are to be utilized in low-noise applications a trade-off has to be made between further advances in RF performance and their influence on the minimum achievable noise figure.

1.2 SCOPE OF DISSERTATION

The aim of this work was to further improve transistor's noise performance, partly for the "Next Generation of Very Low Noise Cryogenic Amplifiers in K/Ka Band" project collaboration with *Centro Astronómico de Yebes* and *European Space Agency (ESA)*. The development of new generations of transistors included design and optimization of new epitaxial layers that were grown in ETH FIRST Laboratory, followed by the optimization of fabrication process and characterization.

This thesis is structured in the following way:

- **Chapter 2: Theory and Characterization Methods**

  This chapter focuses on the HEMT principle of operation, description of the main measurement systems with most important figures-of-merit, followed by basic transistor model and extraction methods.

- **Chapter 3: HEMT Fabrication**

  The first part of Chapter 3 describes the epitaxial layers used to fabricate transistors, and in the second part overview of the standard process flow is presented.

- **Chapter 4: Optimization of the HEMT Epitaxial Layer Structure**

  Chapter 4 describes several optimizations which were carried out in order to improve device performance together with comparison of DC, RF and noise measurement results.

- **Chapter 5: Conclusion and Outlook**

  The results achieved in the course of this work are discussed and summarized. Also, suggestions for future work are given.

2

THEORY AND CHARACTERIZATION METHODS

2.1 DEVICE STRUCTURE AND WORKING PRINCIPLE

2.1.1 *HEMT Heterostructure*

The working principle of a HEMT is based on the formation of a heterojunction between two semiconductor materials with different bandgaps [24]. Creation of a dense quasi two-dimensional sheet of electrons, localized at the interface between the two materials, results in an enhanced carrier mobility in this transistor type. InP based HEMTs, which are the focus of this work, have thin layers of lattice matched (or strained) AlInAs and GaInAs representing wide and narrow bandgap semiconductors that form a type I heterostructure. The energy band diagram of such system has discontinuities at the junction, as shown in figure 2.1, as a result of different electron affinities of two materials. If a wide bandgap AlInAs layer is *n*-doped, electron diffusion occurs across the heterointerface leading to a build-up of electrons in GaInAs, and to a depleted zone in AlInAs. The conduction band discontinuity (ΔE_C) on the AlInAs side of the junction serves as a barrier which separates majority carriers electrons accumulated in GaInAs and remained ionized donors in AlInAs. Together with the resulting conduction band edge on the GaInAs side, the potential barrier forms a quantum well along the boundary of two materials where large number of electrons is confined.

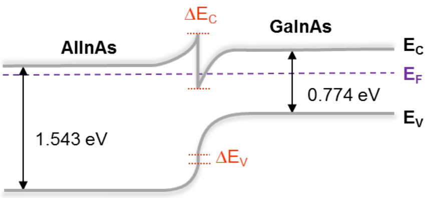


FIGURE 2.1: Schematic band diagram of a type I heterojunction consisting of two semiconductors with different bandgaps.

Electrons confined in the GaInAs quantum well are only free to move in a quasi two-dimensional plane which is parallel to the heterointerface forming a Two-Dimensional Electron Gas (2DEG). The energy of electrons is quantized in direction perpendicular to the heterointerface. Current flowing through a HEMT 2DEG channel will be a function of 2DEG sheet carrier density, n_s, and electron mobility, μ_n. To achieve good transport properties and high electron density in the 2DEG, the semiconductor forming the quantum well should have a narrow bandgap with low electron effective mass such as In-rich GaInAs or pure InAs. Figure 2.2 represents a typical InP HEMT heterostructure along with the corresponding conduction band diagram. It utilizes two AlInAs/GaInAs heterointerfaces to confine the electrons between two potential barriers.

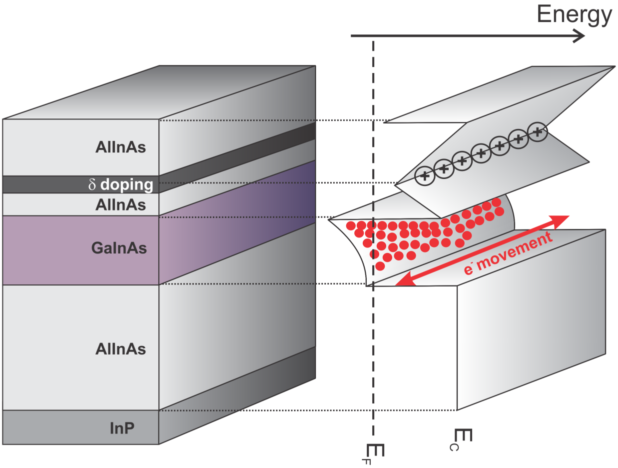


FIGURE 2.2: Schematic of a typical InP HEMT heterostructure together with conduction band diagram in thermal equilibrium.

Doping of top AlInAs layer is done with a thin layer of Si donor atoms, referred to as δ-doping. As a result of separating free electrons from their donors with the potential barrier, impurity scattering is reduced and the mobility of electrons is enhanced, justifying the name of these transistors. At cryogenic temperatures, where impurity and alloy scattering are two dominating scattering mechanisms [25], separation of carriers and donors leads to further increase of the channel mobility and decrease of the channel sheet resistance. Consequently, the transistor exhibits higher gain and overall better noise behavior, thus motivating the study of cryogenically cooled LNAs based on InP HEMTs.

2.1.2 *Principle of Operation*

Figure 2.3 shows the cross-section of the InP HEMT structures processed in this work, with a T-shaped gate contact placed between two annealed Ohmic source and drain contacts. Besides the layers forming a heterostructure, as described in figure 2.2, fabricated devices also have a thin InP etch-stop layer. A good HEMT device also requires a highly n-doped GaInAs capping layer in order to allow low resistance source and drain Ohmic contact formation. Source and drain contacts are placed directly on the GaInAs layer, while the cap has to be removed underneath the gate to allow the formation of the gate Schottky contact. In the growth direction, the full HEMT structure as described in figure 2.3 consists of an AlInAs buffer layer, a GaInAs or composite channel layer, an AlInAs spacer, a δ-doped Si plane, an AlInAs Schottky barrier, an InP etch stop and a highly-doped GaInAs (or composite GaInAs/AlInAs) cap layer.

The operational principle of a HEMT shown in figure 2.3 is as follows: voltage applied at the gate contact modulates the amount of electrons in the 2DEG which participate in current transport, while source and drain contacts drive those electrons through the GaInAs channel. A majority of electrons tunnel from the annealed source and drain contacts directly to the channel to contribute to the current. However, a fraction of electrons flows through the highly-doped cap layer and subsequently tunnels through the barrier layer to the channel thereby effectively making the cap layer serve as an extension of the metal contacts. By applying a negative voltage at the gate, the 2DEG underneath the contact is depleted and the current through the channel, driven by the drain-source voltage, is small. By applying a more positive voltage at the gate, the sheet density of the 2DEG, as well as the current, is increased. For large forward gate bias, the current will saturate and the channel is said to be fully open. Further increase of the forward gate bias leads to a formation of a parasitic parallel channel in the barrier layer which is an undesirable effect leading to diminished transistor control and worse noise behavior.

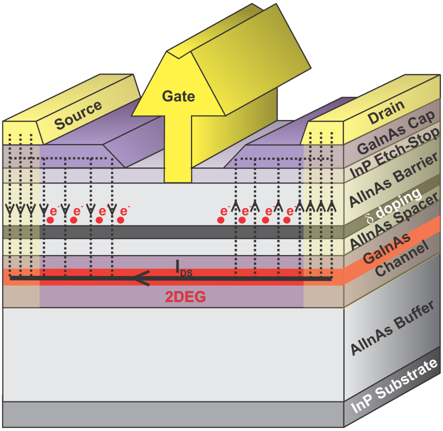


FIGURE 2.3: Cross-section of the InP HEMT processed in this work with gate Schottky contact and annealed source and drain Ohmic contacts. Arrows depict the electron movement and the current direction throughout the structure.

2.2 DEVICE CHARACTERIZATION AND FIGURES-OF-MERIT

2.2.1 *Introduction*

There are several measurements and figures-of-merit used to characterize InP HEMTs, most important being DC, RF and noise measurements at both room and cryogenic temperatures. While DC and RF characterizations are fairly straightforward, noise measurements invoke a complex procedure. Besides having several noise sources which are bias and temperature dependent, a single InP HEMT noise level is often as low as the measurement uncertainty, particularly at cryogenic temperatures. Noise characterization therefore requires a sophisticated measurement setup, very precise calibrations of instruments and accurate noise models for the device. However, noise behavior can be predicted to some extent by examining different figures-of-merit extracted from DC and RF measurements.

Along the course of this work, all devices were DC and RF characterized at both room and cryogenic temperatures. During measurements at room temperature, devices were exposed to ambient light at the manual probe station. For cryogenic characterization at 15 K, devices were measured with a covered viewport using Lakeshore CRX-4K probe station. Representative devices were later selected for additional noise characterization at room temperature.

2.2.2 *DC Characterization and DC Figures-of-Merit*

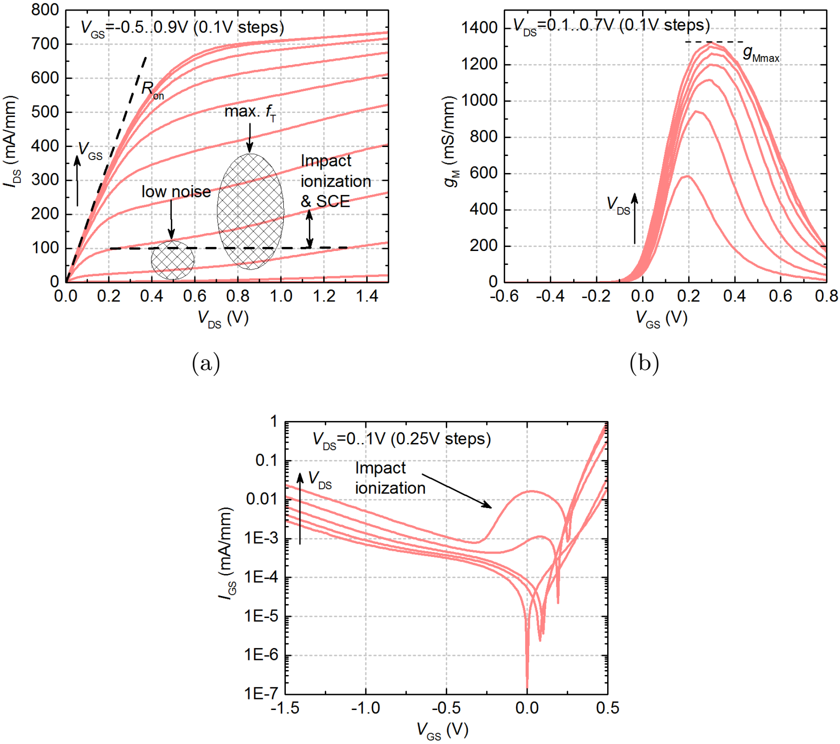
DC characteristics were obtained from on-wafer measurements using an Agilent HP4156B parameter analyzer. A common way of presenting the DC behavior of a HEMT is to plot the normalized I-V characteristics, the extrinsic DC transconductance g_{M} and the gate leakage current I_{GS}. Figure 2.4 shows the typical DC measurement of a two-finger HEMT, with a gate finger width of 25 µm (2 × 25 µm), measured at 300 K, for a device processed on standard epitaxial layer defined in section 3.1. Bias regions for obtaining best noise performance and highest cut-off frequency f_{T} are depicted in figure 2.4a.

For low drain-source voltages I_{DS} increases linearly, with a slope depending on the on-state resistance R_{on} as depicted in figure 2.4a. At high V_{DS}, I_{DS} does not stay constant but is increasing due to SCEs and impact ionization generated electrons in the narrow bandgap GaInAs channel, which reduce the output resistance of the HEMT.

R_{on} can be used as a figure-of-merit to predict the noise behavior, as low values of R_{on} imply low parasitic resistances and better noise behavior. For epitaxial layers where electrons tunneling indirectly through the cap and barrier layer into the channel do not contribute significantly to I_{DS}, a simplified expression can be used to calculate R_{on} based on the contact resistance R_{C} and channel sheet resistance R_{sheet}:

$$R_{\mathrm{on}} \approx 2 \cdot R_{\mathrm{C}} + R_{\mathrm{sheet}} \cdot l_{\mathrm{SD}} \tag{2.1}$$

where l_{SD} is the source-drain spacing (set to 1 µm along the course of this work). In figure 2.4a, extracted $R_{\mathrm{on}} \approx 0.57\,\Omega\text{·mm}$ which corresponds well to extracted contact resistance $R_{\mathrm{C}} = 0.11\,\Omega\text{·mm}$ and channel sheet resistance $R_{\mathrm{sheet}} = 350\,\Omega/\text{square}$ for our standard epitaxial layer. If conduction through cap and barrier layers is not negligible, a more complex model for R_{on} should be used. The complex model is more suited for epitaxial structures optimized for non-annealed Ohmic contacts, structures with high δ-doping or structures with very high cap doping where the cap serves as the extension of the source and drain metal contacts. As presented in figure 2.5,



(a)

(b)

(c)

FIGURE 2.4: a) Normalized DC output characteristic, b) transconductance g_M and c) gate current of a $2 \times 25\,\mu$m HEMT with 100 nm gate length measured at 300 K.

a more complete R_{on} model accounts for: contact resistance both directly from the metal layer to the channel and indirectly from the cap through the barrier into the channel, conductance through the cap and barrier layers in parallel over the length of the cap (R_p), resistance of the channel in the recess area (R_{rec}) and resistance of the channel ($R_{\mathrm{ch}}(V_{\mathrm{GS}})$) underneath the gate:

$$R_{\mathrm{on}} \approx 2 \cdot R_{\mathrm{C'}} + 2 \cdot R_{\mathrm{p}} \cdot l_{\mathrm{cap}} + 2 \cdot R_{\mathrm{rec}} \cdot l_{\mathrm{rec}} + R_{\mathrm{ch}}(V_{\mathrm{GS}}) \cdot l_{\mathrm{ch}}. \tag{2.2}$$

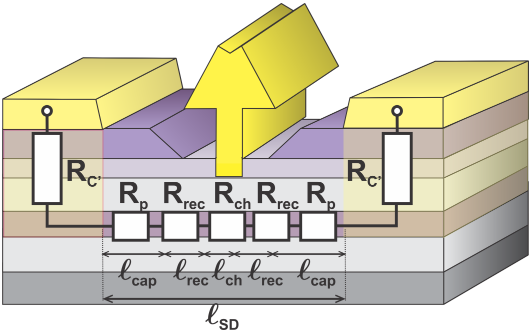


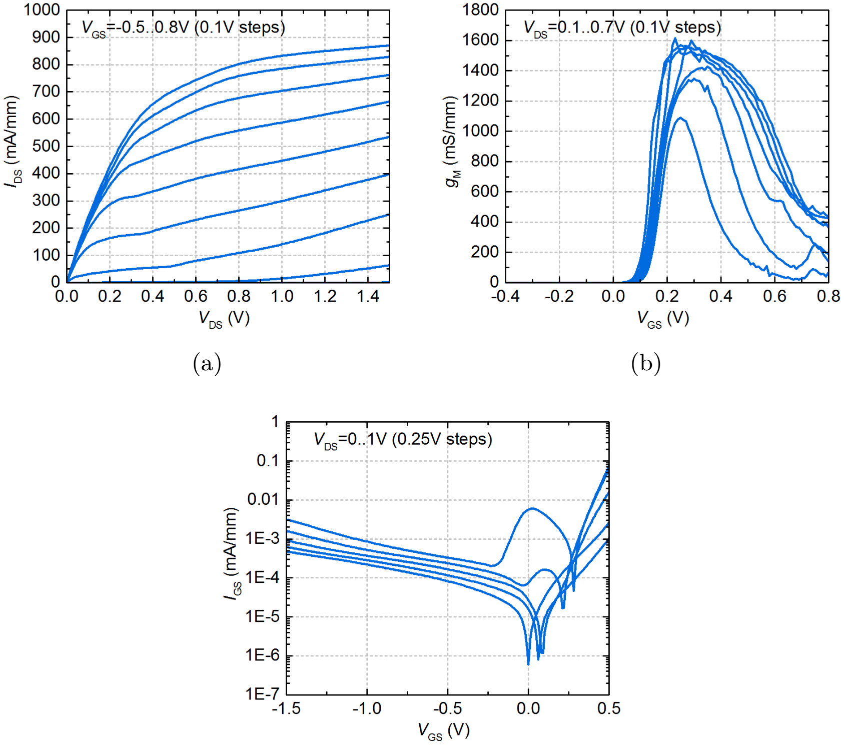
FIGURE 2.5: Cross-section of the InP HEMT showing contributions to the on-state resistance R_{on}.

Separated contributions of the individual terms from equation 2.2 are difficult to obtain; up to some extent the parallel resistance of channel and cap R_{p} can be extracted from standard Transfer Length Method (TLM) measurements on the full epitaxial structure, and R_{rec} can be taken as equal to R_{sheet} obtained from Hall measurements when the cap is layer removed. Contact resistance is hard to extract due to the fact that it accounts both for direct and indirect contact to the channel. One possibility investigated was fabrication of the TLM structures with constant l_{cap} and different lengths of the recessed area l_{rec}. However, measurements of those types of structures failed to provide linear and reproducible dependence of measured resistance versus the l_{rec}, hence the accurate $R_{C'}$ could not be extracted.

Another important figure-of-merit is the quality of gate control over the channel, represented by the transconductance $g_{\mathrm{M}} = \partial I_{\mathrm{DS}}/\partial V_{\mathrm{GS}}$, and plotted in figure 2.4b. High g_{M} values indicate high intrinsic and RF transconductance, $g_{\mathrm{M,intr}}$ and g_{m}, and allow predictions of the maximum transistor gain. Besides having high control of the channel current via gate voltage, a good pinch-off behavior is necessary to achieve good noise performance [1]. To assess the pinch-off quality, the ratio of the drain current in on- and off-state ($I_{\mathrm{on}}/I_{\mathrm{off}}$) around the threshold voltage is used. Good pinch-off at room temperature is considered to be $I_{\mathrm{on}}/I_{\mathrm{off}} > 70\,\mathrm{dB}$.

The gate diode current plotted in figure 2.4c should be below acceptable level required for good noise devices [1], which is on order of several µA/mm at room temperature, and an order of magnitude lower for cryogenic applications. To compare the leakage current for different epitaxial layers, the value of I_{GS} at $V_{\mathrm{GS}} = -1\,\mathrm{V}$ and $V_{\mathrm{DS}} = 0\,\mathrm{V}$ was usually used. Impact ionization, visible in the measurement of the drain current, can also be observed in the measurement of the gate current as the bell-shaped increment (hump) present at higher drain voltages. At moderate negative V_{GS} values, electron concentration in the channel is significant and the impact ionization coefficient is high if the drain voltage is high. Additional electron-hole pairs are generated in the region between gate and drain, and fraction of them can transfer over the barrier, get collected by the gate, and add to the gate current thereby giving the gate current specific bell-shape. If the gate current is high this feature might not be visible. However, impact ionization will still be noticeable in the I-V characteristic and S-parameters.

Figure 2.6 shows the DC measurement at 15 K of the same $2 \times 25\,\mu\mathrm{m}$ HEMT from figure 2.4. At cryogenic temperatures R_{on} is decreased while maximum current, transconductance and $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio are improved due to decreased thermal resistances, as shown in figures 2.6a and 2.6b. At lower temperatures gate leakage is decreased due to reduced thermionic emission over the Schottky barrier as shown in figure 2.6c.



(a)

(b)

(c)

FIGURE 2.6: a) Normalized DC output characteristic, b) transconductance g_M and c) gate current of a $2 \times 25\,\mu m$ HEMT with 100 nm gate length measured at 15 K.

2.2.3 *RF Characterization*

2.2.3.1 *RF Figures-of-Merit*

High frequency behavior of two-port networks such as HEMTs is usually described using the scattering parameters. S-parameters matrix elements are defined as:

$$\begin{aligned} S_{11} &= \left.\frac{b_1}{a_1}\right|_{a_2=0} & S_{21} &= \left.\frac{b_2}{a_1}\right|_{a_2=0} \\ S_{12} &= \left.\frac{b_1}{a_2}\right|_{a_1=0} & S_{22} &= \left.\frac{b_2}{a_2}\right|_{a_1=0} \end{aligned} \tag{2.3}$$

where a_1 and b_1 are the intensities of the incident and the reflected wave at port 1, and a_2 and b_2 are the intensities of the incident and the reflected wave at port 2. S_{ii} therefore represents the reflection coefficient at port i when all other ports are terminated with a reference impedance, whereas S_{ij} represents the transmission coefficient from port j to port i when port i is terminated with a reference impedance. Reference (or characteristic) impedance of measuring systems, probes, cables etc. in practice is usually 50 or 75 Ω. S-parameters are complex numbers, with real and imaginary part, and their graphical representation with respect to the frequency is usually done in the polar coordinate system such as the Smith diagram. The S-parameter matrix can be transformed to any other two-port network parameter set such as impedance (Z), admittance (Y), hybrid (H) and chain matrix ($ABCD$) parameters and vice versa.

S-parameters can be used to determine the RF figures-of-merit, of which the two most commonly used for high speed transistors are the current gain cut-off frequency f_T and the maximum oscillation frequency f_max. For a Field Effect Transistor (FET), f_T is defined as the frequency where the small-signal common-source current gain ($|h_{21}| = \frac{|i_\mathrm{ds}|}{|i_\mathrm{gs}|}$) drops to 1. h_{21} can be calculated from measured S-parameters as:

$$h_{21} = \frac{-2 \cdot S_{21}}{(1 - S_{11}) \cdot (1 + S_{22}) + S_{12} \cdot S_{21}}. \tag{2.4}$$

The frequency at which the power gain is equal to 1 is called f_max, but, due to different definitions used for power gain f_max is not a unique value. Assuming that $|S_{12}|$ is small and can be neglected (which is mostly the case in practice) a device can be considered to be unilateral, and Mason's unilateral power gain (U) can be used to determine $f_{\max}$. U can be calculated from measured S-parameters as follows:

$$U = \frac{\left|(S_{21}/S_{12}) - 1\right|^2}{2 \cdot \left(k \cdot |S_{21}/S_{12}| - \operatorname{Re}\left(S_{21}/S_{12}\right)\right)} \tag{2.5}$$

where k is the Rollet's stability factor:

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11} \cdot S_{22} - S_{12} \cdot S_{21}|^2}{2 \cdot |S_{21} \cdot S_{12}|}. \tag{2.6}$$

The device is said to be unconditionally stable when stability factor $k >= 1$ for all frequencies of interest. If that condition is fulfilled, a useful figure-of-merit is the maximum available gain (MAG):

$$\text{MAG} = \frac{|S_{21}|}{|S_{12}|} \cdot (k - \sqrt{k^2 - 1}). \tag{2.7}$$

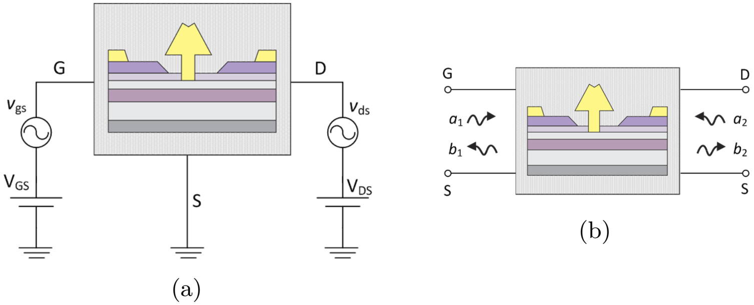
MAG indicates the highest amount of power gain that can be achieved with simultaneous conjugate matching on the input and the output of the device, but it is defined only for $k >= 1$. If $k < 1$ for certain frequencies, the device is conditionally stable and the maximum stable power gain (MSG) defined as:

$$\text{MSG} = \frac{|S_{21}|}{|S_{12}|} \tag{2.8}$$

should be used to calculate the power gain under stable operating conditions. At low frequencies, transistor gain is usually very high and consequently $k < 1$, therefore MSG is used for characterization. As the frequency increases, the gain is reduced and $k >= 1$ is obtained. In this case MSG converts into MAG. Unlike MAG, the unilateral gain U is defined for all values of k. All three power gain definitions can be used for estimating the $f_{\max}$ of the transistor. Along the course of this work, $f_{\max}$ was determined from Mason's unilateral power gain, unless noted otherwise.

2.2.3.2 *RF Measurements*

In order to measure the RF properties of InP HEMTs, devices were biased by applying DC voltages at the gate and drain as depicted in figure 2.7a. An RF signal was then superimposed to the device by a Vector Network Analyzer (VNA), either to the gate or drain electrode successively, for the selected frequency range. The RF signal amplitude was small and did not affect the bias point of the device thereby facilitating the small-signal characterization of the HEMT. The VNA measures intensities of incident (a_1 and a_2) and reflected (b_1 and b_2) normalized voltage waves over a selected frequency range as depicted in figure 2.7b, and calculates the scattering parameters as described in equations 2.3. During the course of this work all S-parameter measurements, both at room and cryogenic temperatures, were performed using an Agilent N5245 PNA-X network analyzer, with an Agilent HP4156B parameter analyzer used for biasing. Devices were measured on-wafer, up to 50 GHz, with a reference impedance of 50 Ω. The PNA-X was calibrated and systematic errors of the test setup were corrected up to the measuring probe tips using the Line-Reflect-Reflect-Match (LRRM) technique with Thru/Short/Load off-wafer calibration standards.



(a)

(b)

FIGURE 2.7: a) Schematic representation of the measurement setup used for measuring the RF behavior of InP HEMT at a bias point defined by V_{DS} and V_{GS}. b) Corresponding two-port network with port 1 defined by gate and source, and port 2 by drain and source electrodes.

The microwave probes used for contacting and measuring the device are usually large compared to the transistor active region, therefore device layout had to include appropriately sized probing pads. Probing pads contribute with their own parasitic capacitance, inductance and resistance, and consequently the measured S-parameters include both device and pad elements. To take out the parasitic effects of the pads, a deembedding procedure was required, where the contribution of the pads was mathematically removed from the measured data. As the first step, special OPEN and SHORT structures, fabricated together with devices, were measured over the same frequency range. These structures use an identical layout to the transistor except that the active area is covered with a metalization for the SHORT and omitted for the OPEN structure, as depicted in figure 2.8. An iterative deembedding procedure [26] gradually subtracts the contributions of the measured OPEN and SHORT structures divided in n non-equal sections from the measured S-parameters. The deembedded Y-parameters of the Device Under Test (DUT), $Y^{\mathrm{OS}}_{\mathrm{DUT},n}$, can be calculated as follows:

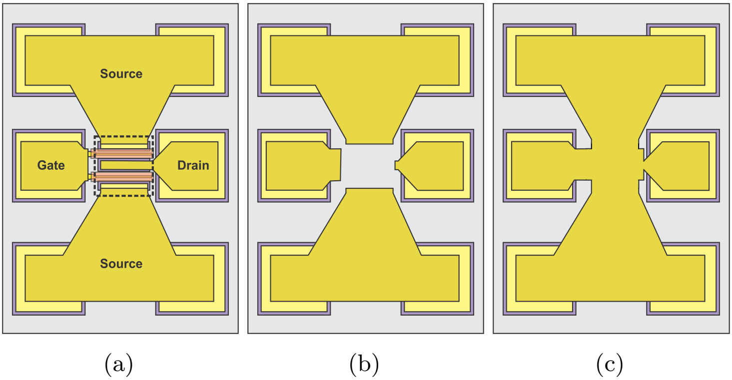
$$Y^{\mathrm{OS}}_{\mathrm{TEMP},i} = \frac{Y^{\mathrm{OS}}_{\mathrm{O},i-1}}{n+1-i} \tag{2.9}$$

$$Z^{\mathrm{OS}}_{\mathrm{TEMP},i} = \frac{(Y^{\mathrm{OS}}_{\mathrm{S},i-1} - Y^{\mathrm{OS}}_{\mathrm{TEMP},i})^{-1}}{n+1-i} \tag{2.10}$$

$$Y^{\mathrm{OS}}_{\mathrm{DUT},i} = ((Y^{\mathrm{OS}}_{\mathrm{DUT},i-1} - Y^{\mathrm{OS}}_{\mathrm{TEMP},i})^{-1} - Z^{\mathrm{OS}}_{\mathrm{TEMP},i})^{-1} \tag{2.11}$$

where $Y^{\mathrm{OS}}_{\mathrm{DUT},0}$, $Y^{\mathrm{OS}}_{\mathrm{O},0}$ and $Y^{\mathrm{OS}}_{\mathrm{s},0}$ are the measured two-port admittance parameters of the DUT, OPEN and SHORT, n is the number of iterations and i is swept from 1 to n. n was usually set to a high value, typically 100, to allow the method to converge to a unique solution. From the deembedded S-parameters, f_{T} and f_{max} of the intrinsic transistor without the parasitic influence of the pads can be obtained.

For high speed transistors, f_{T} and f_{max} are usually above the measurement setup frequency range: it is therefore not possible to directly extract them using equations 2.4-2.8. However, both $|h_{21}|$ and U behavior, plotted in dB on a logarithmic frequency scale, can be approximated using single pole functions with a -20 dB/dec roll-off after the first pole. Theoretical slopes form MSG and MAG are -10 dB/dec and -20 dB/dec, respectively. To be able to fit the measured data with a single pole fit (for $|h_{21}|$ and U) or -10/-20 dB/dec linear fit (for MSG/MAG), devices need to be at least measured up to the first pole, or up to the frequency where $k >= 1$ and MSG converts to MAG.

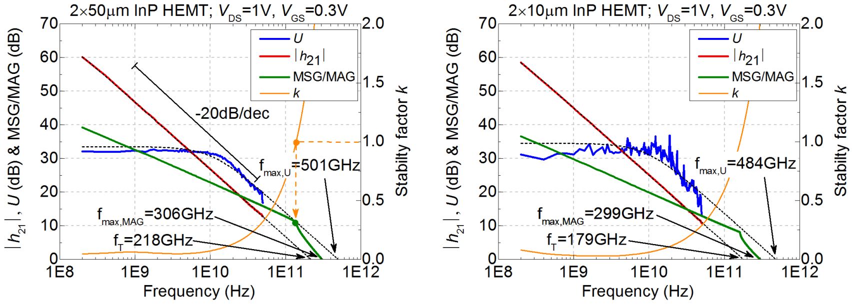


(a) (b) (c)

FIGURE 2.8: a) Schematic illustration of a complete two-finger transistor, b) OPEN and c) SHORT structures used to deembed the effects of the measurement pads.

f_T and f_max can be then extrapolated from the intersection of the respective characteristics with 0 dB as shown in figure 2.9a. Figure 2.9a shows the $|h_{21}|$, U, MSG/MAG and k calculated from measured S-parameters for a $2 \times 50\,\mu\mathrm{m}$ device, fabricated on standard epitaxial layer described in section 3.1. Device was measured at room temperature, and biased for maximum f_T.

Due to their low input resistance and capacitance, nanoscale HEMTs may exhibit resonant spikes in U as a consequence of the measurement uncertainties in S-parameters which can make a precise single pole fit and extrapolation of f_max difficult [27]. These resonances are more pronounced for transistors with S_{11} close to unity, as is the case for narrow gate widths, short gate lengths or large gate-to-channel distance, all resulting in small gate-to-source capacitance C_gs. According to equation 2.5, U is also very sensitive to the S_{21}/S_{12} ratio, which is inherently decreasing for narrower gate widths. Figure 2.9b shows the $|h_{21}|$, U, MSG/MAG and k calculated from measured S-parameters for a short $2 \times 10\,\mu\mathrm{m}$ device biased at the same bias point as the device in figure 2.9a. As it can be seen, clean extrapolation of f_max using the single pole fit through the U data with resonant spikes is problematic and its accuracy questionable. However, extrapolating f_max using MSG/MAG is only marginally better, since measurements above 100 GHz are required even for devices with low f_T.



(a) (b)

FIGURE 2.9: Measurement of the current gain ($|h_{21}|$), unilateral power gain (U), maximum stable gain (MSG) and maximum available gain (MAG) together with Rollet's stability factor k versus the measurement frequency for a) long device and b) short device.

2.2.4 *HEMT Modeling*

2.2.4.1 *Basic Small-Signal Model*

To design a microwave circuit such as an LNA, it is necessary to have an accurate device model that can reproduce measured S-parameters at a desired temperature. Most commonly used model is the Small-Signal Equivalent Circuit (SSEC) which describes the RF performance of a device for a discrete DC bias point. Being the link between physical features of the transistor structure and its electrical circuit representation, the SSEC allows analysis and provides insight into device behavior at high frequencies. A physically representative SSEC can give indications for device optimization, allows predictions for frequencies beyond measurement setup range and can be used for device scaling due to the close connection between the device's geometry and individual elements of the model. In general, the SSEC shown in figure 2.10 can be divided into two parts, extrinsic and intrinsic, where the extrinsic circuit also includes the contact pads. If the contribution of the pads has been deembedded, as explained in section 2.2.3.2, parallel branches with series capacitors and resistors, $C_{\mathrm{g,dsub}i}$ and $R_{\mathrm{g,dsub}i}$, are replaced with two small capacitances to the ground C_{pgs} and C_{pds}. Figure 2.11 shows the physical origin of the SSEC elements presented in figure 2.10 (with deembedded contribution of the contact pads). All elements of the Small-Signal Extrinsic Equivalent Circuit (SSEEC) and Small-Signal Intrinsic Equivalent Circuit (SSIEC) can be extracted from the measured S-parameters. SSEEC elements are extracted when the device is in the cold FET mode with $V_{\mathrm{ds}} = 0$, and SSIEC elements are extracted when $V_{\mathrm{ds}} > 0$ after the elements of the SSEEC have been mathematically removed from the measured data. Extraction routine of the SSEEC used in this work is described in detail in [28]. The method used to extract the SSIEC is based on the extended Berroth model [29].

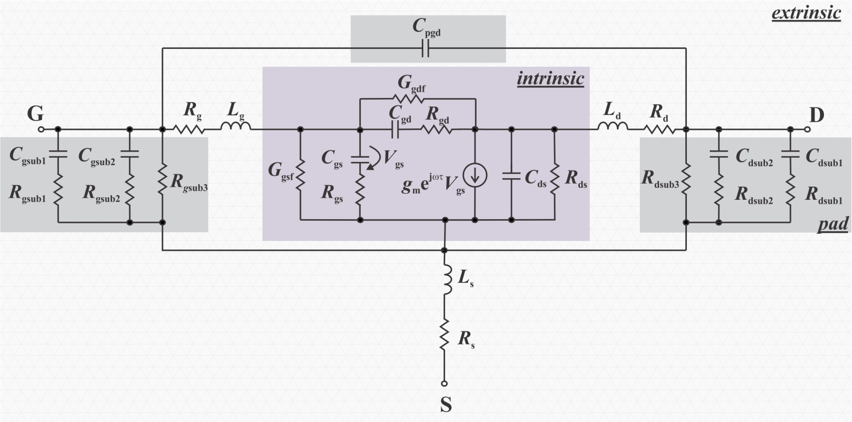


FIGURE 2.10: Small-signal equivalent circuit of the InP HEMT consisting of extrinsic and intrinsic part as described in [28].

The SSEEC elements are bias-independent and are determined by the device's physical structure and properties such as the device size, geometrical shape, contact resistance etc. Measurement pads are modeled by several parallel branches with resistors and capacitors in series, while coupling between gate and drain contact pads is modeled by capacitance C_{pgd}. The extrinsic inductances L_{g}, L_{s} and L_{d} model the inductive behavior of the gate, source and drain contacts. While L_{g} and L_{d} increase with increasing the device width, L_{s} decreases as a result of broadening the outer source pads. The extrinsic resistances R_{g}, R_{s} and R_{d} model the resistive behavior of the respective contacts and access resistances. Whereas R_{s} and R_{d} are

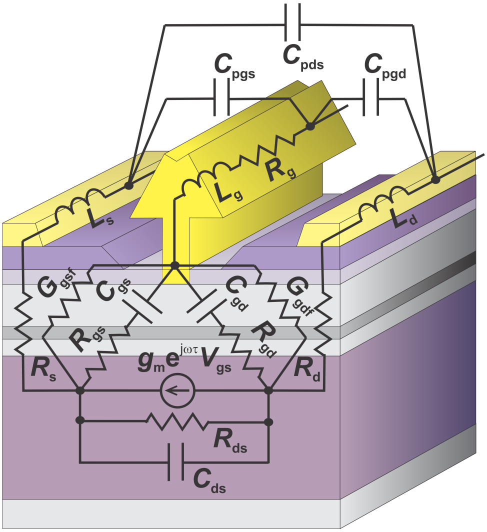


FIGURE 2.11: Physical origin of the small-signal equivalent circuit elements of the InP HEMT depicted in figure 2.10.

mostly determined by the Ohmic contact resistance, R_g is determined by the resistance of the gate metalization, and a special process monitor is required for its extraction [28]. R_g scales linearly with gate width, while R_s and R_d are inversely proportional to the gate width.

The SSIEC elements depend on the selected bias point and describe the behavior of the 2DEG in the active area of the device. The gain mechanism of the HEMT is modeled by a voltage controlled current source with a maximum transconductance $g_\mathrm{m}^\mathrm{max}$:

$$g_\mathrm{m}^\mathrm{max} = \frac{v_\mathrm{sat} \cdot \epsilon_0 \cdot \epsilon_\mathrm{2DEG}}{d} \tag{2.12}$$

reached when electrons in the channel travel with the effective saturation velocity v_sat. $g_\mathrm{m}^\mathrm{max}$ is inversely proportional to the physical distance between gate foot metal and the channel d. τ and R_ds represent the transit time of the electrons underneath the gate and the output resistance, respectively. The capacitance C_gs accounts for the change of carrier density in the channel with respect to the change of V_{gs}. The maximum value of C_{gs} can be assumed to correspond to the geometrical capacitance between gate foot and the channel:

$$C_{\mathrm{gs}} = \frac{l_{\mathrm{G}} \cdot \epsilon_0 \cdot \epsilon_{\mathrm{2DEG}}}{d} \tag{2.13}$$

where l_{G} is the gate length. C_{gs} is also inversely proportional to the physical distance between gate foot metal and the channel d. C_{ds} represents the capacitance between source and drain electrodes. C_{gd} is the gate-drain feedback capacitance, representing the change of 2DEG density with the change of V_{ds}, depending strongly on gate-to-drain distance. R_{gs} and R_{gd} account for the intrinsic gate contact resistance and gate-drain feedback resistance, respectively. G_{gsf} and G_{gdf} model the non-zero leakage current between the gate-source and gate-drain contacts, respectively. As a first approximation, it can be considered that intrinsic capacitances and the transconductance scale linearly with gate width, while intrinsic resistances are reverse proportional with respect to the device width. Both f_{T} and f_{max} as defined is section 2.2.3.1 can now be expressed using the small-signal model element values as follows:

$$f_{\mathrm{T}} = \frac{g_{\mathrm{m}}}{2\pi} \cdot \frac{1}{(C_{\mathrm{gs}} + C_{\mathrm{gd}}) \cdot (1 + \frac{R_{\mathrm{s}}+R_{\mathrm{d}}}{R_{\mathrm{ds}}}) + g_{\mathrm{m}} \cdot C_{\mathrm{gd}} \cdot (R_{\mathrm{s}} + R_{\mathrm{d}})} \tag{2.14}$$

$$f_{\mathrm{max}} = \frac{f_{\mathrm{T}}}{2\sqrt{\frac{R_{\mathrm{g}} + R_{\mathrm{s}} + R_{\mathrm{gs}}}{R_{\mathrm{ds}}} + 2 \cdot \pi \cdot f_{\mathrm{T}} \cdot C_{\mathrm{gd}} \cdot R_{\mathrm{g}}}}. \tag{2.15}$$

2.2.4.2 *Extended Small-Signal Model*

According to equations 2.14 and 2.15, to further improve the RF performance of InP HEMTs it is necessary to increase the transconductance g_{m} while decreasing the parasitic resistances and capacitances. Using a narrow bandgap channel material, such as In-rich GaInAs, will provide higher carrier mobility and saturation velocity and thereby also higher g_{m}. However, at high drain-source voltages, narrow bandgap channels suffer from impact ionization effects which degrade transistor DC, RF and noise performance. For high In-content or pure InAs channel, the onset of impact ionization can be even at a relatively low drain voltage of $V_{\mathrm{DS}} = 0.5\,\mathrm{V}$ which is close to the typical low-noise bias point. Impact ionization has been reported to cause an inductive drain impedance due to the phase lag between the drain-source voltage and the impact ionization current, as well as a reduced transmission coefficient S_{21} due to reduced output resistance at low frequencies [30] [31]. To model the electron-hole pair generation due to impact ionization, an additional voltage-controlled current source is added in the output circuit of the transistor's small-signal model [30] as depicted in figure 2.12.

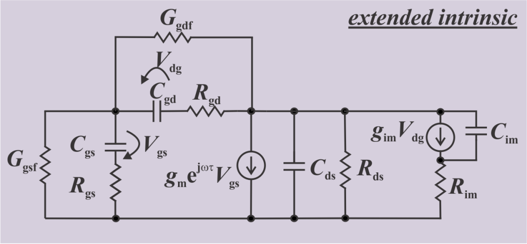


FIGURE 2.12: Intrinsic small-signal equivalent circuit including circuitry modeling impact ionization.

The added current source is controlled by the intrinsic drain-gate voltage V_{dg}, with transconductance g_{im}, while its frequency dependence is modeled with a series $R_{\mathrm{im}}C_{\mathrm{im}}$ circuit parallel to the output resistance R_{ds}. Additional impact ionization modeling elements were determined using a numerical fitting method following the extraction of the basic SSEC as described in [28]. The fitting method used included applying a constrained nonlinear optimization to find the minimum of the difference between measured and modeled imaginary part of intrinsic $Y_{12,\mathrm{i}} + Y_{22,\mathrm{i}}$ for the selected frequency range. According to figure 2.12, and as shown in appendix A1, the model $Y_{12,\mathrm{i}} + Y_{22,\mathrm{i}}$ is calculated as:

$$Y_{12,\mathrm{i}} + Y_{22,\mathrm{i}} = \frac{1 + j \cdot \omega \cdot R_{\mathrm{ds}} \cdot C_{\mathrm{ds}}}{R_{\mathrm{ds}}} + \frac{g_{\mathrm{im}}}{1 + j \cdot \omega \cdot R_{\mathrm{im}} \cdot C_{\mathrm{im}}} \cdot \frac{1}{1 + j \cdot \omega \cdot R_{\mathrm{dg}} \cdot C_{\mathrm{dg}}}. \tag{2.16}$$

With respect to device size, transconductance g_{im} scales linearly with device width, while the impact ionization time constant $\tau_{\mathrm{im}} = (R_{\mathrm{im}} \cdot C_{\mathrm{im}})$ remains invariant. Because impact ionization is manifested in the low frequency measurements, the range used for extraction of additional elements was set to

0.05-10 GHz. The S-parameter measurement sweep included larger number of frequency points in the low frequency range to ensure good resolution for accurate extraction of the impact ionization related elements. The modeled and measured S-parameters for an InP HEMT (with deembedded contact pads) at a bias point where impact ionization is manifested are depicted in figures 2.13 (300 K) and 2.14 (15 K) and show a good agreement for both temperatures. Measured device was fabricated on standard structure detailed in section 3.1, featuring GaInAs channel, therefore the bias point used to demonstrate the effects of impact ionization had high drain voltage of $V_{\mathrm{DS}} = 1\,\mathrm{V}$. The corresponding elements of the small-signal circuit are listed in table 2.1.

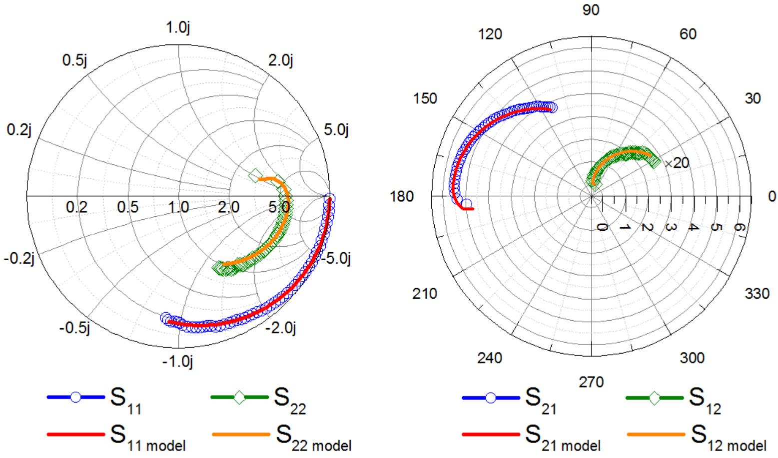


FIGURE 2.13: Measured and modeled S-parameters for a $2 \times 25\,\mu\mathrm{m}$ HEMT measured at 300 K with $V_{\mathrm{DS}} = 1\,\mathrm{V}$ and $V_{\mathrm{GS}} = 0.3\,\mathrm{V}$. Frequency range is 50 MHz to 50 GHz.

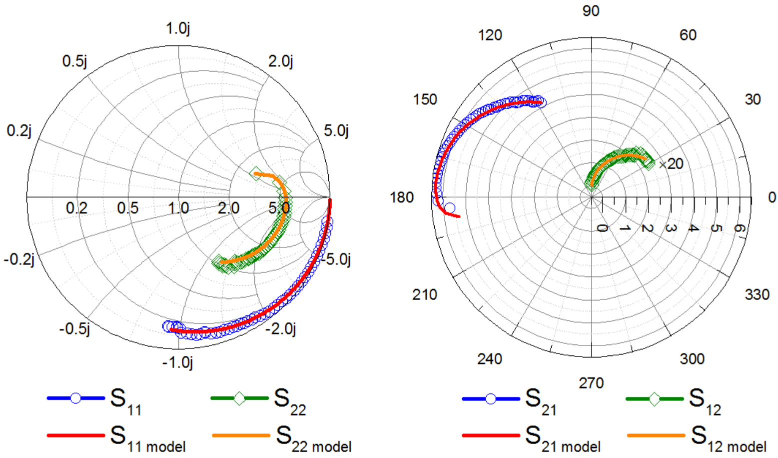


FIGURE 2.14: Measured and modeled S-parameters for a $2 \times 25\,\mu\text{m}$ HEMT measured at 15 K with $V_{\text{DS}} = 1\,\text{V}$ and $V_{\text{GS}} = 0.3\,\text{V}$. Frequency range is 50 MHz to 50 GHz.

Parameter	Value at 300 K	Value at 15 K	Parameter	Value at 300 K	Value at 15 K
R_{s}	4.03 Ω	2.9 Ω	R_{gs}	3.8 Ω	1.14 Ω
R_{d}	4.14 Ω	3.2 Ω	R_{gd}	22 Ω	21.4 Ω
R_{g}	0.89 Ω	0.17 Ω	R_{ds}	238 Ω	243 Ω
L_{s}	0.17 pH	0.16 pH	C_{gs}	47.5 fF	45.9 fF
L_{d}	7.1 pH	7.71 pH	C_{gd}	6.58 fF	6.25 fF
L_{g}	10.8 pH	10.1 pH	C_{ds}	15.9 fF	9.89 fF
C_{pgd}	0.28 fF	0.22 pF	g_{m}	90.7 mS	95.3 mS
C_{pd}	0.4 fF	0.26 pF	τ	60 fsec	137 fsec
C_{pg}	0.8 fF	0.12 pF	g_{im}	6.23 mS	6.54 mS
G_{gsf}	4µS	1 µS	C_{im}	1.67 fF	11.4 fF
G_{gdf}	8 µS	2.4 µS	R_{im}	138 kΩ	27.1kΩ

TABLE 2.1: Extracted SSEC element values for a $2 \times 25\,\mu\text{m}$ HEMT measured at 300 and 15 K with $V_{\text{DS}} = 1\,\text{V}$ and $V_{\text{GS}} = 0.3\,\text{V}$.

2.2.5 *Noise Characterization*

2.2.5.1 *Noise Metrology*

Beside amplifying both the signal and the noise presented at their input, all amplifying devices add extra noise generated within, and degrade the SNR ratio at their output. InP HEMTs add exceptionally low noise powers to the input signal due to their superior transfer properties and minimal parasitic resistances and are therefore very attractive for low-noise applications. To describe the SNR degradation for a signal passing through a device, a frequency dependent noise figure is used. Noise figure is a function of the input (source) admittance and of four independent noise parameters:

$$F = F_{\mathrm{min}} + 4 \cdot \frac{R_{\mathrm{n}}}{Z_0} \cdot \frac{|\Gamma_{\mathrm{s}} - \Gamma_{\mathrm{opt}}|^2}{|1 + \Gamma_{\mathrm{opt}}|^2 \cdot (1 - |\Gamma_{\mathrm{s}}|^2)}. \tag{2.17}$$

Noise parameters describe how the noise figure changes as a function of the source reflection coefficient Γ_{s}. For each frequency, there is an optimum input reflection $\Gamma_{\mathrm{s}} = \Gamma_{\mathrm{opt}}$ coefficient where the minimum noise figure F_{min} is achieved. The noise resistance R_{n} characterizes how rapidly the noise figure changes from F_{min} when the input impedance is diverging from optimum, whereas Z_0 represent the characteristic impedance of a measurement setup (usually $50\,\Omega$). To characterize low noise devices it is also common to use the effective noise temperature, T_{e}, instead of the noise figure. The effective noise temperature is related to the noise figure with the following expression:

$$T_{\mathrm{e}} = (F - 1) \cdot T_0 \tag{2.18}$$

where T_0 is the reference temperature of 290 K.

To obtain the four noise parameters, at least four noise figure measurements corresponding to four different source reflection coefficients, adequately distributed over the Smith-chart, are needed. Usually, more than four terminations, provided by impedance tuners, are used to produce an overdetermined system of equations and minimize errors. Different techniques can later be used to extract the four noise parameters from the measured data. Besides direct extraction of the noise parameters from measurements, it is possible to use transistor's noise model to fit the modeled and measured data, and later use the model to predict the noise performance. The noise model is usually based on the SSEC, together with different number of elements/parameters used for fitting the measured and modeled data. This method has been validated even if only one noise figure measurement, corresponding to one source impedance ($50\,\Omega$), was available [32] [33]. However, this approach relies highly on accuracy of the used noise model, and a very good match between the measured and modeled S-parameters is a prerequisite.

Several semi-empirical device noise models based on extracted SSEC elements and appropriate fitting factors can be used [34] [35] [36] to simulate the noise performance of InP HEMTs when designing an LNA. In this work, noise modeling was performed using the SSEC as described in section 2.2.4 and using Pospiezalski's method [35]. In Pospiezalski's method, the device parasitic resistances contribute only to the thermal noise, while noise properties of the intrinsic chip are treated by assigning effective temperatures to gate (T_{g}) and drain (T_{d}). T_{g} is usually set to ambient temperature while T_{d} is used as a free parameter for fitting the modeled performance with measured noise figures.

There are two basic approaches used to measure the noise figure of a two port network: the Y-factor and cold-source (or direct) method [37]. While the Y-factor technique obtains the noise figure by measuring the noise powers for two different noise levels at the input (hot and cold), the cold-source approach requires only measurement of one noise power corresponding to a single noise level (cold) at the input. However, in cold-source approach usage of both hot and cold states of the noise source is required for the calibration of the noise receiver. Although direct approach is more complex since it requires device's available gain and the gain-bandwidth product of the receiver to be previously determined by a separate measurement, it provides more accuracy than the Y-factor method when measuring single transistors. The Y-factor method adds systematic errors due to different reflection coefficients for the noise source in the hot and cold states, and due to generally poor matching of the device's output and the noise receiver.

2.2.5.2 *Noise Measurements*

Noise measurements presented in this work were performed at room temperature, using the Maury Microwave ATS software v536.04 controlling the N5245A PNA-X, the HP4142 parameter analyzer, the noise receiver, the MT984AU automated tuner (8-50 GHz), HP87222E input and output switches and a 346CK01 noise source. The noise receiver was implemented with a cascade of three low-noise amplifiers and a spectrum analyzer unless noted otherwise. Test setup for the noise measurements is depicted in figure 2.15. Noise modeling and simulations presented in this work were performed using the Keysight's Advanced Design System (ADS) software.

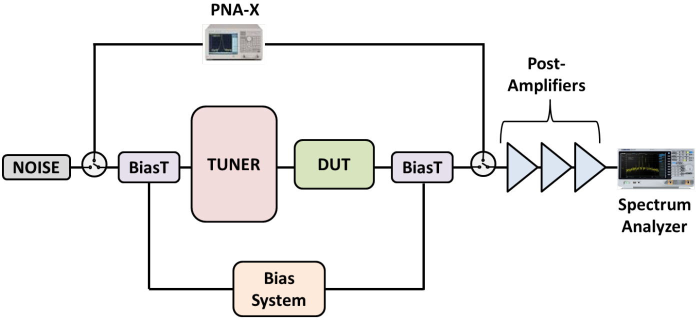


FIGURE 2.15: Block diagram of the noise measurement setup.

For noise characterization, devices were measured over the 8-50 GHz frequency range at room temperature using the cold-source method unless noted otherwise. The noise figure of the device was obtained using following calculations based on measured S-parameters for the tuner and for the device, measured noise power P_{COLD} and measured output reflection coefficient of the noise source $\Gamma_{\mathrm{NS,COLD}}$:

$$F = 1 + G_{\mathrm{TUN}} \cdot \left(\frac{P_{\mathrm{COLD}}}{G_{\mathrm{REC}} \cdot G_{\mathrm{AV}} \cdot MM} - \frac{F_{\mathrm{REC}} - 1}{G_{\mathrm{AV}}} - \frac{T_{\mathrm{COLD}}}{T_0} + 1 - F_{\mathrm{TUN}} \right) \tag{2.19}$$

where T_{COLD} is the ambient temperature, and $T_0 = 290\,\mathrm{K}$. F_{TUN} and G_{TUN} are the tuner noise factor and gain:

$$F_{\mathrm{TUN}} = 1 + \left(\frac{1}{G_{\mathrm{TUN}}} - 1\right) \cdot \frac{T_{\mathrm{COLD}}}{T_0}, \tag{2.20}$$

$$G_{\mathrm{TUN}} = \frac{1 - |\Gamma_{\mathrm{NS,COLD}}|^2}{|1 - S_{11,\mathrm{TUN}} \cdot \Gamma_{\mathrm{NS,COLD}}|^2} \cdot |S_{21,\mathrm{TUN}}|^2 \cdot \frac{1}{1 - |\Gamma_{\mathrm{s,DUT}}|^2}, \tag{2.21}$$

$$\Gamma_{\mathrm{s,DUT}} = S_{22,\mathrm{TUN}} + \frac{S_{21,\mathrm{TUN}} \cdot S_{12,\mathrm{TUN}} \cdot \Gamma_{\mathrm{NS,COLD}}}{1 - S_{11,\mathrm{TUN}} \cdot \Gamma_{\mathrm{NS,COLD}}}. \tag{2.22}$$

F_{REC} and G_{REC} are the receiver noise figure and gain obtained during receiver calibration:

$$F_{\mathrm{REC}} = F_{\mathrm{min,REC}} + 4 \cdot \frac{R_{\mathrm{n,REC}}}{Z_0} \cdot \frac{\left|\Gamma_{\mathrm{s,REC}} - \Gamma_{\mathrm{opt,REC}}\right|^2}{\left|1 + \Gamma_{\mathrm{opt,REC}}\right|^2 \cdot \left(1 - \left|\Gamma_{\mathrm{s,REC}}\right|^2\right)}, \tag{2.23}$$

$$\Gamma_{\mathrm{s,REC}} = S_{22,\mathrm{DUT}} + \frac{S_{21,\mathrm{DUT}} \cdot S_{12,\mathrm{DUT}} \cdot \Gamma_{\mathrm{s,DUT}}}{1 - S_{11,\mathrm{DUT}} \cdot \Gamma_{\mathrm{s,DUT}}}. \tag{2.24}$$

G_{AV} is the available gain of the cascade network of the device and the tuner, and MM is the mismatch between the device and the receiver:

$$MM = \frac{1 - \left|\Gamma_{\mathrm{s,REC}}\right|^2}{\left|1 - S_{11,\mathrm{REC}} \cdot \Gamma_{\mathrm{s,REC}}\right|^2}. \tag{2.25}$$

The procedure for noise characterization was as follows:

- The device was inserted in the noise measurement setup and S-parameters were measured for a selected bias point.
- The small-signal model was extracted from measured S-parameters.
- The noise figure was measured using the cold-source approach with 34 different impedances presented to the input of the device.
- The drain temperature T_{d} was determined by varying its value until the difference between the simulated noise figure of extracted SSEC and measured noise figure for all 34 input impedances is minimized.
- Using the Pospiezalski's noise model, a small-signal simulation generates a complete set of four noise parameters.

Noise measurements, besides requiring a complex setup, are time consuming since they require several calibration steps, frequency sweeps for all tuner states and all bias points, model extractions, optimizations and simulations thus making characterization of each single transistor not practical. However, from the measured DC and RF performance it is possible to estimate to a certain extent the noise behavior of a device and preselect the most promising ones for noise measurements. Using Pospiezalski's noise model, an expression for the minimum noise temperature, omitting the influence of gate leakage current, is given as:

$$T_{\mathrm{min}} \approx 2 \cdot \frac{f}{f_{\mathrm{T}}} \cdot \sqrt{r_{\mathrm{t}} \cdot T_{\mathrm{g}} \cdot g_{\mathrm{ds}} \cdot T_{\mathrm{d}}} \tag{2.26}$$

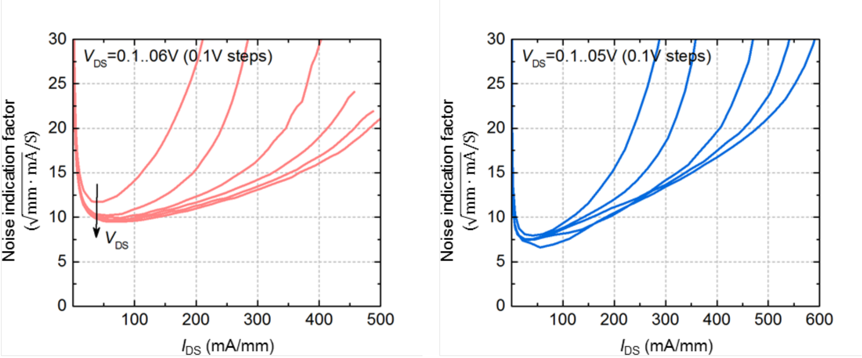
where g_{ds} is the output conductance and $r_{\mathrm{t}} = R_{\mathrm{s}} + R_{\mathrm{g}} + R_{\mathrm{gs}}$. Taking into account that only T_{d} and f_{T} are strong functions of transistor bias, with T_{d} almost linearly depending on the drain current, the minimum noise temperature can be obtained for transistor bias where the value of

$$\frac{\sqrt{I_{\mathrm{ds}}}}{g_{\mathrm{m}}} \tag{2.27}$$

is minimized. Therefore, a low-noise HEMT should have high transconductance achieved at low drain-source current. Expression given in 2.27 is usually referred to as the Noise Indication Factor (NIF), and its minimum value can be used as one of the figures-of-merit to predict the noise performance. The RF transconductance g_{m}, used in expression 2.27, and intrinsic DC transconductance $g_{\mathrm{M,intr}}$ are comparable, with differences arising from impact ionization and charge trapping effects affecting only DC $g_{\mathrm{M,intr}}$. Improvement resulting from device or epitaxial optimization can be observed in both transconductances when biased away from regions where additional carriers are generated or trapped. Because the extrinsic g_{M} and intrinsic $g_{\mathrm{M,intr}}$ are correlated by following equation:

$$g_{\mathrm{M}} = \frac{g_{\mathrm{M,intr}}}{1 + g_{\mathrm{M,intr}} \cdot R_{\mathrm{s}}}, \tag{2.28}$$

it is justified to use the DC extrinsic g_{M} instead of g_{m} to roughly evaluate NIFs for different devices. NIF can be used to compare devices with similar geometry; any change in vertical dimensions will not be properly reflected in the value of expression 2.27 since it does not include capacitances which have a large influence on f_{T}. In figure 2.16a, the NIF versus drain current is shown for a $2 \times 25\,\mu\mathrm{m}$ device from figure 2.4. A minimum is visible for I_{DS} between 50 and 100 mA/mm, and $V_{\mathrm{DS}} \approx 0.5\,\mathrm{V}$. At cryogenic temperatures, as a consequence of reduced resistances and increased g_{m}, NIF is decreasing and optimum bias point is moving towards lower drain current as depicted in figure 2.16b. The optimum I_{DS} at cryogenic temperatures is below 50 mA/mm with $V_{\mathrm{DS}} \approx 0.5\,\mathrm{V}$.

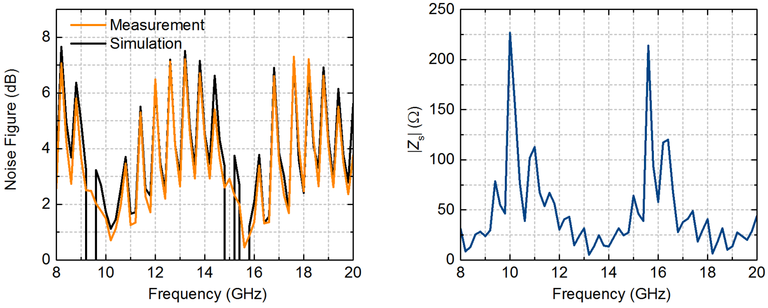


(a) (b)

FIGURE 2.16: Noise indication factor for a $2 \times 25\,\mu\text{m}$ HEMT with 100 nm gate length a) measured at 300 K and b) measured at 15 K.

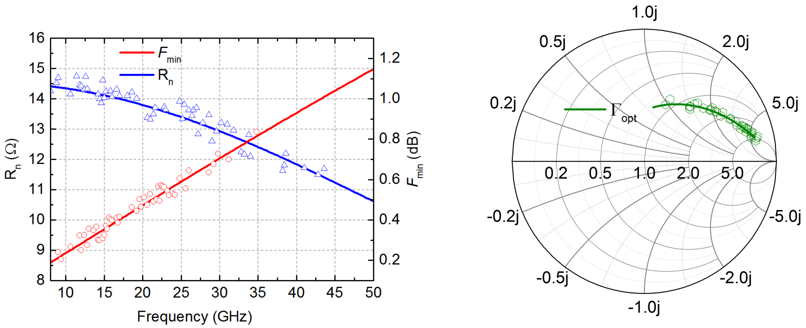
Typical noise measurement data and simulation of the extracted noise model from 8-20 GHz are depicted in figure 2.17a for one arbitrary impedance tuner state. Device in figure 2.17a is a $2 \times 25\,\mu\text{m}$ InP HEMT, the same device from figure 2.4, biased close to optimum low-noise bias point of $V_{\text{DS}} = 0.5\,\text{V}$ and $I_{\text{DS}} = 100\,\text{mA/mm}$. Extracted drain temperature for this bias point is $T_{\text{d}} = 2153\,\text{K}$. Measurements and simulation show similar and good fit for all tuner states. The shape of measured noise figure has a characteristic form versus frequency due to the source impedance, Z_{s}, varying with frequency as shown in figure 2.17b. The extracted and modeled noise parameters are shown in figure 2.18.

On the path to circuits operating at THz frequencies an increase of the transconductance g_{m} is required, together with reduction of the parasitics resistances and capacitances by scaling the lateral and vertical HEMT dimensions. Common approach, as stated in section 2.2.4.2, is to use the narrower bandgap material for the channel such as In-rich GaInAs or pure InAs. However, while the device frequency performance will improve, the noise performance will suffer due to the optimum low-noise bias point potentially located close or at the onset of impact ionization. Along the collaboration with *Centro Astronómico de Yebes* and *ESA*, increased low-frequency noise was observed in devices with InAs/GaInAs channels compared to the devices



(a) (b)

FIGURE 2.17: a) Measured and modeled noise figure for a 2 × 25 µm HEMT at 300 K with $V_{DS} = 0.5\,\mathrm{V}$ and $I_{DS} = 100\,\mathrm{mA/mm}$. b) Magnitude of the source impedance, $|Z_s|$, presented to the device.



(a) (b)

FIGURE 2.18: Extracted and modeled noise parameters a) F_{min} and R_{n} and b) Γ_{opt} for a 2 × 25 µm HEMT measured at 300 K with $V_{DS} = 0.5\,\mathrm{V}$ and $I_{DS} = 100\,\mathrm{mA/mm}$. Extracted $T_d = 2153\,\mathrm{K}$.

with conventional GaInAs channel. During the testing procedure devices were inserted in the first stage of the hybrid wide-band amplifier and their gain and effective noise temperature were measured at 15 K. In figure 2.19 a comparison for three different devices, all biased with equal V_{DS} and I_{DS}, is shown:

- 2 × 100 µm HEMT with GaInAs channel from NGST,
- 2 × 100 µm HEMT with 1 nm InAs inserted in GaInAs channel from ETH,
- 2 × 150 µm HEMT with GaInAs channel from ETH.

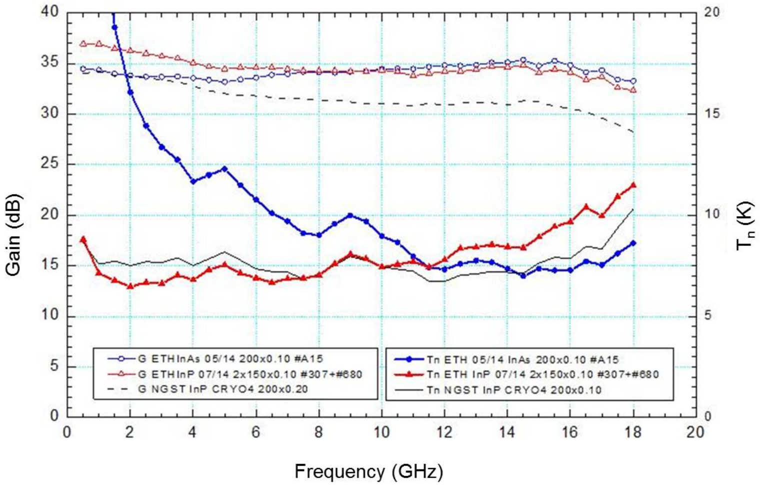


Figure 2.19: Gain and effective noise temperature for various HEMTs measured at 15 K biased at the same bias point. Graph obtained from *Centro Astronómico de Yebes.*

For the device with InAs channel inset, a large increase in noise temperature T_n can be observed below 10 GHz. The shape of elevated low frequency noise was similar as reported in [38], where it was attributed to impact ionization as a result of increased V_DS. In figure 2.19, all three devices were biased with the same $V_\mathrm{DS}/I_\mathrm{DS}$, however, due to the InAs inset in the channel, onset for impact ionization was at lower V_DS compared to devices with a GaInAs channel. The InAs channel inset device was the only one showing signs of impact ionization at the selected bias point, and it was also the only one exhibiting impaired noise performance.

The observed behavior could not be clearly identified or modeled using the noise figures obtained in the standard way described in this section. To investigate if the worse performance in fact impact ionization related, and whether it is possible to model it using the small-signal circuit as described in section 2.2.4.2, additional measurements were done in the low frequency range. Low frequency measurements were performed over 0.8-18 GHz range, with the same measurement setup from figure 2.15 but using a low frequency impedance tuner MT982BU (0.8-18 GHz) instead of MT984AU. For this frequency range the Maury MT7553 module was used as the noise receiver.

Measurements were performed on a device with GaInAs channel, the same shown for 8-50 GHz range in figures 2.17 and 2.18, to exclude any unknown effect arising from the InAs channel. The device was biased at $V_{\mathrm{DS}} = 1\,\mathrm{V}$ and $I_{\mathrm{DS}} = 100\,\mathrm{mA/mm}$, a bias point where measured S-parameters showed the onset of impact ionization. The noise parameters (F_{min}, R_{n} and Γ_{opt}), extracted from measurements by the Maury software, were used to fit the model and measured data from over 0.8-18 GHz range as opposed to the total measured noise figure (F) which was used to fit the measurements over 8-50 GHz range. Noise parameters extracted from measurements, and noise parameters obtained from the standard and extended model including impact ionization are depicted in figure 2.21. Both the minimum noise figure F_{min} and the noise resistance R_{n} extracted from measurements show a large increase at lower frequencies, similar to what was observed in figure 2.19 for a device with an InAs channel inset.

In order to fit the device model to the noise measurements shown in figure 2.21, an additional ideal white noise source had to be added to the noise model based on the extended SSEIC described in section 2.2.4.2. The additional current noise source i_{noise} accounting for noise generated by impact ionization was added parallel to the g_{im} and C_{im} as depicted in figure 2.20.

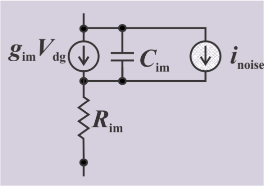
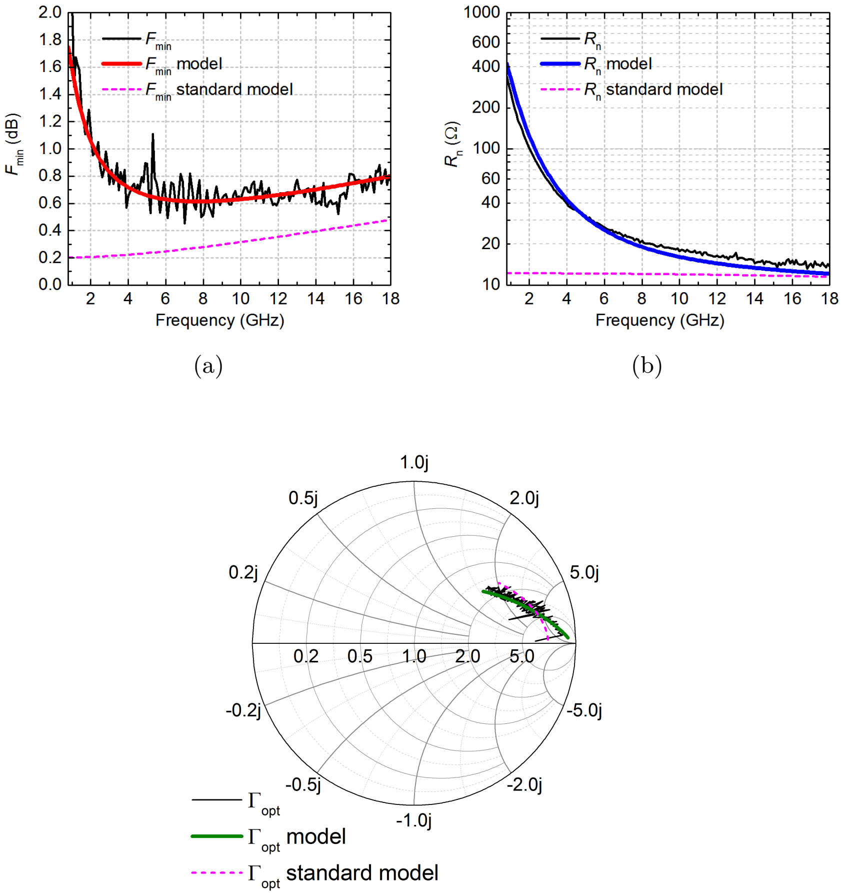


FIGURE 2.20: White noise source added to the device noise model representing the noise generated by impact ionization.



(a)

(b)

(c)

FIGURE 2.21: Extracted and modeled noise parameters a) F_{min}, b) R_{n} and c) Γ_{opt} for a $2 \times 25\,\mu\mathrm{m}$ HEMT measured at 300 K with $V_{\mathrm{DS}} = 1\,\mathrm{V}$ and $I_{\mathrm{DS}} = 100\,\mathrm{mA/mm}$.

The frequency behavior of the added current noise source is given as:

$$i_{\mathrm{im}} = \frac{i_{\mathrm{noise}}}{\sqrt{1 + (\omega \cdot R_{\mathrm{im}} \cdot C_{\mathrm{im}})^2}} \tag{2.29}$$

due to the arrangement of the i_{noise} and the $R_{\mathrm{im}}C_{\mathrm{im}}$ circuit. However, because of the significant increase in the gate current from holes generated by impact ionization, just adding i_{noise} to the noise model was not sufficient to fit all four noise parameters. To account for the increased gate leakage and its influence on the noise, the effective temperature of the resistances at the gate side (R_{gs}, R_{gd}, G_{gsf} and G_{gdf}) had to be increased to T_{im}, similar as in [30]. In [30], three different noise temperatures and a white noise source were used for modeling, where the third temperature accounts for the gate leakage resulting from electrons tunneling through the barrier to the gate. The measured device, depicted in figure 2.21, had low gate leakage (order of magnitude lower compared to [30]), hence it was not necessary to add the third noise temperature to the model. Optimized values of T_{d}, T_{im} and i_{noise} for the device depicted in figure 2.21 are:

$$\begin{aligned} T_{\mathrm{d}} &= 7661\,\mathrm{K}, \\ T_{\mathrm{im}} &= 951\,\mathrm{K}, \\ i_{\mathrm{noise}} &= 377.5\,\mathrm{pA}. \end{aligned}$$

They were obtained by tuning and optimizing their values to minimize the difference between extracted and simulated noise parameters using the least-squares error function built in the ADS Gradient Optimizer. From figure 2.21 it can be observed that the model which includes impact ionization circuit is capable of replicating low frequency behavior of noise parameters, whereas the standard model fails.

Another possibility for fitting the noise parameters when impact ionization is detected is to use two noise sources: one at the gate side and one on the drain side, as shown in figure 2.22. In that case, the increase of the effective temperature on the gate side was not necessary because the added white noise source models the effect that the increased gate current has on the noise figure. The optimized values of the circuit elements in this case are:

$$\begin{aligned} T_{\mathrm{d}} &= 6840\,\mathrm{K}, \\ i_{\mathrm{noise,d}} &= 407.5\,\mathrm{pA}, \\ i_{\mathrm{noise,g}} &= 1.7\,\mathrm{pA}. \end{aligned}$$

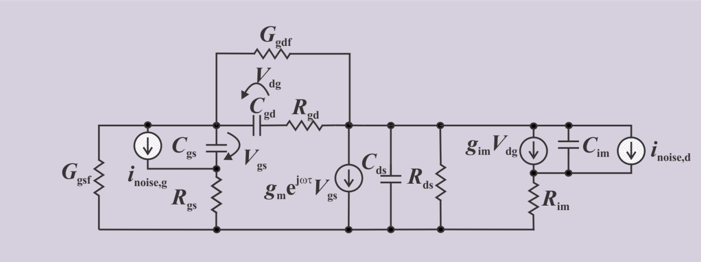
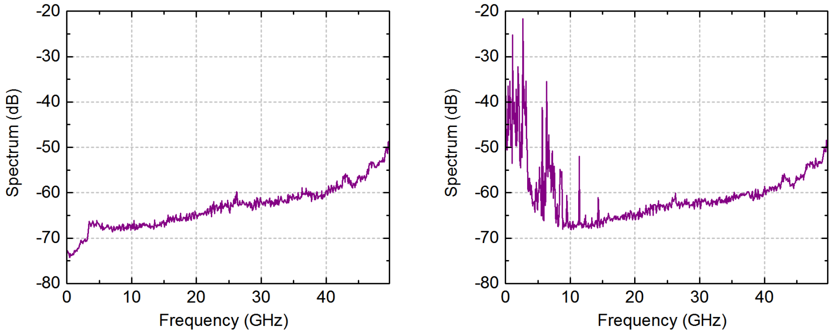


FIGURE 2.22: Intrinsic noise equivalent circuit including additional noise sources $i_{\text{noise,g}}$ and $i_{\text{noise,d}}$ modeling impact ionization added noise.

2.2.6 *Oscillations*

Unusual distortions of the I-V characteristic in GaAs FETs have been observed in 1987 [39], and similar instabilities can also appear in InP-based HEMTs [40]. Design of the state-of-the-art LNAs is thus challenging because observed distortions may prohibit achieving the ultimate low noise performance. These nondeterministic distortions, referred to as oscillations, have a detrimental influence on the noise behavior of the transistor if it is biased close to or at an unstable $V_{\text{DS}}/I_{\text{DS}}$ region. Until today a solution and a proper explanation of the origin for oscillations is lacking, while its fundamental frequency is also questionable. Some authors refer to it as *'High Frequency Oscillations'* appearing when oscillating frequency is lower than device's f_{max}, others refer to it as '*Low Frequency Dispersion*' due to harmonics appearing at low frequencies when measuring the spectrum of the biased device at unstable region. In figures 2.23a and 2.23b measurements done with a spectrum analyzer at 15 K over 0-50 GHz range are shown for an InP HEMT biased at stable and unstable region, respectively. For a HEMT biased at unstable region, pronounced harmonics are detectable at the lower part of the frequency spectrum.

Oscillations appear in the DC characteristics as steps in both drain and gate current, and consequently discontinuities in the transconductance curve as shown in figure 2.24. The drain current discontinuities can be more or less abrupt depending on the severity of dispersion, and can form a forbidden zone in which there are values of I_{DS} not accessible by static bias settings. Upon cooling InP HEMTs down to cryogenic temperatures, the issue be-



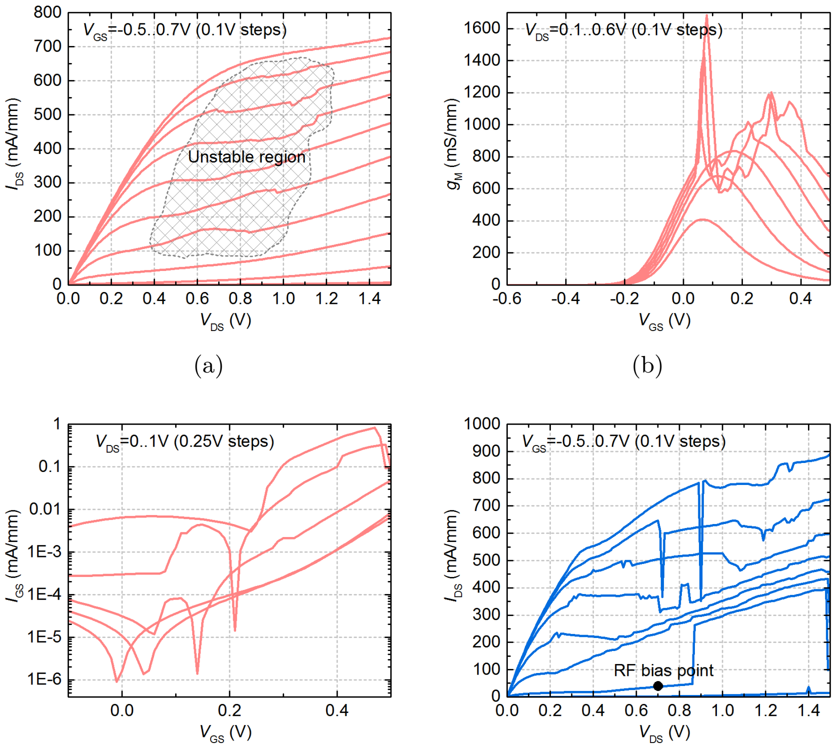
(a) (b)

Figure 2.23: Spectrum of an InP HEMT biased at a) stable and b) unstable regions measured with a spectrum analyzer at 15 K.

comes more severe; devices that were stable at room temperature can now show signs of dispersion while devices that were showing signs of oscillations at room temperature become even more unstable as shown in figure 2.24d compared to figure 2.24a.

Besides reducing the temperature, other design aspects of InP HEMTs and LNAs have also an influence on the severity of oscillations:

- With respect to device geometry, increasing the gate finger width makes dispersion more pronounced as shown in figures 2.25a for $4 \times 25\,\mu m$ and 2.25b for $4 \times 37.5\,\mu m$ HEMTs. However, there are indications suggesting that dispersion will reach a peak for certain gate width and will reduce and disappear with further increase of the width [41].
- Reducing the gate length to achieve higher cut-off frequencies also has an adverse effect as shown in figures 2.25b and 2.25c for $4 \times 37.5\,\mu m$ HEMTs with 100 nm and 250 nm gate length, respectively.
- The common approach of increasing the number of gate fingers to reduce the gate resistance and improve the noise behavior can also lead to contrary results due to appearance of unstable bias regions potentially including the optimum low noise bias point. A clear difference in stability is visible in figures 2.25b and 2.25d for $4 \times 37.5\,\mu m$ and



(a) (b)

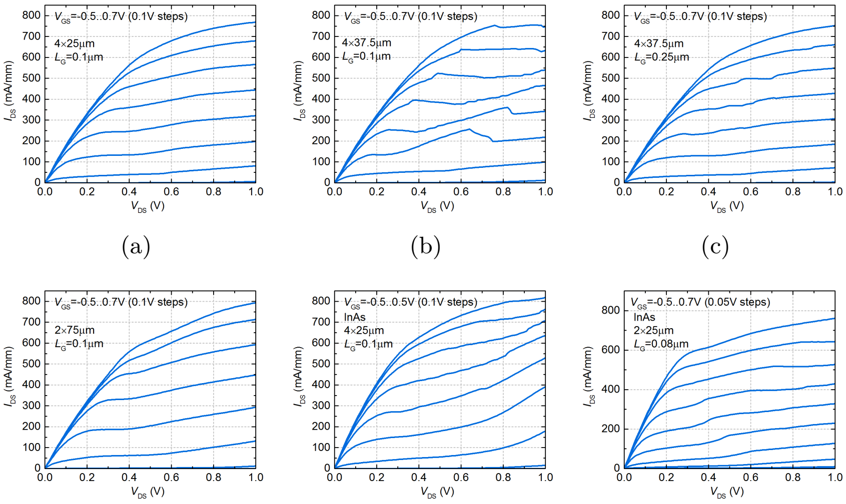
(c) (d)

FIGURE 2.24: a) Normalized DC output characteristic, b) transconductance g_M, c) gate current, all measured at 300 K and d) output characteristic measured at 15 K. Device is 4 × 50 µm HEMT with 100 nm gate length.

2 × 75 µm HEMTs although both devices have the same total width of 150 µm.

- Changing the gate-to-gate spacing has also a large influence: devices with smaller gate pitch exhibit suppressed dispersion up to some extent. However, there is a limit in reducing the gate pitch imposed by the minimum width needed for the source airbridge pad, and the minimum width of the drain finger needed to keep R_d low.

- Decreasing the channel sheet resistance or parasitic contact resistances to achieve higher gain also enhances device instabilities. Adding 1 nm of InAs in the GaInAs channel resulting in 15% decrease of the channel sheet resistance leads to appearance of dispersion as presented in figure 2.25e compared to figure 2.25a for 4 × 25 µm HEMTs.
- Vertical scaling of device epitaxial layers resulting in higher transconductance and consequently higher gain leads to more unstable behavior as shown in figure 2.25f for 2 × 25 µm HEMT with 80 nm gate length and reduced barrier and spacer thickness by 50%.



(a) (b) (c)

(d) (e) (f)

FIGURE 2.25: Normalized DC output characteristic of a) 4 × 25 µm L_G=100 nm HEMT, b) 4 × 37.5 µm L_G=100 nm HEMT, c) 4 × 37.5 µm L_G=250 nm HEMT, d) 2 × 75 µm L_G=100 nm HEMT, e) 4 × 25 µm L_G=100 nm HEMT with 1 nm InAs in the channel and f) 2 × 25 µm L_G=80 nm HEMT with reduced barrier and spacer thickness, all measured at 15 K.

In addition, depending on the input impedance presented to the device during measurement, dispersion is also more or less pronounced suggesting that for the design of LNA there might be an optimal matching in order to reduce the oscillation behavior.

S-parameters measured when the device is biased close or in the unstable region show anomalous behavior including spikes, ripples, and values of S_{11} and S_{22} larger than 1 (0 dB). For a bias point depicted in figure 2.24d measured S-parameters are presented in figure 2.26. Unstable S-parameters can not be reproduced by our basic or extended small-signal model since device behavior diverges from the proposed model.

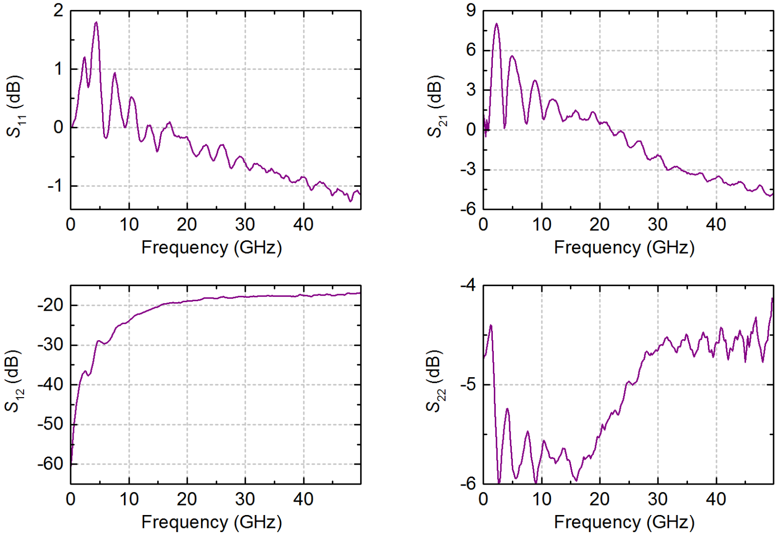


FIGURE 2.26: S-parameters of a device measured at 15 K and biased at the unstable point depicted in figure 2.24d.

For 100 nm gate length HEMTs fabricated on our standard epitaxial layer, described in section 3.1, two-finger devices with gate widths above 150 µm are very difficult to bias at a stable region and use at cryogenic temperatures. Four- and six-finger HEMTs are unstable at 15 K starting from gate widths of 30 and 17 µm, respectively.

To suppress the instabilities and have a reliable and reproducible LNA performance, several solutions have been tested including changes in device geometry by increasing the width of the source airbrigde, changing its position, adding gate and drain air bridges [40] etc. Most effective seem to be adding source airbridge on two-finger devices, tying the gate ends together, increasing the gate resistance [41] and adding drain airbridge on four-finger device [42]. However, all proposed solutions have been implemented for one specific device type (gate width and length) and more investigation is needed to confirm whether the solution is reproducible and complete.

3

HEMT FABRICATION

3.1 EPITAXIAL LAYER DESIGN

3.1.1 *Introduction*

The epitaxial layers used to fabricate HEMTs described in this work were grown on 2-inch Fe-doped InP substrates by Molecular Beam Epitaxy (MBE) in the ETH FIRST Laboratory. The basic layers forming the InP HEMT heterostructure were presented in section 2.1, and a more detailed structure with layer composition and thicknesses is shown in figure 3.1.

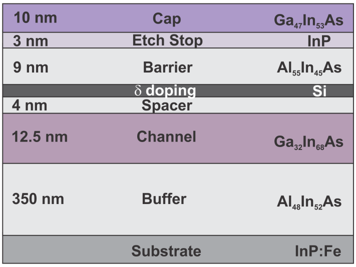


FIGURE 3.1: Typical epitaxial layer structure of the InP HEMTs investigated in this work.

Epitaxial layers depicted in figure 3.1 are referred to as "standard structure" and used as a reference layer throughout this work. The standard structure was adopted from [43] where the layers were purchased from IQE, while in this work they were grown *in-house* featuring similar properties and performance. The layers are described in detail below in the growth direction (from the substrate up).

3.1.2 *Description of the HEMT Epitaxial Layers*

BUFFER

An undoped lattice matched $Al_{0.48}In_{0.52}As$ buffer is grown on top of the semi-insulating Fe-doped InP substrate in order to move the active layers away from the substrate and substrate/epilayer interface. A wide bandgap buffer layer lowers inherent electron injection, thereby reducing buffer leakage current, and improves carrier confinement in the channel as described in section 2.1. With respect to layer thickness, thinner buffer layer has an advantage in terms of device self-heating, while thicker layers provide a smooth surface for the subsequent channel growth, avoiding roughness scattering at the buffer/channel junction maintaining electron mobility of the 2DEG as high as possible. Furthermore, a thick buffer alleviates undesirable effects coming from the substrate interface, such as impurity migration, and depletion of the 2DEG by traps on the surface or incorporated in the substrate causing a parasitic leakage path between the source and drain.

To investigate optimum buffer thickness, three HEMT structures were grown with 50, 150 and 350 nm buffer thicknesses and identical top layers. Based on the thermal resistance model of GaN HEMT presented in [44], using $k_{\mathrm{AlInAs}} = 6.4\,\mathrm{W/K{\cdot}m}$ and $k_{\mathrm{InP}} = 68\,\mathrm{W/K{\cdot}m}$ for thermal conductivities of AlInAs and InP, it can be estimated that thermal resistance of a multi-finger InP HEMT with gate width of 50 µm, gate length of 100 nm and gate-to-gate spacing of 20 µm is lowered by approximately 60% for buffer thickness of 50 nm, and by 25% for buffer thickness of 150 nm compared to 350 nm. Indicated decrease in thermal resistance could be beneficial for further improving transistor noise behavior. However, Hall measurements on these structures featuring the same δ-doping show significant loss of sheet carrier density and carrier mobility for the thinner buffer structures. Devices processed on thinner buffer structures measured both at room temperature and 15 K feature lower drain current, lower transconductance, lower cut-off frequency, lower $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio and higher gate leakage due to parasitic leakage path formed on the interface with the substrate. Obtained degradation in performance was detrimental for noise behavior and thereby hindered evaluation of self-heating on the minimum noise figure. Therefore, for all subsequent grown epitaxial layers the buffer thickness is set to 350 nm.

CHANNEL

Following the buffer, a 12.5 nm channel is grown consisting of strained $Ga_{0.32}In_{0.68}As$ for standard structure as shown in figure 3.1. As stated in section 2.1, a narrow bandgap semiconductor should be chosen for channel material in order to increase the conduction band offset and carrier confinement, along with providing low electron effective mass to improve carrier mobility. The channel thickness is selected by taking into account several factors:

- Strain induced layer relaxation if the critical thickness is exceeded,
- Loss of carrier confinement for thicker channels,
- Reduced mobility as a result of scattering with channel/buffer and channel/spacer interfaces for thinner channels.

InP HEMTs with high In content in the channel (>53%) provide advantages in terms of maximum transconductance g_m, cut-off frequency f_T and minimum noise figure F_min [25] with a cost of having more pronounced impact ionization and lower breakdown voltage. Optimization strategies for the channel layer presented in Chapter 4 include increase of the In content, adding InAs insets and using composite GaInAs/InP or GaInAs/InPAs/InP channels to reduce impact ionization.

SPACER AND BARRIER

For the spacer and top barrier layers, strained AlInAs with increased Al content to 55% is chosen to increase the Schottky barrier height and decrease the gate leakage current to achieve a good noise performance [45] [46]. For the standard structure, the total thickness of barrier and spacer is set to 13 nm in order to provide good pinch-off for the 100 nm gate length devices [43]. The position of the Si δ-doping plane within AlInAs layer, as well as the doping level, is selected with respect to minimizing the leakage current and maximizing sheet carrier density and mobility. While gate leakage current is reduced by increasing the barrier thickness, the transistor transconductance and gain are deteriorated. In order to have high sheet carrier density, the thickness of the spacer layer should be kept at a minimal value. On the other hand, proximity of the ionized donors in that case reduces carrier mobility. For 100 nm gate length devices optimized thicknesses of the barrier and spacer are therefore set to 9 nm and 4 nm respectively, while for sub-100 nm gate length devices they are set to 4 nm and 2 nm.

INP ETCH STOP

The AlInAs barrier layer surface depicted in figure 3.1 is very sensitive and if it is exposed to atmosphere during the device process flow Al is likely to form a native oxide Al_2O_3. Due to the uncontrolled formation of this native oxide, device fabrication lacks repeatability and devices can suffer performance degradation. A thin InP layer added to AlInAs/GaInAs/InP heterostructures has a lesser degree of oxidation than used ternary materials [47]. Therefore, having a 3 nm layer of InP as the etch stop layer, besides allowing selective etching of the GaInAs cap with respect to the barrier, is enough to protect sensitive Al-rich AlInAs surface from oxidation [48]. InP also passivates the deep level defects on AlInAs surface incorporated during the growth thereby reducing the kink effect [49].

HIGHLY DOPED CAP

To achieve a good device performance in terms of high gain and minimum noise figure, besides improving the channel transport properties, special attention needs to be attributed to reduction of the parasitic resistances of source and drain Ohmic contacts [50]. Taking into account that targeted application of InP HEMT is at cryogenic temperatures, dominant mechanism for current transport through the Ohmic contact should be tunneling, which is temperature independent, as oppose to thermionic emission where the contact resistance will increase with decrease of the temperature. To raise the probability of tunneling and the tunneling current through the contact, a highly n-doped capping layer is needed underneath the source and drain metalization. Most commonly used cap layers are lattice matched $Ga_{0.47}In_{0.53}As$ as is the case for our standard structure, strained GaInAs with 68% or 75% In content, graded $Ga_{1\text{-}x}In_xAs$, or composite GaInAs/AlInAs layer designed for non-annealed contacts [51]. Along the course of this work cap doping was limited by the capabilities of MBE machine, and it has always been set to the maximum achievable level in order to further reduce the contact resistance. In Chapter 4 a comparison of two different cap doping levels on device performance is shown. For our standard structure the cap doping is set to $3 \cdot 10^{19}\,\mathrm{cm}^{-3}$.

3.2 DEVICE PROCESS FLOW

3.2.1 *Overview*

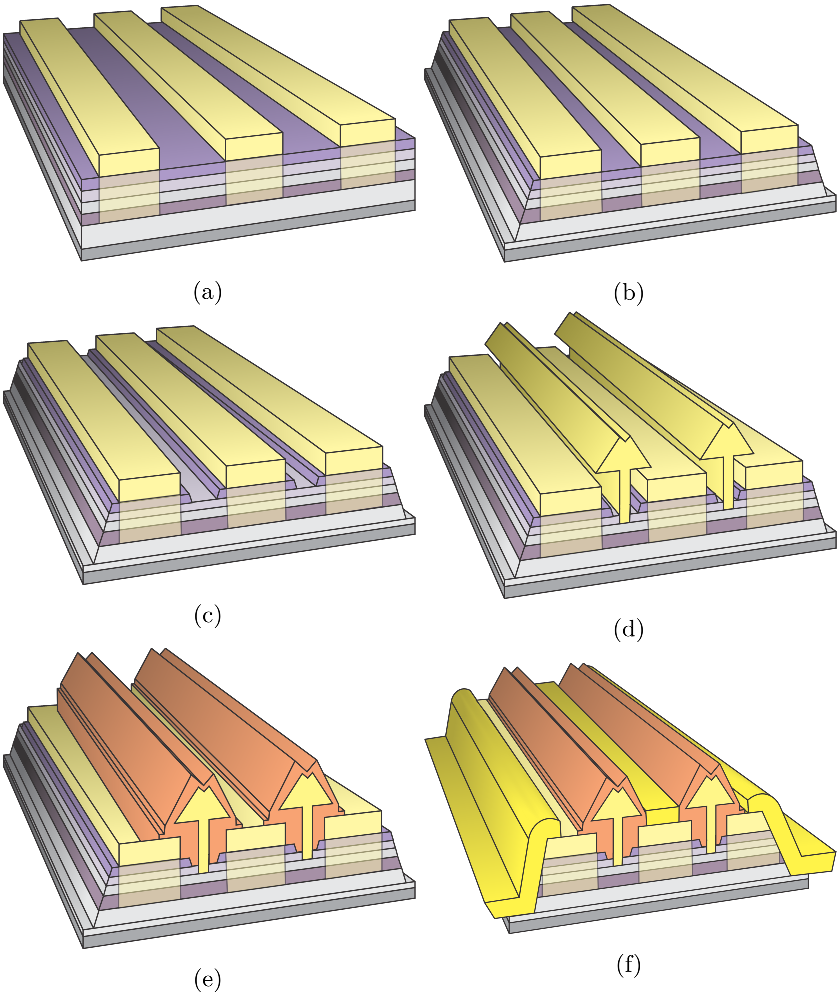
Fabrication of low-noise InP HEMTs requires eight major steps, each consisting of several substeps e.g. sample cleaning, optical or electron beam lithography, metal deposition, and wet or dry etching. The conventional process flow, from epilayer growth to a finished device, consists of:

- Cleaving and characterization,
- Ohmic contact formation,
- Mesa isolation,
- Recess etching,
- Gate contact formation,
- Active area passivation,
- Overlay metallization,
- Air-bridge metallization for multi-finger devices,

and it is illustrated in figure 3.2. For some special cases described in Chapter 4, mesa isolation and recess etching step are performed in reverse order due to the selectivity and etch rate of the selected etching solution.

3.2.2 *Cleaving and Characterization*

For the first step of device fabrication, MBE grown wafer is cleaved and a preliminary characterization is performed. Hall measurements using the Van der Pauw method are carried out to measure channel sheet carrier density and electron mobility at room temperature and 77 K. Samples used for characterization have annealed InZn contacts, with the cap layer removed after annealing of the contacts using the same etching procedure as for real devices to ensure stable and comparable results. The standard structure yields a sheet carrier density of $n_s = 1.5 \cdot 10^{12}\,\mathrm{cm}^{-2}$ and an electron mobility $\mu_n = 11900\,\mathrm{cm}^2/\mathrm{V{\cdot}s}$ at room temperature, and $n_s = 2 \cdot 10^{12}\,\mathrm{cm}^{-2}$ and $\mu_n = 30800\,\mathrm{cm}^2/\mathrm{V{\cdot}s}$ at 77 K. Hall measurements for other analyzed epitaxial layers are summarized in Chapter 4.



(a) (b) (c) (d) (e) (f)

FIGURE 3.2: Schematic representation of the InP HEMT process. a) 3D view of device active area after Ohmic contact formation, b) after device isolation etching, c) after gate recess etching, d) after gate metal deposition and gate sink-in, e) after device passivation and f) after overlay metalization.

3.2.3 *Ohmic Contact Formation*

Exceptional HEMT performance can only be achieved with minimum source and drain access resistances R_s and R_d. Their reduction, specifically of the principal contributor – the Ohmic contact resistance, plays a key role in HEMT fabrication. Two main components of R_s and R_d can be distinguished: the contact resistance R_C from metal to the channel, and the sheet resistance of the 2DEG in the channel, R_sheet, in different device areas.

R_sheet is mostly determined by epitaxial layer design, namely the mobility and the sheet carrier density of the 2DEG, and it can for example be altered by adjusting the In content of the channel or by changing Si δ-doping density. Taking into account that the device channel is positioned relatively shallow, the 2DEG properties can also be very sensitive to any process steps that create defect states on the semiconductor surface. R_C on the other hand, is mainly defined by fabrication procedure i.e. the choice of metal layer stack, the interface cleanliness, the qualitative formation of the tunnel contact, and exposure to high temperature steps in case the contact is annealed. For a more accurate model, R_s and R_d can be separated into several components as illustrated in figure 3.3 [52]: the resistance between metal and cap layer ($R_\mathrm{C,cap}$), the resistance to the 2DEG ($R_\mathrm{C,2DEG}$), the sheet resistance of the cap layer ($R_\mathrm{sheet,cap}$), the sheet resistance of the 2DEG (R_sheet) and the resistance of the barrier (R_AlInAs). The sheet resistance of the metal layer, $R_\mathrm{sheet,met}$, is very small, so its influence on access resistances was omitted. For structures where the Ohmic contact is determined mainly by direct contact between metal and channel, i.e. annealed contacts, conduction through the cap and barrier layer can be neglected. However, this is not the case for non-annealed contacts where the contact from source and drain to the channel is determined mainly by electrons tunneling from the edges of the cap layer adjacent to the recessed area.

Besides proper choice and optimization of fabrication steps, contact resistance can be also improved by adjusting the epitaxial design. Namely $R_\mathrm{C,cap}$ and $R_\mathrm{sheet,cap}$ benefit from an increase in cap doping level as mentioned in paragraph Highly Doped Cap, $R_\mathrm{C,cap}$ can be improved by reducing the barrier height between cap and metal with the increase of cap's In content, and resistance of the barrier R_AlInAs can be reduced by increasing the doping of the channel or by reducing the barrier thickness.

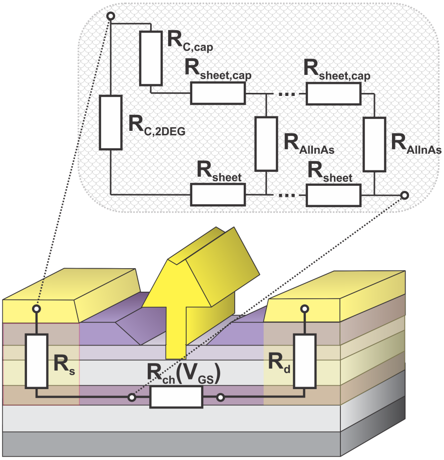


FIGURE 3.3: Distributed resistance model as introduced by [52].

The Ohmic source and drain contacts are formed with cleaning the cleaved sample, patterning via optical lithography, removing the native oxide by *in-situ* low-energy Ar sputtering, and depositing a Ge/Au/Ni/Au layer stack [43] in an electron-beam evaporator. Metal lift-off is performed using a strong resist remover heated to a high temperature to ensure no resist residuals are left on the semiconductor surface. These residuals can later lead to formation of connections between source and drain contacts as explained in section 3.2.5. However, strong resist removers can easily promote electrochemical etching of semiconductor layers adjacent to metal stacks and degrade the contact resistance [53]. Therefore, in order to ensure minimum parasitic resistances, duration and temperature of the process are limited. After the metal lift-off, contacts are annealed in a Rapid Thermal Annealer (RTA) at a temperature of approximately 290°C in order to diffuse GeAu compound into the semiconductor and contact the 2DEG channel layer. Diffused Ge acts like a donor, forming a thin highly doped region between the channel and cap layer as desired for a tunnel contact. The annealing process is performed under high flow rate of forming gas, $5\%\,H_2 : 95\%\,N_2$, to ensure minimal oxidation of metal layers at elevated temperatures and consequential degradation of the contact resistance. Figure 3.2a illustrates the Ohmic contact formation.

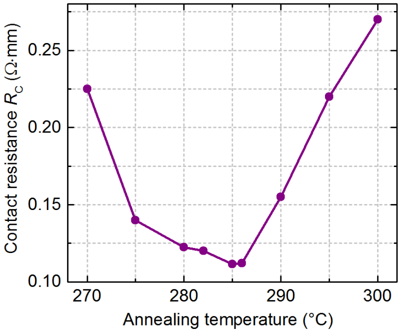
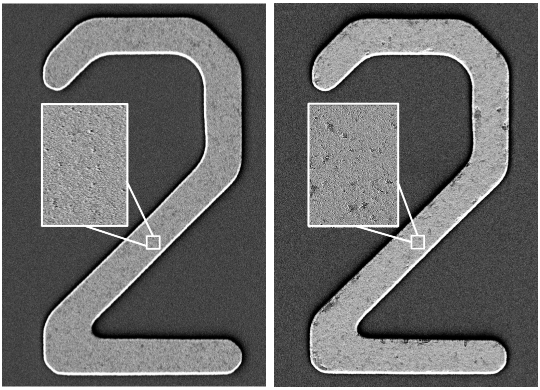


FIG. 3.4: Extracted R_C versus annealing temperature for standard structure.

Because of the sensitivity of R_C towards annealing conditions, annealing temperature calibration is performed for each epitaxial layer in order to find the optimum giving the minimum achievable contact resistance. Temperature calibration is performed on standard TLM structures with spacings ranging from 2 to 10 µm, fabricated using optical lithography, and measured via four-point resistivity measurement on the needle prober at room temperature. The annealing time is set to 60 seconds [43], and the annealing temperature is swept until a clear minimum is visible in extracted contact resistance as shown in figure 3.4 for the calibration of the standard structure. Once the optimal annealing conditions are identified, they are used for final device fabrication.

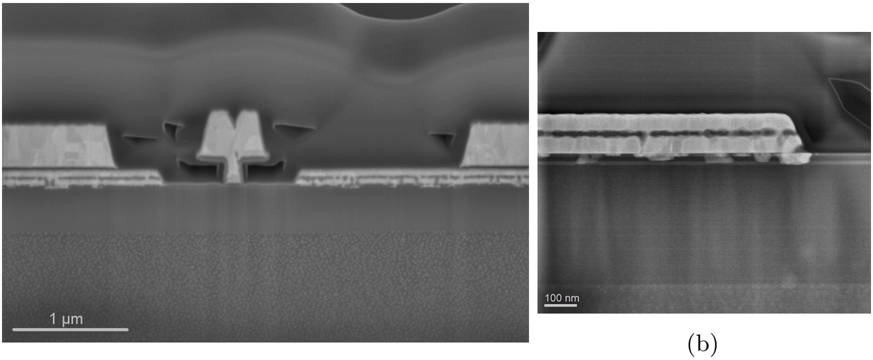
By comparing the images of measured TLM structures acquired by Scanning Electron Microscopy (SEM) it was observed that the metal stack roughness for optimum temperature is higher compared to non-annealed or low-temperature annealed stacks, with hole-like structures appearing at the surface, as depicted in figure 3.5a. Furthermore, by raising the temperature beyond optimal, the hole structures broadened and their density increased as presented in figure 3.5b. The observed behavior is consistent with the extracted contact resistance exhibiting a clear minimum versus temperature: if the annealing temperature is too low, Ge does not penetrate deep enough into the semiconductor and it is not significantly contacting the channel layer. On the other hand, if the annealing temperature is too high, Ge diffuses below the channel layer, interrupting the contact with the top metalization layers, resulting in increased resistance. High-resolution cross-sectional Scanning Transmission Electron Microscopy (STEM) analysis was performed on a device annealed at optimum temperature to confirm that the optimum requires AuGe contacting the channel layer and not sinking deeper, as shown in figures 3.6a and 3.6b. To investigate the composition of the alloy diffusing towards the channel, as visible in figure 3.6, Energy



(a) (b)

Figure 3.5: SEM image of a 20 µm long structures with Ohmic metalization a) annealed at optimum temperature corresponding to minimum resistance and b) annealed at elevated temperature by 5°C.

Dispersive X-ray Spectroscopy (EDS) was performed. The EDS identified the metal alloy sinking to the channel as the AuGe compound.



(a) (b)

Figure 3.6: a) Cross-sectional STEM image of an InP HEMT and b) zoomed-in Ohmic metal region.

3.2.4 *Device Isolation*

Isolation between different devices shown in figure 3.2b is implemented with resist patterning using optical lithography, followed by removing of conductive layers via wet etching. An etch depth of approximately 120 nm is found to be sufficiently deep, providing a resistance between two neighboring devices in $10^9\,\Omega$ range.

For the standard epitaxial layer structure, the GaInAs cap and channel layers together with the AlInAs barrier, spacer and buffer layers are etched using a solution based on phosphoric acid (H_3PO_4:H_2O_2:H_2O). For layers with a GaInAs/AlInAs composite cap GaInAs and AlInAs layers are etched using a solution based on citric acid ($C_6H_8O_7$:H_2O_2:H_2O) in order to achieve smooth isolation edge required for T-gate process. InP layers, including etch stop and backchannel, are removed with a hydrochloric acid based solution (HCl:H_2O).

After reaching the final etch depth required for isolation, a selective succinic acid based solution ($(CH_2)_2(CO_2H)_2$:H_2O_2:H_2O), is used to laterally etch into the GaInAs channel layer to prevent a direct contact between the gate electrode and the channel [54] and to reduce the mesa sidewall leakage as shown in figure 3.7.

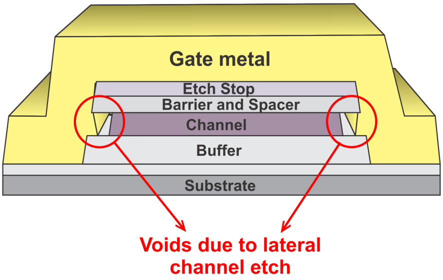


FIG. 3.7: Schematic cross-section of gate metalization over the mesa slope.

3.2.5 *Recess Etching*

To prevent a short circuit between gate and source/drain contacts, and to reduce gate leakage current, the conductive GaInAs cap layer has to be completely removed underneath the gate contact, as depicted in figure 3.2c. Particles or resist residuals, specifically hardened leftovers from the Ohmic metal lift-off and subsequent annealing, are difficult to remove and can result in short-circuits between the source, drain and gate contacts as shown in figure 3.8. Any cap residuals underneath the gate, even when not short-circuiting the contacts, will result in deteriorated Schottky contact and inferior control over the channel. Therefore for high-performance HEMTs, the gate recess represents one of the most important steps of the process flow.

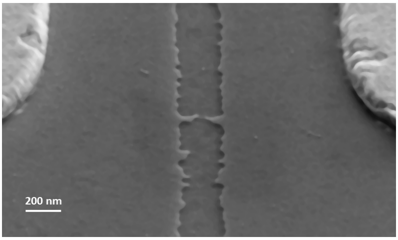


Fig. 3.8: SEM picture of the gate recess with not etched material connecting source and drain.

The area which to be recessed is defined by electron-beam lithography, and the GaInAs layer is removed via wet etching with a highly selective solution based on succinic acid. For the GaInAs/AlInAs composite cap, recess is performed in solution based on citric acid. Owing to the gate contact also defined by electron-beam lithography, a minimum recess width required to prevent a direct contact between the gate and GaInAs layer exists and is defined by electron-beam lithography alignment precision. With procedure proposed in [43] the alignment error is reduced to approximately 20 nm. However, in order to decrease the probability of partial bridge of non-etched material shortening the gate and one of the Ohmic contacts, the minimum recess width for our reliable and repeatable process is set to 50 nm on each side of the gate contact.

The area exposed by etching contains large amounts of surface traps which can significantly deplete the 2DEG due to the proximity of the surface to the intrinsic transistor and consequently degrade the gate control over the channel. These defects on the surface can only be partially neutralized with a proper choice of passivation layer. Therefore, even with the entire cap perfectly removed under the gate contact, the width of the recessed area has a strong influence on device DC and RF performance. Wider recess decreases the gate leakage current and parasitic capacitance between gate and drain C_{gd}, while devices with narrower recesses feature a lower contact resistance, higher transconductance and have less pronounced kink-effect due to smaller area with with surface traps incorporated during etching [55]. In order to optimize the gate recess width for good noise performance, 100 nm gate length devices with total recess widths from 200 nm to 350 nm were processed on standard structure of commercial material purchased from IQE. Parameters of their performance were compared and summarized in table 3.1.

L_{rec} (nm)	I_{GS} (µA/mm)	g_{Mmax} (mS/mm)	NIF_{min} ($\sqrt{\text{mm}\cdot\text{mA}}/\text{S}$)	$f_{\text{T,max}}$ (GHz)	C_{gd};C_{gs} (fF/mm)	R_{s};R_{d} (mΩ·mm)	g_{m} (mS/mm)
200	-3.7	1259	9.67	259	203;648	224;256	1325
250	-3.2	1240	9.79	253	187;652	240;272	1320
300	-2.2	1225	9.82	247	177;708	248;280	1320
350	-1.9	1203	9.94	241	163;739	256;288	1322

TABLE 3.1: Comparison of device performance versus gate recess width at room temperature.

Table 3.1 compares several figures-of-merit together with SSEC elements which are extracted close to low-noise bias point for $2 \times 40\,\mu\text{m}$ devices measured at room temperature:

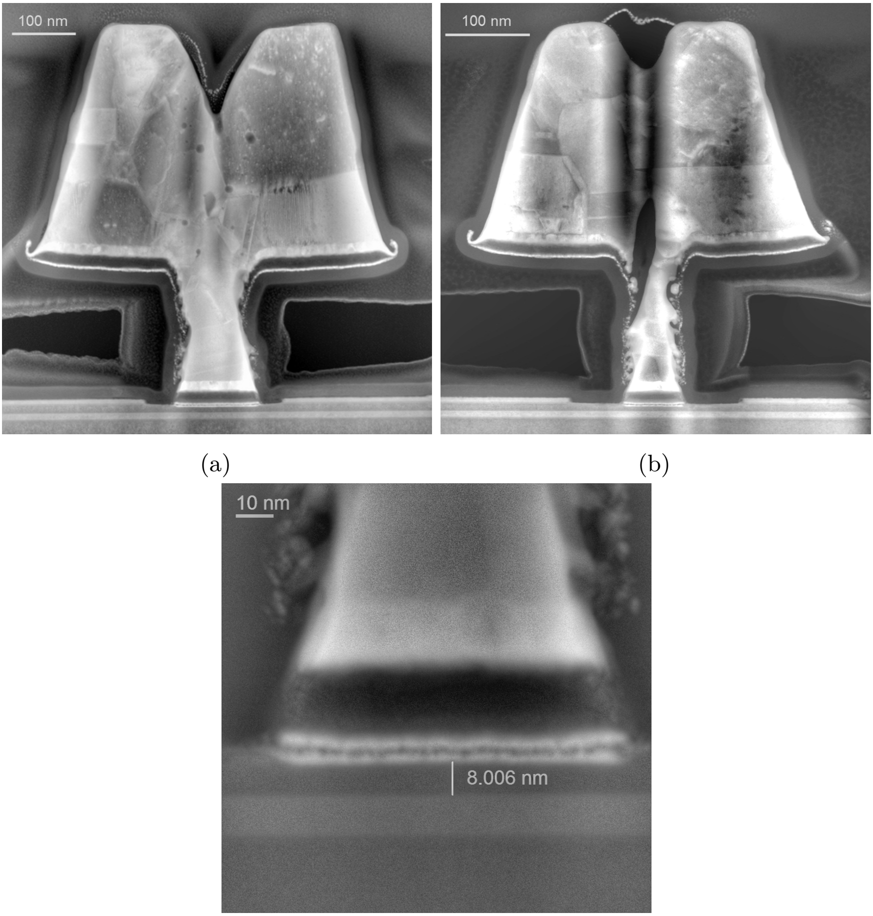
- Normalized gate leakage current measured at $V_{\text{GS}} = -1\,\text{V}$ $V_{\text{DS}} = 0\,\text{V}$,
- Normalized maximum DC transconductance,
- Normalized noise indication factor as defined in section 2.2.5,
- Maximum deembedded cut-off frequency,
- Normalized gate-to-drain and gate-to-source capacitances,
- Normalized source and drain resistances,
- Normalized small signal transconductance.

To maximize the cut-off frequency and minimize the gate leakage current, the optimum gate recess width suggested in [56] was quite large compared to the size of the gate footprint: 260 nm for 30 nm gate foot. From the results shown in table 3.1, gate current on our standard structure was not significantly reduced for recess width of 350 nm versus 200 nm, while maximum transconductance and noise indication factors were reduced, and, contrary to the finding from [56], cut-off frequency was decreased. According to the expression for f_T (equation 2.14), and analyzing the values of the extracted SSEC for our material, it can be noticed that the change in gate-to-drain capacitance is much smaller than reported in [56], and consequently degradation of f_T with wider recess is observed due to decreased g_m, increased parasitic resistances R_s and R_d and increased C_gs.

Gate leakage could be decreased even further with widening the recess above 350 nm, however its value was at acceptable level both at room and cryo temperatures for good noise performance [1]. Measurements at 15 K reflect similar trends as at room temperature. Therefore, in choosing the most appropriate recess width, more significance was attributed to noise indication factor and transconductance, settling the optimum to 200 and 180 nm for 100 and 80 nm gate lengths, respectively.

3.2.6 *Gate Contact Formation*

Following gate recess, the gate contact is defined in a two-step electron-beam lithography process followed by electron-beam evaporation of Pt/Ti/Pt/Au metal stack. The T-shaped gates are implemented featuring a low gate resistance for better noise performance. In this work, gate footprints are 80 nm and 100 nm, whereas the gate head widths are 500 nm and 600 nm respectively. Gate stem has a typical height of 200 nm, with the height of the gate head of 400 nm. Before the gate metal deposition, a resist reflow performed in RTA at 130°C is necessary to change the negative flanks of developed resist and improve mechanical attachment of the large gate head with the small foot. An STEM image of a 100 nm gate is depicted in figure 3.9a. For small gate foot lengths, below 100 nm, the metal deposition rate and the resist reflow have a large influence on the homogeneity gate metal stack. Because of the narrow resist opening for the smaller gate lengths and positive resist flanks after the resist reflow, high metal deposition rates result in non-uniform metal stack. In figure 3.9b an STEM image is presented for a 50 nm gate foot, showing a 'hole' spreading through the gate stem and head. The hole structure is not constant throughout the total gate width, its position is shifting, and the width is varying. The EDS was performed, and has identified the composition of the hole structure to be the Al_2O_3 form the device passivation step. Although no anomalies were found in the measurements of devices with holes in the gates, the deposition rate for the sub-100 nm gates is lowered ensuring a uniform metal layer stack.



(a) (b)

(c)

FIGURE 3.9: Cross-sectional STEM image of a Pt/Ti/Pt/Au gate with gate foot length of a) 100 nm, b) 50 nm and c) zoomed-in image of the gate foot region.

In terms of noise performance, gate leakage current is an important figure-of-merit [46]. For low-noise HEMTs Schottky gate contacts are used, with large barrier heights, which result in a very low current. Pt as the gate contact metal allows vertical device scaling with the possibility of controlled Pt diffusion through InP etch stop and into the AlInAs barrier while at the same time keeping the gate leakage low due to high Schottky barrier of Pt on AlInAs [57] [58] [59]. Besides annealing time and temperature, atmosphere and thermal ramp rate also play a key role in Pt diffusion [60]. To achieve a fully sunken-in gate, after the gate metal lift-off, devices are annealed at 250°C in 5% $H_2 : 95\% N_2$ atmosphere in RTA with a high thermal ramp rate. Gate contact formation is illustrated in figure 3.2d. A zoomed-in STEM image of a 100 nm gate foot is depicted in figure 3.9c with a measured gate-to-channel distance of 8 nm. With a total barrier and spacer thickness of 13 nm, Pt is controllably and uniformly penetrated 5 nm into the barrier.

3.2.7 *Active Area Passivation*

In order to stabilize the T-gate mechanically and prevent degradation of device performance by suppressing the impact of surface traps incorporated by recess etching, the active region between source and drain is passivated with Al_2O_3 deposited by Atomic Layer Deposition (ALD) as shown in figure 3.2e. Al_2O_3 is reported as a viable and superior alternative to previously used Si_3N_4 due to improved film coverage and film uniformity, even at relatively low deposition temperature of 180°C, together with better control of growth thickness [61]. Devices passivated with Al_2O_3 exhibit better DC, RF and noise behavior [61] [43]. Al_2O_3 film quality can be improved by increasing the deposition temperature allowing reduction of film thickness and improving the RF performance and potentially also combining the gate sink-in and gate passivation step in one. However, with increase from 180 to 250°C, due to the thermal budget of the deposition process, Ohmics contacts degrade even though the selected temperature is below the annealing point [60].

The 25 nm thick Al_2O_3 is deposited on the whole chip at 180°C, followed by patterning by optical lithography and Al_2O_3 removal outside of device active area. Al_2O_3 is etched back with Reactive Ion Etching (RIE) with a Tetrafuloromethane (CF_4) based etch process.

3.2.8 *Overlay Metalization*

Probing pads are formed by optical lithography, followed by deposition of a thick Ti/Au overlay metallization via electron-beam evaporation as shown is figure 3.2f. After the metal lift-off, two-finger devices are ready for measurement and performance evaluation. Figure 3.10 shows the top view of the finished two-finger InP HEMT. The highlighted area corresponds to the section used to demonstrate the process flow depicted in figure 3.2.

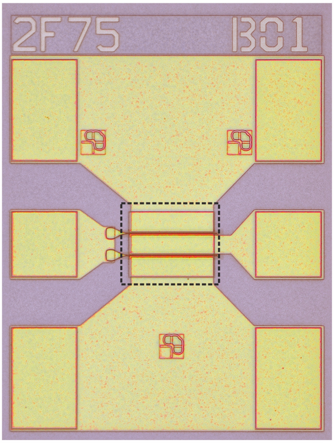


FIGURE 3.10: Optical microscope image of a $2 \times 75\,\mu m$ InP HEMT. The dashed section corresponds to the transistor active area demonstrating the process flow shown in figure 3.2.

3.2.9 *Air Bridge Metalization*

For multi-finger devices, air bridges formed by electroplated Au are necessary to electrically connect all source fingers and source probing pads. The air bridges are formed in a two-step lithography process: the first step is used to define electroplated areas that contact the overlay metalization, and second step defines areas where the Au will be electroplated. SEM image of a finished six-finger HEMT is depicted in figure 3.11.

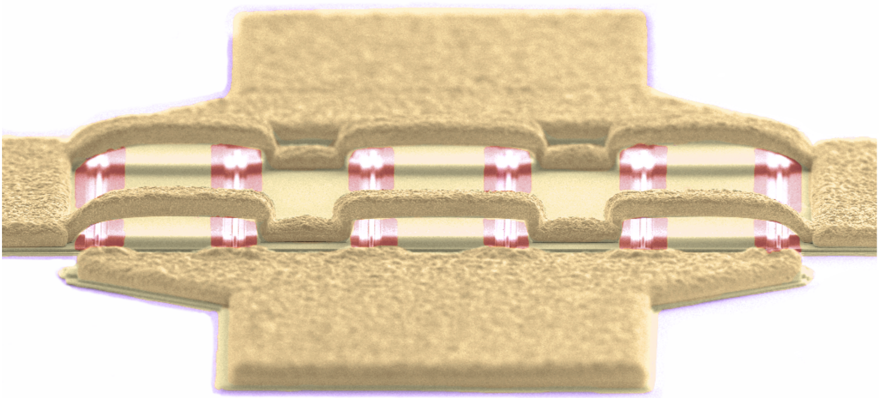


FIGURE 3.11: Colored SEM picture of a finished six-finger HEMT with air bridges contacting the source fingers and pads.

4

EPITAXIAL LAYER OPTIMIZATIONS

4.1 INTRODUCTION

Progress achieved in the RF and noise performance of InP HEMTs over the last few decades came as a result of the minimization of parasitic resistances and the maximization of intrinsic cut-off and maximum oscillation frequencies (f_{T} and $f_{\max}$). Both the reduction of parasitics and the increase of bandwidth were addressed by improvements of epitaxial layer structure or by transistor vertical and lateral scalings.

Modifications of the epitaxial layers usually include improvements of the carrier transfer properties and confinement. This is achieved by increasing the In content of $\mathrm{Ga}_{1-x}\mathrm{In}_x\mathrm{As}$ channel to $x > 68\%$ and above, or by introducing the InAs channel insets. As a consequence of the lattice constant mismatch between the InAs channel and the InP substrate (6.04 A lattice constant for InAs compared to 5.86 A for InP), its inclusion in the channel introduces uncompensated strain in the structure. Strain can lead to undesirable 3D growth and layer relaxation, therefore the maximum thickness of InAs layer is limited.

The parasitic resistances of the source and drain contacts are also reduced by suitable epitaxial layer adjustments, for instance by employing the highly-doped GaInAs or composite GaInAs/AlInAs cap layers.

The scaling of the transistor's vertical dimensions increases the device transconductance g_{m}, but at a cost of having higher gate leakage deteriorating the noise performance and higher gate-to-source capacitance C_{gs}. Higher g_{m} should result in higher f_{T} and $f_{\max}$, however this is suppressed because of the increase in C_{gs}. On the other hand, vertical scaling of the device dimensions allows a reduction of the gate foot length while still providing a good pinch-off [62]. The shorter foot length will reduce the C_{gs}, and is consequently followed by a rise of the f_{T} and $f_{\max}$.

The scaling of the transistor's lateral dimensions includes a decrease of the source-drain spacing resulting in lower access resistances R_{s} and R_{d}.

The main focus of this chapter are the optimizations of epitaxial layers to reduce the influence of impact ionization, the optimization of the cap layer in order to reduce the source and drain resistances and the optimization of the channel layer for vertically scaled HEMTs. The energy bandgaps of different semiconductor materials referenced in this chapter are summarized in table 4.1 [63] [64].

Material	**Bandgap (eV)**
InP	1.344
InAs	0.354
$Al_{0.48}In_{0.52}As$	1.543
$Al_{0.55}In_{0.45}As$	1.725
$Ga_{0.47}In_{0.53}As$	0.774
$Ga_{0.32}In_{0.68}As$	0.621
$Ga_{0.25}In_{0.75}As$	0.556
$InP_{0.37}As_{0.63}$	0.726

TABLE 4.1: Summary of the energy bandgaps for materials used for HEMT epitaxial layer optimization.

4.2 COMPOSITE GAINAS/INP CHANNEL

The $Ga_{0.47}In_{0.53}As$ channel has excellent transport properties, such as low electron effective mass and high saturation velocity, but suffers from high impact ionization rates in strong electric fields. Further increase of the In concentration in the channel to 68% and above, or addition of InAs channel insets, results in manifestation of impact ionization even at a relatively low drain voltage of $V_{DS} = 0.5\,V$. Additional noise generated by impact ionization is detrimental for device's performance as shown in section 2.2.5.2. Therefore, as a promising alternative, a composite GaInAs/InP [65] [66] channel is implemented according to figure 4.1.

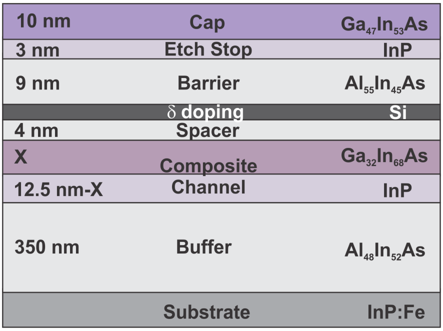


FIGURE 4.1: Epitaxial layer structure used to optimize the GaInAs/InP composite channel.

InP has good transport properties and lower impact ionization rate at high electric fields, with a drawback of having lower electron mobility. The composite GaInAs/InP channel merges the advantages of both materials: at lower fields, electrons are in the GaInAs channel at the source side of the device with superior transport properties, whereas at higher fields electrons are transferred into the InP backchannel at the drain side of the device with reduced impact ionization rate. To lower the impact ionization rate, the InP thickness should be as large as possible, taking care that the excellent channel transport properties at lower electric field are not compromised.

To investigate the optimum GaInAs/InP thickness ratio, four structures were grown and processed side-by-side in the standard process flow described in Chapter 3.

Epitaxial layers used for comparison were:

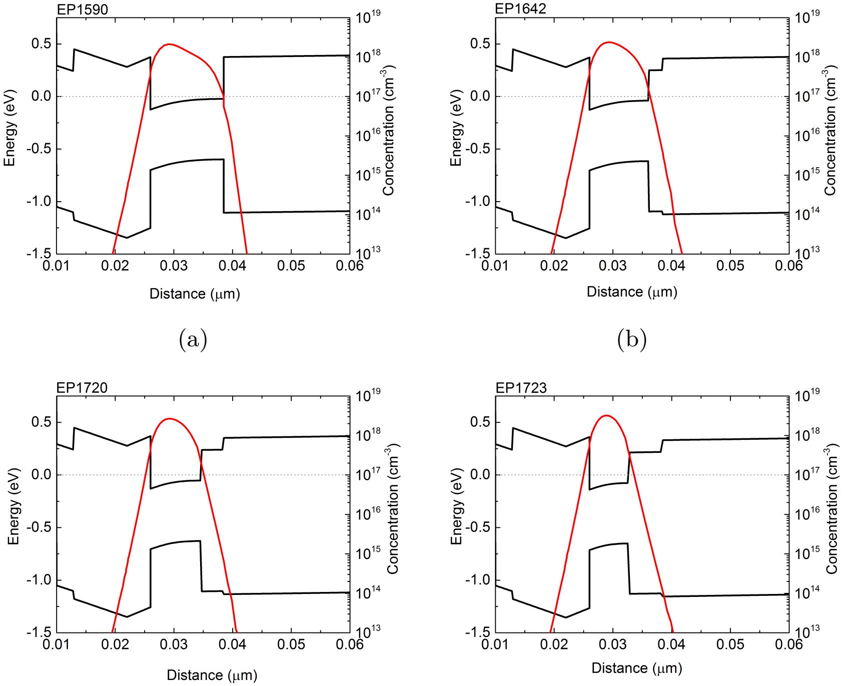
- EP1590: Standard structure as described in section 3.1,
- EP1642: Standard structure with 10 nm GaInAs channel and 2.5 nm InP backchannel,
- EP1720: Standard structure with 8.5 nm GaInAs channel and 4 nm InP backchannel,
- EP1723: Standard structure with 6.5 nm GaInAs channel and 6 nm InP backchannel.

Energy band diagrams and electron concentrations in the channels for the four structures, obtained by numerical simulation using the Sentaurus TCAD environment, are depicted in figure 4.2. Carrier mobilities, sheet carrier densities and channel sheet resistances for studied epitaxial layers, obtained from Hall measurements at 300 K and 77 K, are summarized in table 4.2.

Epitaxial Layer	**Temperature (K)**	**Mobility ($\mathrm{cm}^2/\mathrm{V{\cdot}s}$)**	**Sheet Carrier Density ($10^{12}\,\mathrm{cm}^{-2}$)**	**Sheet Resistance (Ω/square)**
EP1590	300	11900	1.5	346
EP1590	77	30800	2.1	98
EP1642	300	12700	1.7	287
EP1642	77	36100	2.3	74
EP1720	300	12800	1.6	295
EP1720	77	43400	2.2	65
EP1723	300	12000	1.6	324
EP1723	77	38000	2.4	69

TABLE 4.2: Summary of the Hall measurements for the four epitaxial layer structures used for the study of the GaInAs/InP composite channel.

As shown in table 4.2, structures with the InP backchannel show higher mobilities and higher sheet carrier densities compared to the standard structure, which can be justified by examining the band diagrams depicted in figure 4.2. Electrons in the layers with backchannels are more confined, and their peak concentration is increasing with the thickness of InP. Carrier mobility is improved for thicker InP layers, however it starts to descend again for the structure with 6 nm backchannel.



(a)

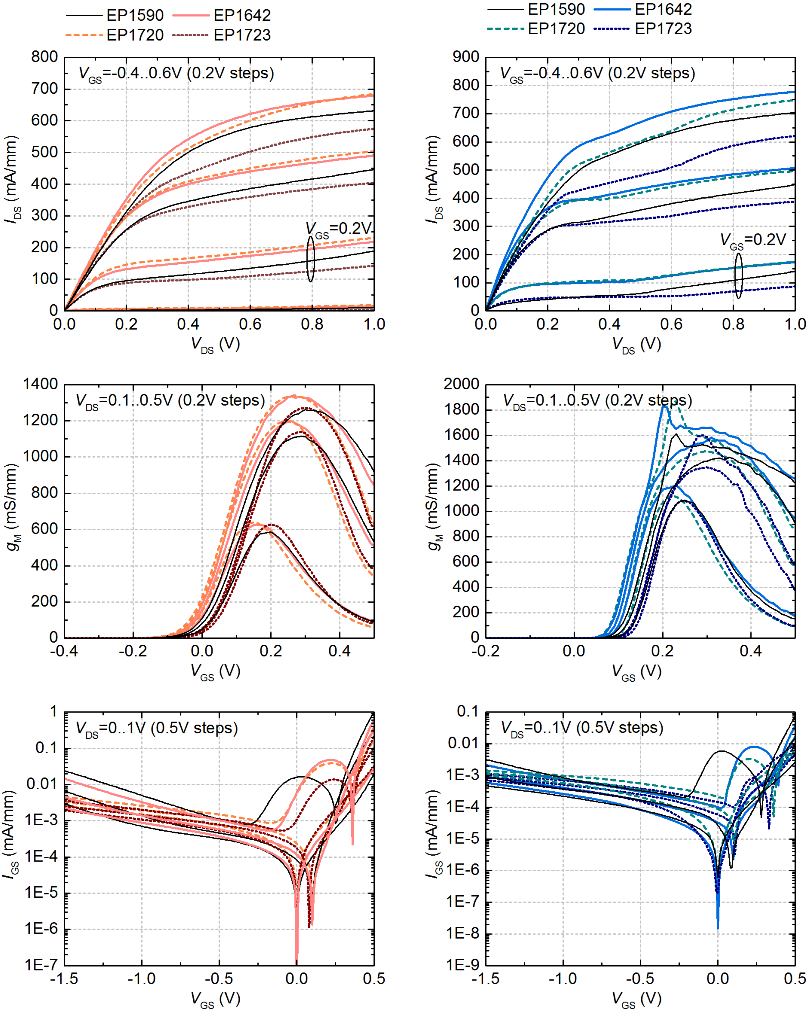
(b)

(c)

(d)

FIGURE 4.2: Simulated energy band diagrams and electron concentrations of structure with a) no InP backchannel, b) 2.5 nm InP backchannel, c) 4 nm InP backchannel and d) 6 nm backchannel.

DC measurements of 2 × 25 µm HEMTs with 100 nm gate lengths fabricated on these four structures, performed at room and cryogenic temperature, are depicted in figure 4.3.



(a) (b)

FIGURE 4.3: DC measurements of EP1590, EP1642, EP1720 and EP1723 performed at a) 300 K and b) 15 K for 2 × 25 µm HEMTs with 100 nm gate lengths.

In accordance with the Hall measurements and the numerical band diagram simulations, the DC characteristics show the following trends:

- Maximum drain current is higher for the structures with 2.5 and 4 nm backchannel compared to the other two structures.
- Maximum transconductance is higher for the structures with 2.5 and 4 nm backchannel compared to the other two structures.
- Impact ionization, noticeable as the hump in the gate diode measurements or as the slope of the IV curve, is lowest for the structure with 6 nm backchannel.
- Gate leakage is at the same level for all four structures.

The RF performance for these four structures (in terms of deembedded f_T and f_{max}) for $2 \times 25\,\mu m$ HEMTs with 100 nm gate lengths is summarized in table 4.3, for both 300 K and 15 K.

Epitaxial Layer	**Temperature (K)**	$f_{T,max}$**@**$V_{DS} = 0.75$ **V (GHz)**	f_T**@LNBP**[1] **(GHz)**	f_{max}**@LNBP (GHz)**
EP1590	300	211	171	302
EP1590	15	234	179	351
EP1642	300	219	181	337
EP1642	15	269	190	343
EP1720	300	218	187	331
EP1720	15	271	189	401
EP1723	300	214	182	304
EP1723	15	225	165	327

TABLE 4.3: RF performance of $2 \times 25\,\mu m$ HEMTs with 100 nm gate lengths for the four epitaxial layer structures with GaInAs/InP composite channel.

The extracted impact ionization transconductances for the investigated structures are depicted versus V_{DS} and I_{DS} in figures 4.4 and 4.5. Devices are $2 \times 25\,\mu m$ HEMTs with 100 nm gate lengths measured at 300 K and 15 K, respectively. Impact ionization time constant ($\tau_{im} = R_{im} \cdot C_{im}$) is increasing with the InP thickness.

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[1] LNBP (Low Noise Bias Point), typically $V_{DS} = 0.5$ V and $I_{DS} = 100$ mA/mm.

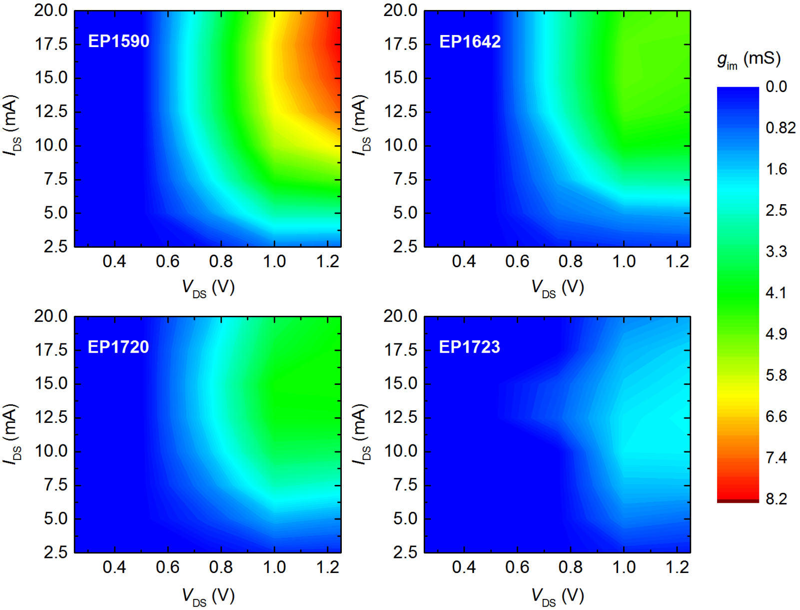


FIGURE 4.4: Comparison of impact ionization transconductance, g_{im}, for EP1590, EP1642, EP1720 and EP1723 extracted from RF measurements of $2 \times 25\,\mu\mathrm{m}$ HEMTs with 100 nm gate lengths at room temperature.

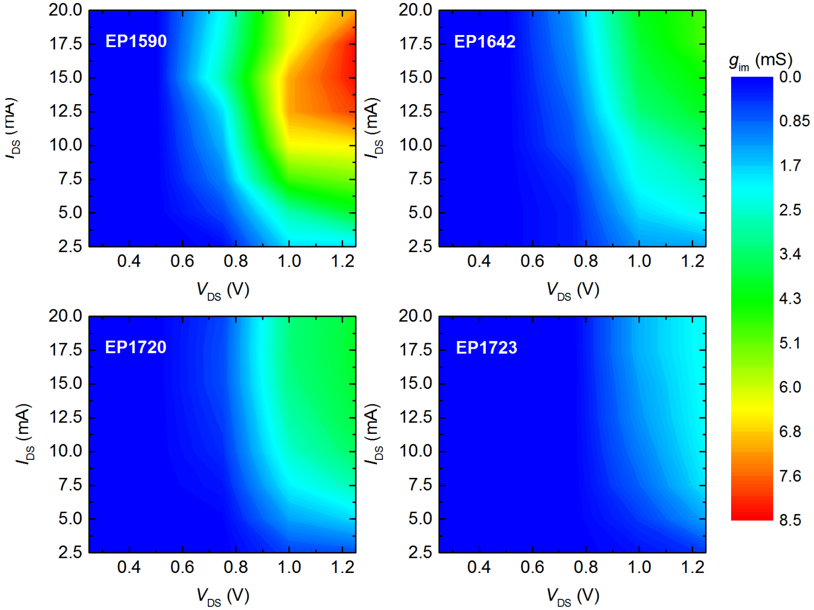


FIGURE 4.5: Comparison of impact ionization transconductance, g_{im}, for EP1590, EP1642, EP1720 and EP1723 extracted from RF measurements of $2 \times 25\,\mu\mathrm{m}$ HEMTs with 100 nm gate lengths at 15 K.

Comparison of extracted minimum noise figures and gains for $2 \times 25\,\mu\text{m}$ HEMTs with 100 nm gate lengths fabricated on the investigated structures is depicted in figure 4.6. Devices were all measured at the low noise bias point of $V_{\text{DS}} = 0.5\,\text{V}$ and $I_{\text{DS}} = 100\,\text{mA/mm}$.

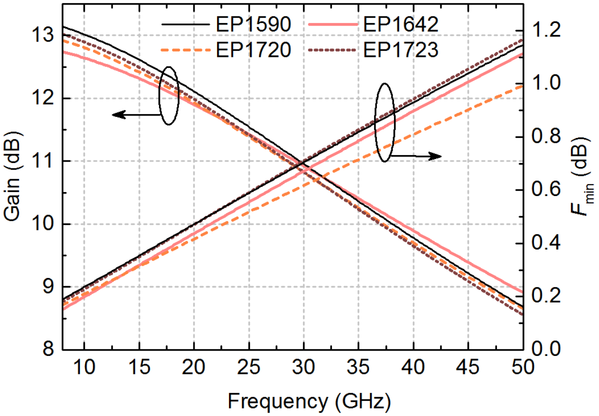


FIGURE 4.6: Gain and minimum noise figure of $2 \times 25\,\mu\text{m}$ HEMTs with 100 nm gate lengths for EP1590, EP1642, EP1720 and EP1723. The Maury MT7553 module was used as the noise receiver.

According to results presented in this section, the use of thicker InP backchannels reduces significantly the impact ionization effects. Moreover, because carriers in the channel are better confined, the structures with 2.5 and 4.5 nm InP even show improvements in f_{T} and f_{max} compared to the standard structure, whereas the performance of the structure with 6 nm backchannel is similar to the standard structure. Although the low noise bias point for all four structures is located outside of the impact ionization region according to figure 4.4, devices with 2.5 and 4.5 nm backchannel show a clear improvement in minimum noise figure at that bias as a result of improved f_{T} and f_{max}. Improvement in noise performance for the structures with backchannels is expected to be even more significant if devices are biased at higher drain voltages where impact ionization is manifested.

Further reduction of impact ionization could be achieved with additional increase of the InP layer thickness, however, RF and noise performance will deteriorate according to measurements shown in this section. A potential alternative to thicker InP layer would be adjusting the electron distribution in the 2DEG in order to have more carriers in the backchannel even at moderate V_{DS}. This can be achieved by adding a Si δ-doping plane below the channel as depicted in figure 4.7.

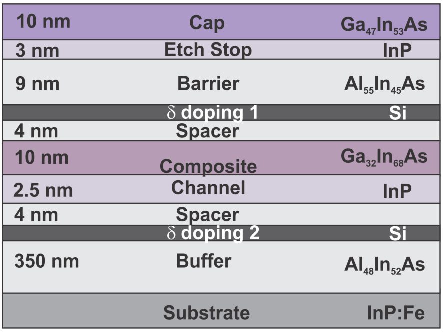


FIGURE 4.7: Epitaxial layer structure including 2.5 nm InP backchannel and two δ-doping layers.

The structure in figure 4.7, EP1693, is identical to EP1642 (2.5 nm InP backchannel), with addition of a second Si donor layer 4 nm below the channel. The numerically simulated energy band diagrams and electron concentrations for structures EP1642 and EP1693 are depicted in figure 4.8. As shown in figure 4.8, the positively charged Si donors below the channel for EP1693 attract the electrons towards the InP/AlInAs interface, therefore increasing their concentration in the backchannel compared to EP1642. However, the concentration of electrons in the buffer is also increased, potentially resulting in the formation of additional leakage path through the buffer. To compensate for the lower carrier mobilities in InP and obtain a similar 2DEG sheet resistance as for the EP1642, the total δ-doping (sum of upper and lower doping) in structure EP1693 was increased by 10%. The ratio of δ-doping density for the upper and the lower Si donor layer was set to 2:1, respectively. Hall measurements at 300 K and 15 K are summarized in table 4.4.

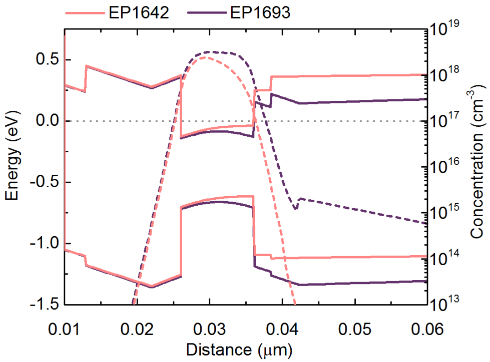


FIGURE 4.8: Simulated energy band diagrams and electron concentrations for structures including 2.5 nm InP backchannel (EP1642), and 2.5 nm InP backchannel with two δ-doping layers (EP1693).

Epitaxial Layer	**Temperature (K)**	**Mobility (cm^2/V·s)**	**Sheet Carrier Density (10^{12} cm^{-2})**	**Sheet Resistance (Ω/square)**
EP1693	300	14400	1.8	239
EP1693	77	34500	2.9	61

TABLE 4.4: Hall measurements for epitaxial layer with 2.5 nm InP backchannel and double δ-doping.

Comparison of DC measurements performed at room and cryogenic temperature for structures EP1642 and EP1693 is shown in figure 4.9 for $2 \times 25\,\mu\text{m}$ HEMTs with 100 nm gate lengths. The double δ-doping structure with the backchannel shows:

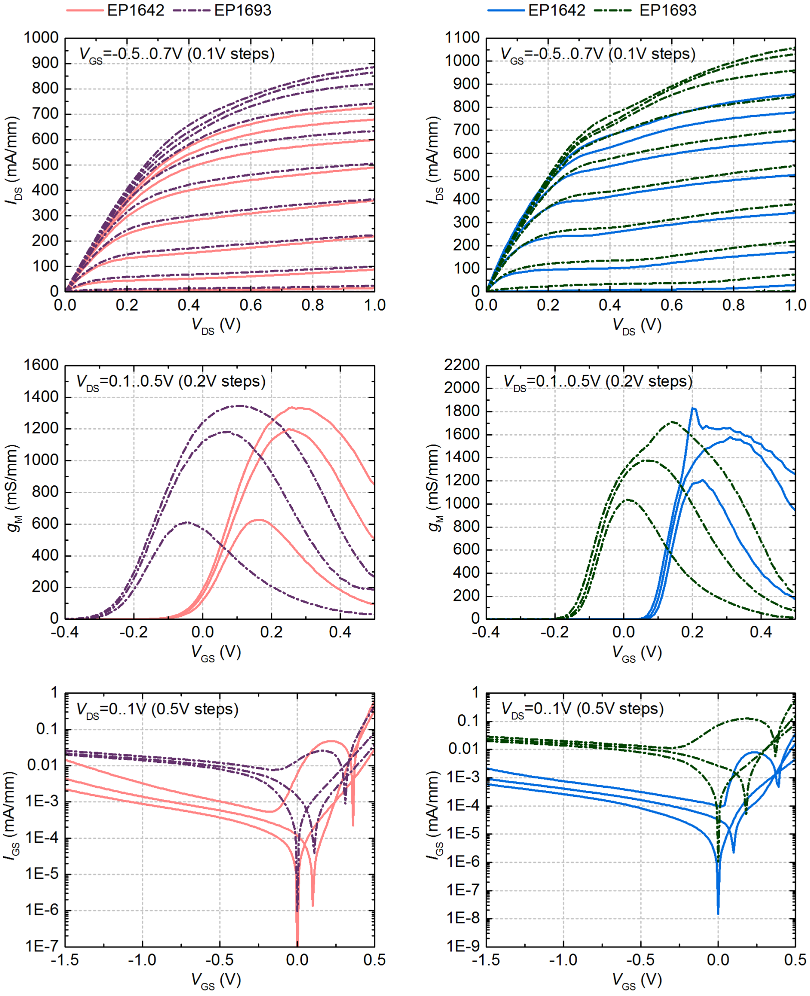
- Higher maximum current,
- Equal DC transconductance at 300 K,
- Reduced DC transconductance at 15 K,
- More negative threshold due to increased doping level and larger distance between the gate and the channel peak carrier concentration,
- Lower $I_{\text{on}}/I_{\text{off}}$ ratio due to higher current in off-state resulting from leakage through the buffer,
- Higher minimum NIF of $9.64\,\sqrt{\text{mA}\cdot\text{mm}}/\text{S}$ compared to $9.08\,\sqrt{\text{mA}\cdot\text{mm}}/\text{S}$ for EP1642,
- Higher gate leakage current due to increased doping level.

The RF performance for a $2 \times 25\,\mu\text{m}$ HEMT with 100 nm gate length fabricated on EP1693 is summarized in table 4.5, for both 300 K and 15 K.

Epitaxial Layer	**Temperature (K)**	$f_{\mathrm{T,max}}$**@**$V_{\mathrm{DS}} = 0.75\,\mathrm{V}$ **(GHz)**	f_{T}**@LNBP (GHz)**	$f_{\max}$**@LNBP (GHz)**
EP1693	300	231	186	321
EP1693	15	301	203	348

TABLE 4.5: RF performance of $2 \times 25\,\mu\text{m}$ HEMT with 100 nm gate length fabricated on the structure with double δ-doping.

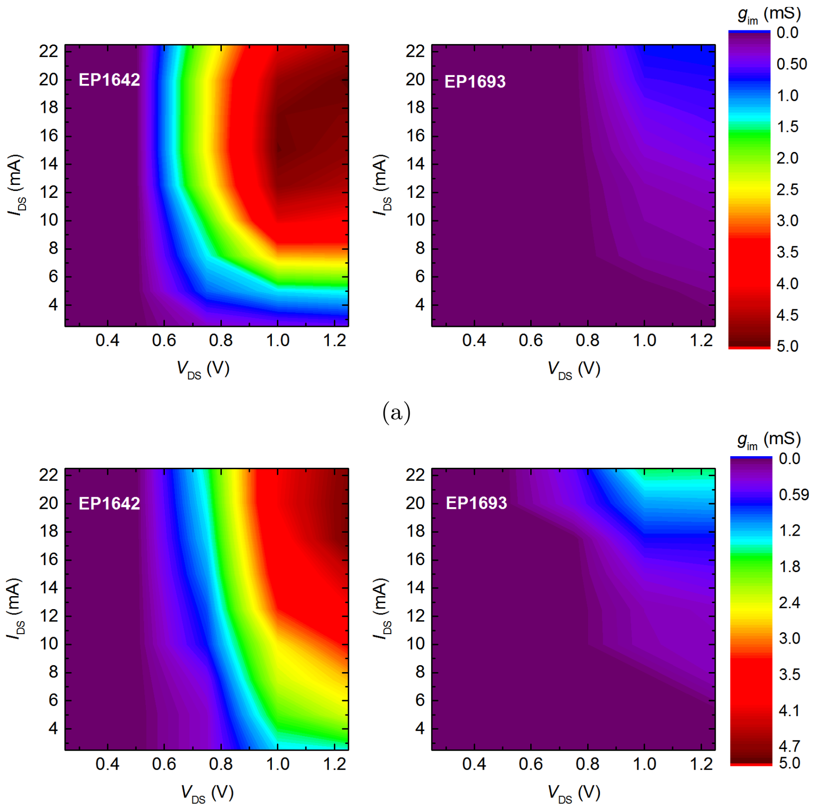
The comparison of extracted g_{im} for EP1642 and EP1693 is depicted in figure 4.10 for a $2 \times 25\,\mu\text{m}$ HEMTs with 100 nm gate lengths measured at 300 and 15 K, respectively. Impact ionization time constant is higher for structure EP1693 with respect to all other structures described in this section.



(a)

(b)

FIGURE 4.9: DC measurements of EP1642 and EP1693 performed at a) 300 K and b) 15 K for 2 × 25 µm HEMTs with 100 nm gate lengths.



(a)

(b)

FIGURE 4.10: Comparison of impact ionization transconductance, g_{im}, for EP1642 and EP1693 extracted from RF measurements of $2 \times 25\,\mu\text{m}$ HEMTs with 100 nm gate lengths at a) 300 K and b) 15 K.

The extracted minimum noise figures and gain of $2 \times 25\,\mu\text{m}$ HEMTs with 100 nm gate lengths are depicted in figure 4.11 for EP1642 and EP1693 at the low noise bias point of $V_{\text{DS}} = 0.5\,\text{V}$ and $I_{\text{DS}} = 100\,\text{mA/mm}$.

As shown in figure 4.10 and compared to figures 4.4 and 4.5, the impact ionization transconductance is considerably lower for the structure with double δ-doping, yielding even lower value with respect to the structure with

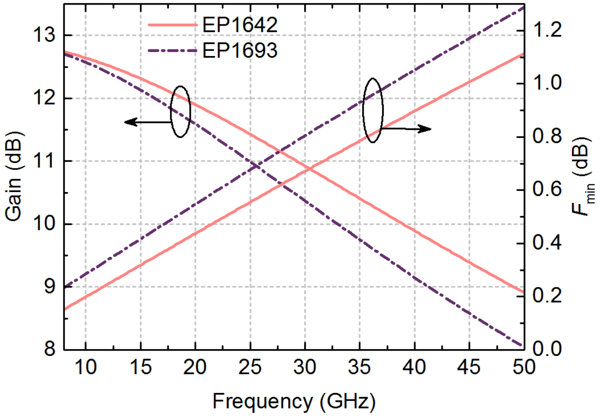


FIGURE 4.11: Gain and minimum noise figure of 2 × 25 µm HEMTs with 100 nm gate lengths for EP1642 and EP1693. The Maury MT7553 module was used as the noise receiver.

6 nm backchannel. On the other hand, the gate leakage and the off-state current increased above the optimum level required for good noise performance, hence the minimum noise figure is also increased, as shown in figure 4.11. However, there might exist other more suitable distribution between the two δ-doping levels and their overall increase needed to keep the 2DEG conductivity high. An optimized structure including two doping planes and a backchannel could provide acceptably low gate leakage and off-state current, together with reduced impact ionization effects.

The investigation presented in this section was performed for 12.5 nm thick $\mathrm{Ga_{0.32}In_{0.68}As}$ channel. According to the results presented, a good layer structure for the low noise bias point of $V_{\mathrm{DS}} = 0.5\,\mathrm{V}$ and $I_{\mathrm{DS}} = 100\,\mathrm{mA/mm}$ would be structure EP1642 (2.5 nm InP backchannel) or EP1720 (4 nm InP backchannel) in light of their similar RF and noise performances and improvements with respect to the standard structure EP1590. As a consequence of the optimum bias point located outside of the impact ionization region, additional suppressing of impact ionization effects at the low noise bias point is unnecessary. However, this might not be the case for the bias point with higher drain voltage, or for the epitaxial structures with increased In content to $x > 68\%$, where thicker backchannel or double δ-doping structure would be more suited.

In conclusion, to suppress the negative influence of the impact ionization on the noise behavior of InP HEMTs several solutions are possible depending on the extent of the effect at the selected bias point. For the desired gain/bandwidth and noise performance, specific trade-offs can be considered:

- Reducing the effects of impact ionization by adding an InP backchannel. This is to be weighted against the potential decrease of the channel conductivity for thick InP layers and can be partially compensated by increasing the 2DEG density.
- Reducing the effects of impact ionization by adding a Si δ-doping plane below the channel to increase the fraction of channel electrons residing in the backchannel. This is to be weighted against the increase of the gate leakage and off-state current.

4.3 COMPOSITE GAINAS/INPAS/INP CHANNEL

As described in section 4.2, the composite GaInAs/InP channel HEMTs offer improved performances and reduced impact ionization effects with respect to the standard GaInAs channel devices. However, due to a significant conduction band discontinuity between GaInAs and InP, it is relatively difficult to transfer electrons form the GaInAs channel into the InP backchannel where they have a reduced impact ionization rate. The electron distribution in the channel can be altered in order to provide more carriers in the backchannel by introducing the back doping, below the InP backchannel, as described in section 4.2. Alternatively, a composite GaInAs/InPAs/InP is implemented according to figure 4.12. The $Ga_{0.32}In_{0.68}As/InP_{0.37}As_{0.63}/InP$ channel in principle offers both high carrier mobilities and reduction of impact ionization rate in the $InP_{0.37}As_{0.63}$ layer.

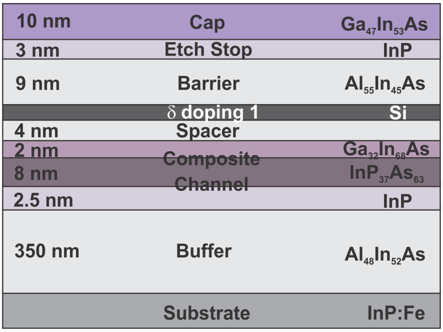


FIGURE 4.12: Epitaxial layer structure with GaInAs/InPAs/InP composite channel.

The numerically simulated energy band diagrams and electron concentrations for $Ga_{0.32}In_{0.68}As/InP_{0.37}As_{0.63}/InP$ and $Ga_{0.32}In_{0.68}As/InP$ channels are shown in figure 4.13. Both structures have the InP backchannel thickness of 2.5 nm. Because of the step down in conduction band at the GaInAs/InPAs interface electrons easily transfer from the GaInAs into InPAs where they have reduced impact ionization rate due to the wider band gap. In high electric fields, electrons eventually transfer from the InPAs into the InP.

For investigating the performance of GaInAs/InPAs/InP HEMTs, two structures were grown in accordance with figure 4.12 (EP1674 and EP1679),

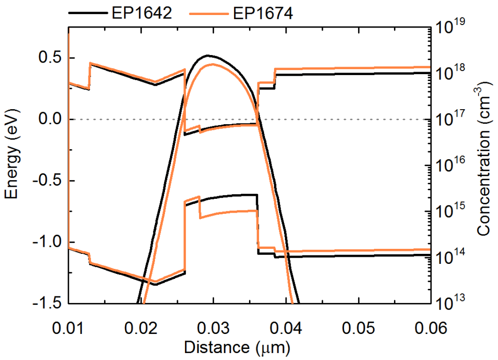


FIGURE 4.13: Simulated energy band diagrams and electron concentrations for structures with GaInAs/InPAs/InP (EP1674) and GaInAs/InP (EP1642) channel.

with different δ-doping levels to achieve a desired 2DEG conductivity comparable to the EP1642 (10 nm GaInAs and 2.5 nm InP). Structure EP1674 has the same δ-doping level as EP1642, whereas structure EP1679 has 30% higher doping level. Carrier mobilities, sheet carrier densities and channel sheet resistances for studied epitaxial layers, obtained from Hall measurements at 300 and 77 K, are summarized in table 4.6.

Epitaxial Layer	**Temperature (K)**	**Mobility (cm^2/V·s)**	**Sheet Carrier Density (10^{12} cm^{-2})**	**Sheet Resistance (Ω/square)**
EP1674	300	9660	1.3	483
EP1674	77	28200	2.1	103
EP1679	300	9740	1.9	337
EP1679	77	21100	3	99

TABLE 4.6: Summary of the Hall measurements for the epitaxial layer structures with GaInAs/InPAs/InP composite channel.

Devices form EP1642, EP1674 and EP1679 were fabricated side-by-side using the standard fabrication procedure described in Chapter 3. DC measurements of 2 × 50 µm HEMTs with 80 nm gate lengths fabricated on these structures and performed at room and cryogenic temperature are depicted in figure 4.14.

The DC characteristics from figure 4.14 show the following trends:

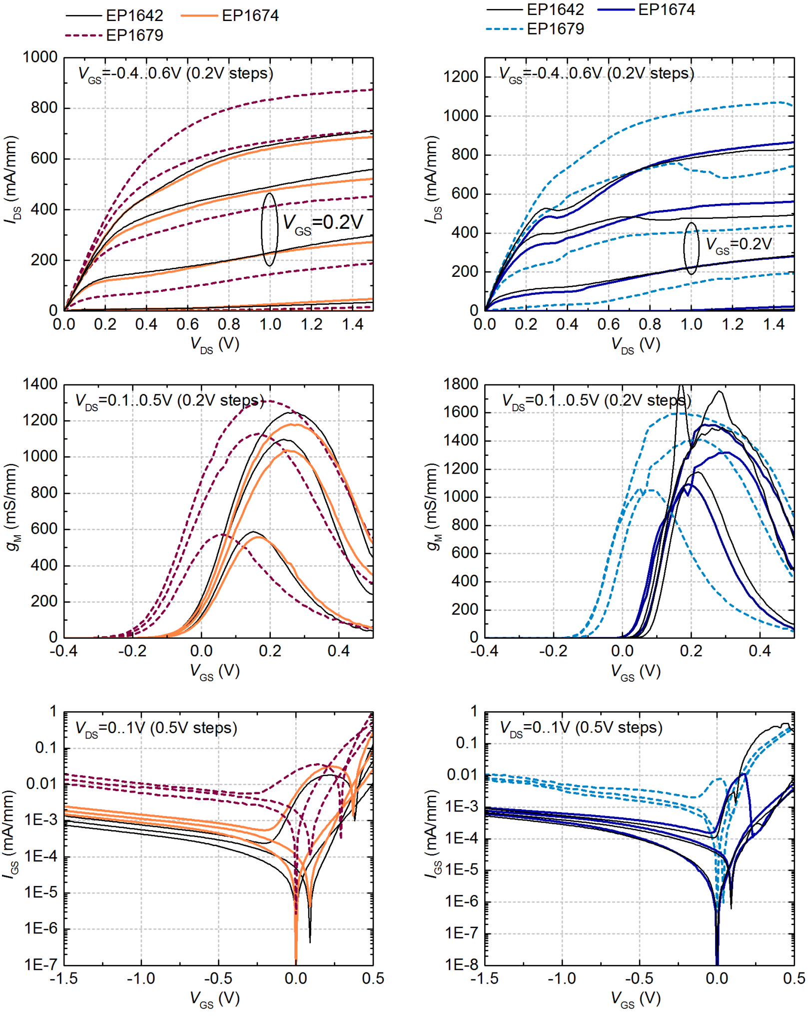
- Devices from EP1642 and EP1674 show similar behavior, with slightly lower current and transconductance for devices from EP1674. This is a consequence of the lower carrier mobility and sheet carrier density for wider bandgap $InP_{0.37}As_{0.63}$ channel in EP1674.
- Devices from EP1679 show higher drain current, higher gate leakage current, increased transconductance and have a more negative threshold due to higher doping level.

RF performance for $2 \times 50\,\mu m$ HEMTs with 80 nm gate lengths is summarized in table 4.7, for both 300 and 15 K.

Epitaxial Layer	**Temperature (K)**	$f_{\mathrm{T,max}}$**@**$V_{\mathrm{DS}} = 0.75\,\mathrm{V}$ **(GHz)**	f_{T}**@LNBP (GHz)**	f_{max}**@LNBP (GHz)**
EP1642	300	295	240	344
EP1642	15	327	223	362
EP1674	300	279	235	326
EP1674	15	333	214	354
EP1679	300	291	218	300
EP1679	15	328	211	371

TABLE 4.7: RF performance for GaInAs/InPAs/InP and GaInAs/InP channel $2 \times 50\,\mu m$ HEMTs with 80 nm gate lengths.

Devices from EP1674 and EP1642 have very similar RF performance at the low noise bias point, whereas performance of device from higher doped EP1679 is deteriorated despite reduced channel sheet resistance. With higher gate leakage and worse RF performance, EP1679 is not a good candidate for low noise operation and is therefore omitted from further characterization.



(a)

(b)

FIGURE 4.14: DC measurements of EP1642, EP1674 and EP1679 performed at a) 300 K and b) 15 K for 2 × 50 µm HEMTs with 80 nm gate lengths.

To model the impact ionization for GaInAs/InPAs/InP channel, additional circuitry had to be added to the small-signal model, as shown in figure 4.15, to account the electrons located at both GaInAs and InPAs layers. To illustrate the modeling differences, the measured and modeled S_{22} are plotted in figure 4.16 for a randomly selected bias point of $V_{\mathrm{DS}} = 1\,\mathrm{V}$ and $I_{\mathrm{DS}} = 10\,\mathrm{mA}$. Measured devices are $2 \times 50\,\mu\mathrm{m}$ HEMTs with a 80 nm gate length fabricated on EP1642 and EP1674. Modeled data for device from EP1642 is based on the extended SSIEC as shown in section 2.2.4.2, while for the device from EP1674 both models from section 2.2.4.2 and figure 4.15 are used. The extracted impact ionization parameters used to model the data in figure 4.16 are given in table 4.8.

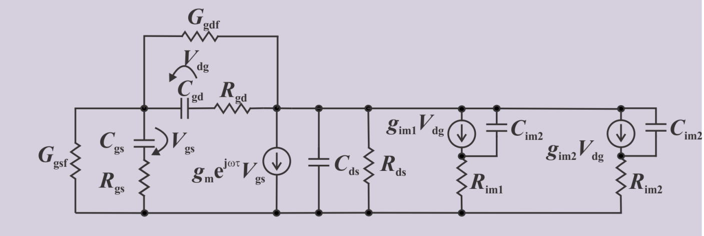


FIGURE 4.15: Intrinsic small-signal equivalent circuit used to model impact ionization for the structures with GaInAs/InPAs/InP channel.

Epitaxial Layer	g_{im1} **(mS)**	τ_{im1} **(ns)**	g_{im2} **(ns)**	τ_{im2} **(ns)**
EP1642	5.2	0.4	-	-
1674	2.9	4.9	-	-
1674 (model from fig. 4.15)	2.7	7	0.58	0.06

TABLE 4.8: Extracted impact ionization parameters used to model the data in figure 4.16 for $2 \times 50\,\mu\mathrm{m}$ HEMTs with 80 nm gate lengths.

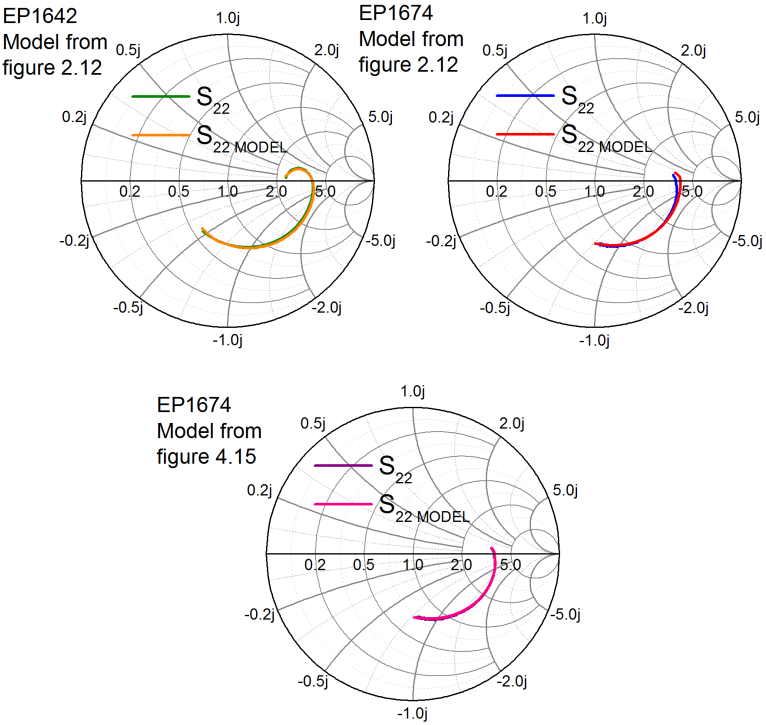


FIGURE 4.16: Measured and modeled S_{22} for 2 × 50 µm HEMTs with 80 nm gate lengths fabricated on EP1642 and EP1674. Bias point is $V_{\mathrm{DS}} = 1\,\mathrm{V}$ and $I_{\mathrm{DS}} = 10\,\mathrm{mA}$. Frequency range is 50 MHz to 40 GHz.

From figure 4.16 it can be seen that inductive behavior S_{22} is less strong for EP1674 with respect to EP1642, hence impact ionization effects are reduced for GaInAs/InPAs/InP channel. Furthermore, the fit between modeled and measured data for device from EP1674 data is clearly improved when two additional impact ionization circuits are used, indicating that the carriers are located in both GaInAs and InPAs, whereas most of the carriers for EP1642 are confined in GaInAs.

The extracted impact ionization transconductances versus V_{DS} and I_{DS} for EP1642 and EP1674 are depicted in figure 4.17 for 2 × 50 µm HEMTs with 80 nm gate lengths measured at 300 K. Impact ionization transconductances were extracted according to the extended SSIEC as shown in section 2.2.4.2 for devices from EP1642, whereas the modeling for EP1674 was done according to the SSIEC shown in figure 4.15.

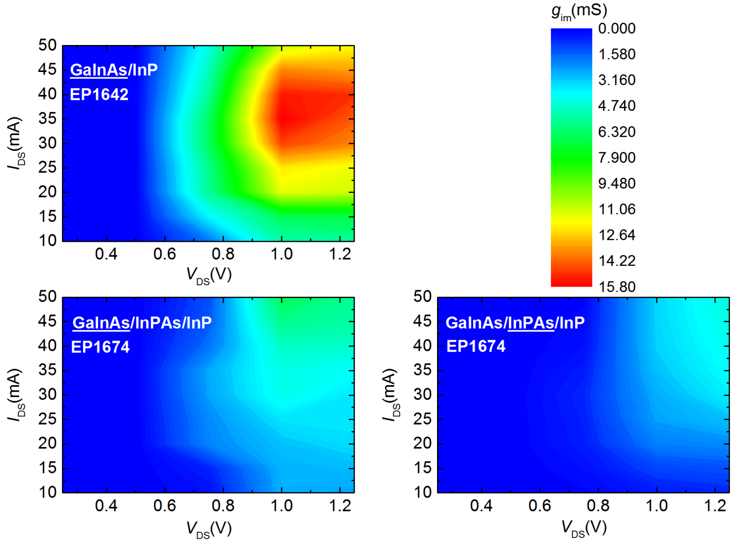
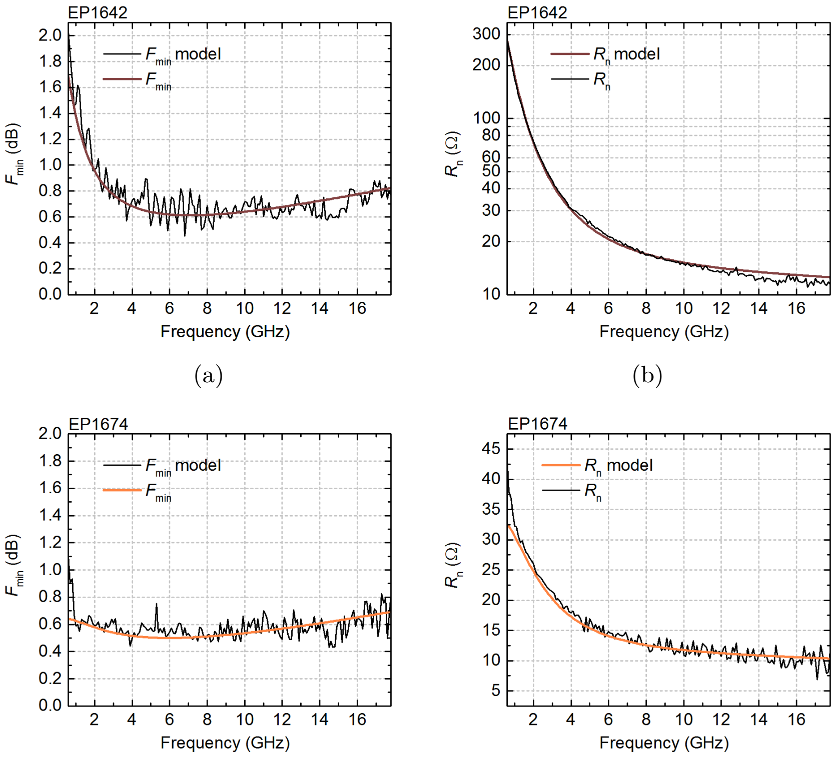


FIGURE 4.17: Comparison of impact ionization transconductance, g_{im}, for EP1642 and EP1674 extracted from RF measurements of 2 × 50 µm HEMTs with 80 nm gate lengths at 300 K.

Modeling of impact ionization effects for the GaInAs/InPAs/InP channel of EP1674 according to figure 4.15 yields two transconductances which represent impact ionization in $\mathrm{Ga_{0.32}In_{0.68}As}$ and $\mathrm{InP_{0.37}As_{0.63}}$ sub-channels individually. Due to the smaller bandgap, onset of impact ionization for the $\mathrm{Ga_{0.32}In_{0.68}As}$ sub-channel is at lower drain voltage compared to the $\mathrm{InP_{0.37}As_{0.63}}$ sub-channel. As a consequence, the extracted transconductances correspond to the respective sub-channels in a manner shown in figure 4.17.

Noise parameters (F_{min} and R_{n}) extracted from measurements and obtained from the model for EP1642 and EP1674 are depicted in figure 4.18. Measurement range was 0.8-18 GHz, and measured devices and the bias point are the same as in figure 4.16. Both the minimum noise figure F_{min} and the noise resistance R_{n} extracted from measurements of device from EP1674 show a smaller increase at low frequencies compared to device from EP1642, confirming reduced impact ionization effects for GaInAs/InPAs/InP channel.



(a) (b)

(c) (d)

FIGURE 4.18: Extracted and modeled noise parameters a) F_{min}, b) R_{n} for EP1642 and c) F_{min}, d) R_{n} for EP1674. Devices are $2 \times 50\,\mu\text{m}$ HEMTs with 80 nm gate lengths measured at 300 K at a bias point of $V_{\text{DS}} = 1\,\text{V}$ and $I_{\text{DS}} = 10\,\text{mA}$.

The extracted minimum noise figures and gains of 2 × 25 µm HEMTs with 80 nm gate lengths are depicted in figure 4.19 for EP1642 and EP1674 at a low noise bias point of $V_{\mathrm{DS}} = 0.5\,\mathrm{V}$ and $I_{\mathrm{DS}} = 100\,\mathrm{mA/mm}$. At the low noise bias point devices from EP1642 and EP1674 exhibit comparable minimum noise figure, while gain for EP1642 devices is higher.

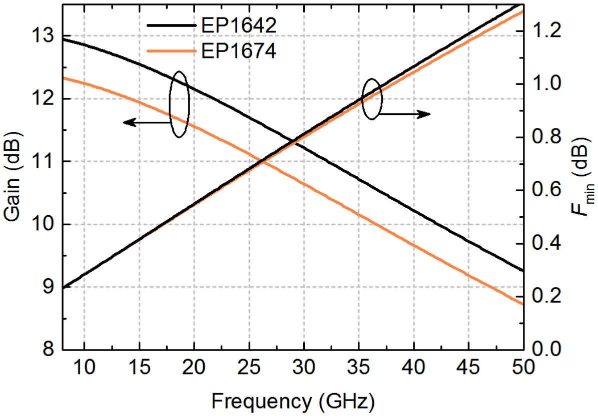


FIGURE 4.19: Gain and minimum noise figure of 2 × 25 µm HEMTs with 100 nm gate lengths for the EP1642 and EP1674. The noise receiver was implemented according to figure 2.15.

In conclusion, $Ga_{0.32}In_{0.68}As/InP_{0.37}As_{0.63}/InP$ channel HEMTs with the same δ-doping level exhibit similar RF and noise performance at the low noise bias point as the $Ga_{0.32}In_{0.68}As/InP$ devices. Moreover, at higher V_{DS}, due to the larger bandgap of $InP_{0.37}As_{0.63}$ with respect to $Ga_{0.32}In_{0.68}As$, impact ionization effects are less pronounced making the GaInAs/InPAs/InP HEMT a good alternative for GaInAs/InP or GaInAs channel HEMT. The GaInAs/InPAs/InP channel can be further improved by adding an even narrower bandgap material such as InAs to the composite mix. The InAs/GaInAs/InPAs/InP channel devices would be able to achieve superior f_{T} and f_{max} due to InAs/GaInAs while at the same time significantly suppressing the effects of impact ionization due to InPAs/InP layers.

4.4 CAP LAYER DESIGN FOR REDUCED ACCESS RESISTANCES

InP HEMTs owe their superior noise and gain performances not only to their excellent channel transport properties but also to their minimal parasitic source and drain resistances. Formation of the source and drain Ohmic contacts, as explained in Chapter 3, heavily relies on the attributes of the highly-doped n^+ cap layer that supplies the electrons tunneling to the channel. Therefore, any increase in the cap doping level should consequently reduce the contact resistance, providing that the crystal structure of the semiconductor is intact. Besides the crystal quality, the growth conditions, such as the maximum temperature of the Si source, pose a limiting factor for the maximum level of cap doping.

To investigate the influence of the cap doping on InP HEMT performance, two identical structures were processed side-by-side using the standard fabrication procedure described in Chapter 3. The two examined structures are the reference structure EP1590 with cap doping of $3 \cdot 10^{19}\,\mathrm{cm}^{-3}$ and EP1815, with identical composition and thickness as EP1590, and cap doping of $4.5 \cdot 10^{19}\,\mathrm{cm}^{-3}$. Cap doping was determined using capacitance-voltage profiling. Hall measurements of the EP1815 are summarized in table 4.9.

Epitaxial Layer	**Temperature (K)**	**Mobility ($\mathrm{cm}^2/\mathrm{V{\cdot}s}$)**	**Sheet Carrier Density ($10^{12}\,\mathrm{cm}^{-2}$)**	**Sheet Resistance (Ω/square)**
EP1815	300	12100	1.6	319
EP1815	77	25100	2.5	98

Table 4.9: Hall measurements for the epitaxial layer EP1815 with 50% higher cap doping.

Comparison of DC performance of 2 × 25 µm HEMTs with 100 nm gate lengths at 300 and 15 K is summarized in table 4.10. Comparison of RF performance of 2 × 25 µm HEMTs with 100 nm gate lengths at 300 and 15 K is summarized in table 4.11.

According to tables 4.10 and 4.11, structure with higher cap doping (EP1815) exhibits lower source and drain resistances, and consequently f_T and f_max are improved. The gate leakage currents are at the same level for both structures. The effects of impact ionization characterized by the transconductance g_im and τ_im are similar for both structures.

Epitaxial Layer	**Temperature (K)**	$g_{\mathrm{M,max}}$ **(mS/mm)**	$I_{\mathrm{DS,max}}$ **(mA/mm)**	V_{th} **(V)**	I_{GS} **(uA/mm)**	R_{s} **(Ω)**	R_{d} **(Ω)**
EP1590	300	1102	650	-0.16	0.53	4.18	4.26
EP1590	15	1250	830	-0.11	0.22	3.19	3.25
EP1815	300	1187	780	-0.18	0.66	3.79	3.91
EP1815	15	1320	950	-0.12	0.25	2.95	2.97

Table 4.10: DC performance of $2 \times 25\,\mu\mathrm{m}$ HEMTs with 100 nm gate lengths for the two structures with different cap doping.

Epitaxial Layer	**Temperature (K)**	$f_{\mathrm{T,max}}$**@**$V_{\mathrm{DS}} = 0.75$ **(GHz)**	f_{T}**@LNBP (GHz)**	f_{max}**@LNBP (GHz)**	g_{m}**@LNBP (mS)**
EP1590	300	195	173	298	60
EP1590	15	238	170	312	57
EP1815	300	212	183	327	64
EP1815	15	244	172	345	60

Table 4.11: RF performance of $2 \times 25\,\mu\mathrm{m}$ HEMTs with 100 nm gate lengths for the two structures with different cap doping.

The extracted minimum noise figures and gains of $2 \times 25\,\mu\mathrm{m}$ HEMTs with 100 nm gate lengths for the two structures are depicted in figure 4.20 for the low noise bias point of $V_{\mathrm{DS}} = 0.5\,\mathrm{V}$ and $I_{\mathrm{DS}} = 100\,\mathrm{mA/mm}$. As expected, the structure with higher cap doping shows decreased minimum noise figure and increased gain.

Further reduction of the access resistances can be achieved by employing a composite GaInAs/AlInAs cap as depicted in figure 4.21. A heavily-doped GaInAs/AlInAs cap lowers the potential barrier of the Schottky barrier layer as depicted in figure 4.21, and considerably increases the tunneling current between the contacts and the channel. This cap structure is commonly used for the formation of the non-annealed contacts [51] [67], however, it is beneficial for the formation annealed contacts as well.

The influence of the composite cap on the InP HEMT performance was studied with three epitaxial layer structures processed side-by-side using a modified fabrication procedure where the mesa isolation and gate recess steps were performed with a solution based on citric acid. They were done in opposite order to obtain the sharply defined etch edges and the smooth

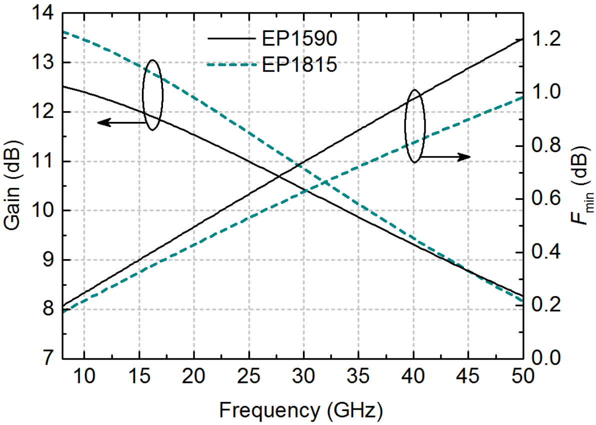


FIGURE 4.20: Gain and minimum noise figure of 2 × 25 µm HEMTs with 100 nm gate lengths for the EP1590 and EP1815. The Maury MT7553 module was used as the noise receiver.

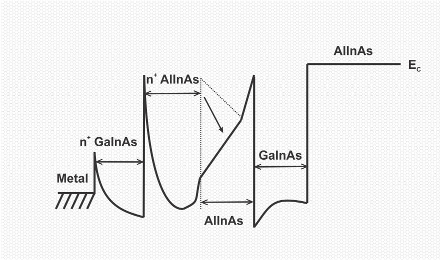
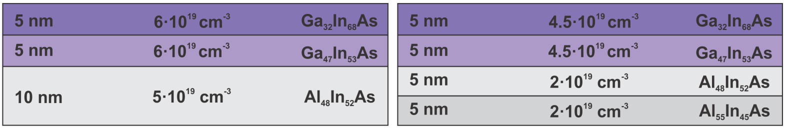


FIGURE 4.21: Conduction band profile for the GaInAs/AlInAs composite cap [51] HEMTs.

surface required for the T-gate contact formation. Two different cap layers (EP1842 and EP1872) were implemented according to figure 4.22. A third structure (EP1873) has identical cap layer as shown in figure 4.22b but uses a composite 10 nm GaInAs and 2.5 nm InP channel. Hall measurements for these three epitaxial structures are summarized in table 4.12.



5 nm	$6 \cdot 10^{19}$ cm^{-3}	$Ga_{32}In_{68}As$
5 nm	$6 \cdot 10^{19}$ cm^{-3}	$Ga_{47}In_{53}As$
10 nm	$5 \cdot 10^{19}$ cm^{-3}	$Al_{48}In_{52}As$

(a)

5 nm	$4.5 \cdot 10^{19}$ cm^{-3}	$Ga_{32}In_{68}As$
5 nm	$4.5 \cdot 10^{19}$ cm^{-3}	$Ga_{47}In_{53}As$
5 nm	$2 \cdot 10^{19}$ cm^{-3}	$Al_{48}In_{52}As$
5 nm	$2 \cdot 10^{19}$ cm^{-3}	$Al_{55}In_{45}As$

(b)

FIGURE 4.22: Composite GaInAs/AlInAs cap layer for the structures a) EP1842 and b) EP1872 and EP1873.

Epitaxial Layer	**Temperature (K)**	**Mobility (cm^2/V·s)**	**Sheet Carrier Density (10^{12} cm^{-2})**	**Sheet Resistance (Ω/square)**
EP1842	300	12300	1.5	329
EP1842	77	32200	2.1	88
EP1872	300	14500	1.2	348
EP1872	77	26000	2.5	94
EP1873	300	11700	2.1	264
EP1873	77	32100	2.6	74

TABLE 4.12: Summary of the Hall measurements for the three epitaxial layer structures used for the study of the GaInAs/AlInAs composite cap.

Comparison of DC performance at 300 and 15 K is summarized in table 4.13 for 2 × 25 µm HEMTs with 80 nm gate lengths. Comparison of RF performance of 2 × 25 µm HEMTs with 80 nm gate lengths at 300 and 15 K is summarized in table 4.14.

According to tables 4.13 and 4.14, structures with a step-graded AlInAs cap (EP1872 and EP1873, figure 4.22b) show an advantage in f_T and f_{max} over the structure with a lattice matched AlInAs cap (EP1842, figure 4.22a). Moreover, compared to the highly-doped GaInAs cap structure EP1815, access resistances are reduced when the graded AlInAs is used. The performance of devices with composite GaInAs/InP channel (EP1873) is improved compared to the structure with standard channel (EP1872), in a similar manner as described in section 4.2. The gate leakage currents are at comparable level for all structures.

The extracted minimum noise figures and gains of 2 × 25 µm HEMTs with 80 nm gate lengths for EP1815, EP1842, EP1872 and EP1873 are

Epitaxial Layer	**Temperature (K)**	$g_{\mathbf{M,max}}$ **(mS/mm)**	$I_{\mathbf{DS,max}}$ **(mA/mm)**	$V_{\mathbf{th}}$ **(V)**	$I_{\mathbf{GS}}$ **(uA/mm)**	$R_{\mathbf{s}}$ **(Ω)**	$R_{\mathbf{d}}$ **(Ω)**
EP1815	300	1200	790	-0.22	0.6	3.92	4.15
EP1815	15	1350	930	-0.14	0.1	3.11	3.27
EP1842	300	1130	750	-0.28	3.8	4.35	4.64
EP1842	15	1280	890	-0.12	0.4	3.17	3.24
EP1872	300	1210	850	-0.27	0.7	3.68	3.63
EP1872	15	1360	1020	-0.13	0.2	2.81	3.06
EP1873	300	1252	950	-0.33	2.4	3.58	3.61
EP1873	15	1400	1180	-0.19	0.3	2.74	2.93

TABLE 4.13: DC performance of $2 \times 25\,\mu\text{m}$ HEMTs with 80 nm gate lengths for the epitaxial structures with composite cap layers and highly doped GaInAs cap.

Epitaxial Layer	**Temperature (K)**	$f_{\mathbf{T,max}}$ **(GHz)**	$f_{\mathbf{T}}$**@LNBP (GHz)**	$f_{\mathbf{max}}$**@LNBP (GHz)**	$g_{\mathbf{m}}$**@LNBP (mS)**
EP1815	300	263	211	321	58
EP1815	15	290	208	295	53
EP1842	300	276	217	311	52
EP1842	15	283	213	310	49
EP1872	300	283	222	336	54
EP1872	15	298	211	370	50
EP1873	300	293	226	337	56
EP1873	15	416	268	315	52

TABLE 4.14: RF performance of $2 \times 25\,\mu\text{m}$ HEMTs with 80 nm gate lengths for the epitaxial structures with composite cap layers and highly doped GaInAs cap.

depicted in figure 4.23 at the low noise bias point of $V_{\text{DS}} = 0.5\,\text{V}$ and $I_{\text{DS}} = 100\,\text{mA/mm}$. The structure with graded AlInAs and composite GaInAs/InP channel (EP1873) shows the best minimum noise figure and gain, whereas the other two structures with composite GaInAs/AlInAs cap exhibit worse performance compared to highly doped single layer GaInAs cap (EP1815).

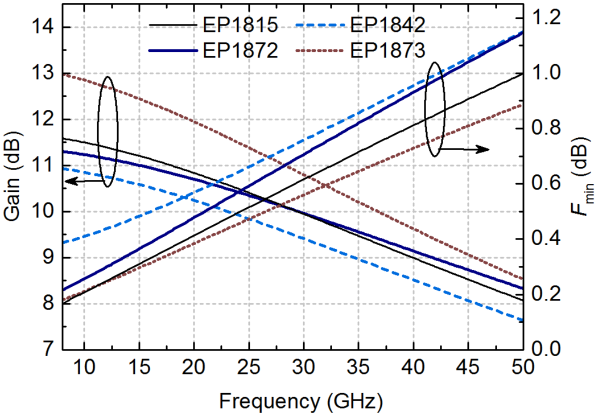


FIGURE 4.23: Gain and minimum noise figure of 2 × 25 µm HEMTs with 80 nm gate lengths for EP1815, EP1842, EP1872 and EP1873. The Maury MT7553 module was used as the noise receiver.

Deteriorated noise performance of EP1842 compared to EP1815 was expected due to the increased access resistances for that composite cap layer structure. However, despite a reduction in device access resistances for EP1872 compared to EP1815, an improvement in minimum noise figure is not obtained. Justification can be found by examining the RF transconductances from table 4.14. For composite cap layers, g_m is decreased, indicating impaired gate control over the channel. One explanation for worse gate control over the channel is the shorter effective gate length resulting from the highly doped composite cap making the recess effectively smaller. This can be observed in the plot of DC transconductances versus drain current in figure 4.24. More current is needed for devices from EP1872 to obtain the same g_M with respect to devices from EP1815, hence the quality of pinch-off is reduced. The extracted NIFs for the EP1815 and EP1872 at low noise bias point are 10.52 and 10.89 $\sqrt{\mathrm{mA}\cdot\mathrm{mm}}/\mathrm{S}$ respectively, confirming the decreased pinch-off quality. The SCEs, such as Drain Induced Barrier Lowering (DIBL), are more pronounced for devices with composite cap layers. However, despite reduced gate control over the channel (similar as for EP1872) performance of devices from EP1873 is superior with respect to EP1815 due to the positive effect of the InP backchannel.

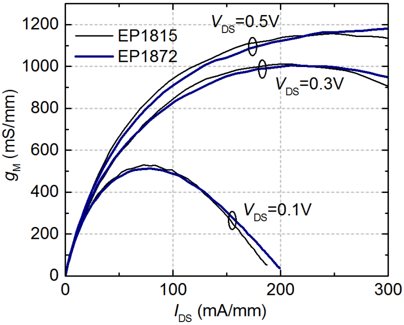


FIGURE 4.24: DC transconductance of 2 × 25 µm HEMTs with 80 nm gate lengths measured at 300 K for EP1815 and EP1872.

Non-annealed Ti/Pt/Au Ohmic contacts fabricated on all structures with the composite cap shown in this section exhibit four times higher contact resistance with respect to the annealed contacts. Because similar composite cap layers have been successfully used in the low resistance non-annealed contacts [67] [13], additional improvement is therefore possible. Further reduction of access resistances can in principle be obtained by increasing the thickness of the doped AlInAs cap layer or by increasing the doping of the AlInAs layer, both increasing the tunneling probability through the AlInAs Schottky barrier and the tunneling current between the Ohmic contact and the channel. However, a trade-off has to be made between the additional reduction of access resistances by employing more conductive cap layers and the potential loss of the gate control over the channel.

4.5 VERTICALLY SCALED HEMTS

Over the last few decades transistor downscaling has brought immense improvements in performance, density and power consumption to every technology. For InP-based HEMTs, the reduction of their main parasitic capacitances is done by decreasing the length of their smallest fabricated feature – the gate. The decrease of the gate length usually has to be accompanied by the downscaling of the epitaxial layer thicknesses to avoid enhancing the SCEs and to maintain a good pinch-off behavior [62]. Epitaxial layer structure of vertically scaled HEMTs fabricated in this work is depicted in figure 4.25.

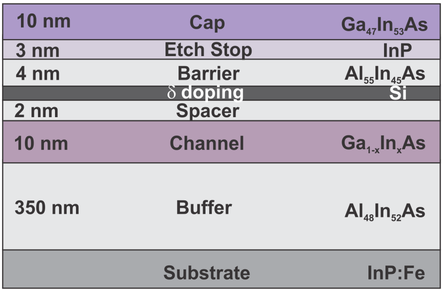


FIGURE 4.25: Epitaxial layer structure of vertically scaled HEMTs.

Downscaling of epitaxial layers involves reduction of the barrier, spacer and channel layer thicknesses, and thus the distance between the gate and the channel. As a consequence, the probability of tunneling through the Schottky barrier is higher, and the gate leakage is increased. Moreover, due to the channel being closer to the surface, the δ-doping of vertically scaled HEMTs has to be increased to compensate for the depletion by the surface traps. As a result of the channel thickness reduction, transport properties deteriorate because of enhanced carrier scattering. Compensation for impaired transport properties in thin channels is usually done with the increase of the channel In content. To optimize the $\mathrm{Ga}_{1-x}\mathrm{In}_x\mathrm{As}$ channel for vertically scaled HEMTs shown in figure 4.25, four structures were grown with $x = 68, 75$ and 100%, and processed side-by-side in the standard process flow described in Chapter 3.

Epitaxial layers based on the figure 4.25 compared in this section are:

- EP1638: Structure with $Ga_{0.32}In_{0.68}As$ channel,
- EP1640: Structure identical to EP1638 with 30% higher δ-doping,
- EP1641: Structure with $Ga_{0.25}In_{0.75}As$ channel,
- EP1609: Structure with $Ga_{0.47}In_{0.53}As/InAs/Ga_{0.47}In_{0.53}As$ channel with 3, 2 and 5 nm thicknesses, respectively.

Carrier mobilities, sheet carrier densities and channel sheet resistances for the studied epitaxial layers, obtained from Hall measurements at 300 K and 77 K, are summarized in table 4.15.

Epitaxial Layer	**Temperature (K)**	**Mobility ($cm^2/V{\cdot}s$)**	**Sheet Carrier Density ($10^{12}\,cm^{-2}$)**	**Sheet Resistance (Ω/square)**
EP1638	300	11800	2.4	219
EP1638	77	33200	2.9	64
EP1640	300	10400	3.4	178
EP1640	77	24700	3.6	70
EP1641	300	12600	2.6	187
EP1641	77	32200	3.3	59
EP1609	300	13200	2.5	189
EP1609	77	36600	3.0	55

TABLE 4.15: Summary of the Hall measurements for the epitaxial layer structures EP1638, EP1640, EP1641 and EP1609.

The comparison of DC performance of 2 × 25 µm HEMTs with 80 nm gate lengths at 300 and 15 K for investigated structures is depicted in figure 4.26 and summarized in table 4.16. The comparison of RF performance of 2 × 25 µm HEMTs with 80 nm gate lengths at 300 and 15 K is summarized in table 4.17.

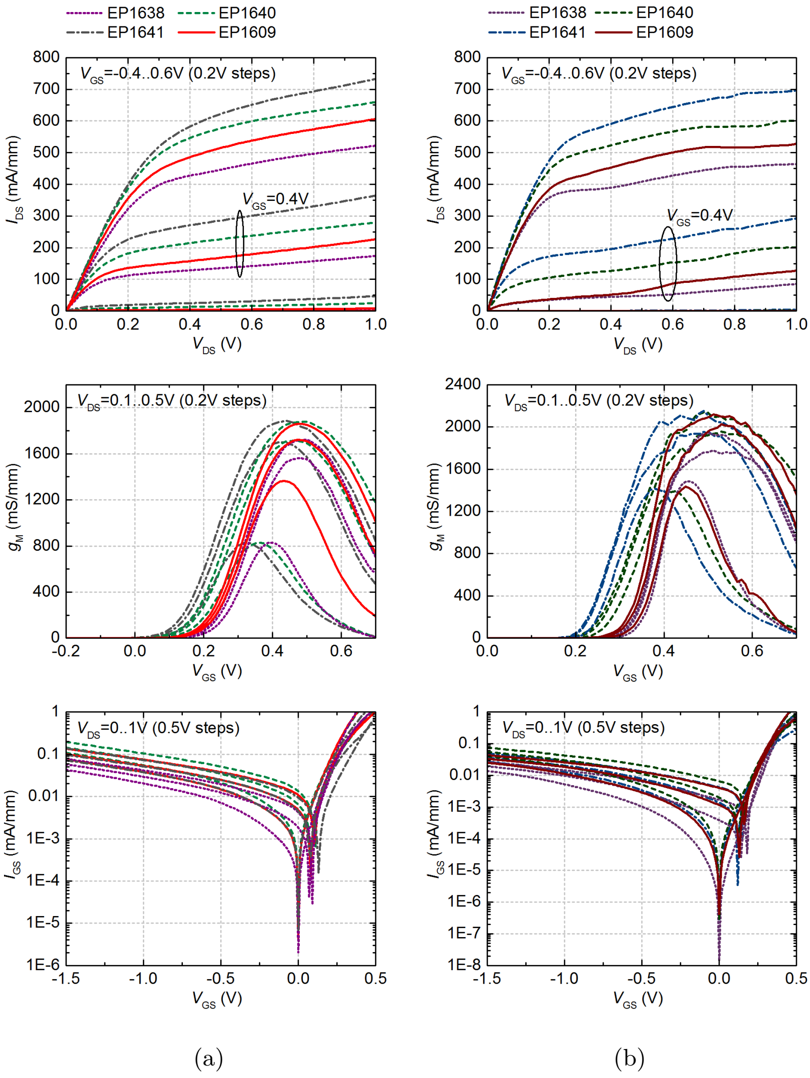


FIGURE 4.26: DC measurements of EP1638, EP1640, EP1642 and EP1609 performed at a) 300 K and b) 15 K for 2 × 50 µm HEMTs with 80 nm gate lengths.

Epitaxial Layer	**Temperature (K)**	$g_{\mathbf{M,max}}$ **(mS/mm)**	$V_{\mathbf{th}}$ **(V)**	$I_{\mathbf{GS}}$ **(uA/mm)**	$R_{\mathbf{s}}$ **(Ω)**	$R_{\mathbf{d}}$ **(Ω)**
EP1638	300	1764	0.19	20.0	3.65	3.68
EP1638	15	1801	0.33	7.9	2.45	2.62
EP1640	300	1908	0.13	55.0	1.98	2.13
EP1640	15	2103	0.25	20.4	1.63	1.41
EP1641	300	1928	0.11	37.0	2.71	2.75
EP1641	15	2130	0.20	15.3	1.89	1.98
EP1609	300	1923	0.17	38.0	2.77	2.81
EP1609	15	2210	0.31	11.2	2.23	2.3

Table 4.16: DC performance of $2 \times 25\,\mu\mathrm{m}$ HEMTs with 80 nm gate lengths for EP1638, EP1640, EP1641 and EP1609.

Epitaxial Layer	**Temperature (K)**	$f_{\mathbf{T,max}}$[2]**@** $V_{\mathbf{DS}} = 0.7\,\mathbf{V}$ **(GHz)**	$f_{\mathbf{T}}$**@LNBP (GHz)**	$f_{\mathbf{max}}$**@LNBP (GHz)**
EP1638	300	320	241	402
EP1638	15	-	255	408
EP1640	300	338	212	306
EP1640	15	-	206	380
EP1641	300	344	261	373
EP1641	15	-	266	402
EP1609	300	336	248	366
EP1609	15	-	279	410

Table 4.17: RF performance of $2 \times 25\,\mu\mathrm{m}$ HEMTs with 80 nm gate lengths for EP1638, EP1640, EP1641 and EP1609.

Compared to devices fabricated on the standard structure (EP1590 shown in figure 4.3), vertically scaled HEMTs have higher maximum DC transconductance, more positive threshold and an order of magnitude higher gate current. Due to the higher gate current level, characteristic bell-shape due to impact ionization is not noticeable. Access resistances have decreased compared to extracted values for standard structure (summarized in table 4.10).

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[2] Values of $f_{\mathrm{T,max}}$ at 15 K is omitted due to device instability

With respect to the standard structure (shown in table 4.11), intrinsic cut-off and maximum oscillation frequencies have increased with the reduction of the gate length and increase of the transconductance, whereas the SCEs such as the DIBL are comparable. However, devices at cryogenic temperatures are more unstable, slight oscillations are noticeable even for 2 × 25 µm devices.

Comparison of extracted g_{im} for investigated structures is depicted in figure 4.27 for 2 × 25 µm HEMTs with 80 nm gate lengths measured at 300 K.

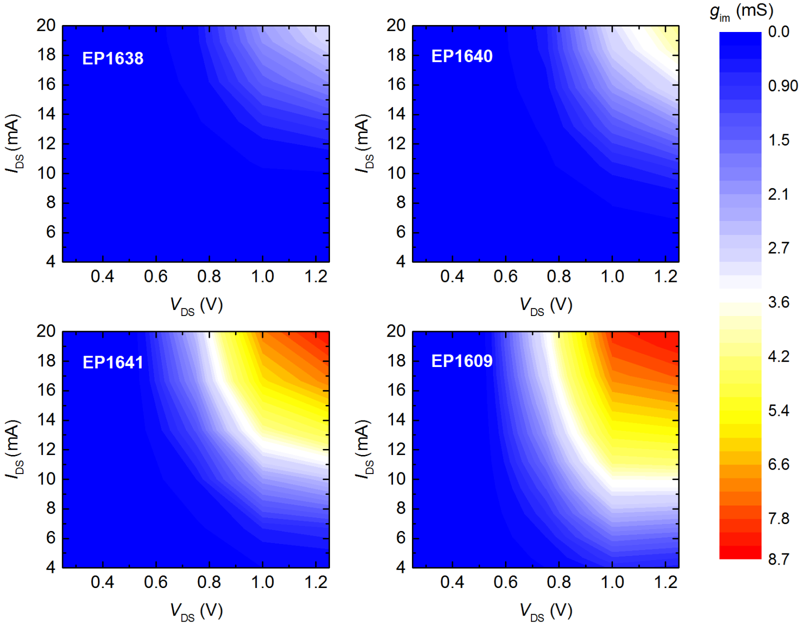

FIGURE 4.27: Comparison of impact ionization transconductance, g_{im}, for EP1638, EP1640, EP1641 and EP1609 extracted from RF measurements of 2 × 25 µm HEMTs with 80 nm gate lengths at room temperature.

As expected, the impact ionization transconductance is considerably higher for structures with higher In content or pure InAs in the channel. In comparison to the standard structure (extracted g_{im} shown in figure 4.4), the impact ionization transconductances for vertically scaled HEMTs with the same $\mathrm{Ga}_{0.32}\mathrm{In}_{0.68}\mathrm{As}$ channel (EP1638 and EP1640) are lower, most likely due to the higher gate leakage enabling generated holes to leak through the gate. The extracted impact ionization transconductances at cryogenic temperatures are omitted, due to the inability of our model to reproduce the S-parameters of unstable devices, as explained in section 2.2.6.

The extracted minimum noise figures and gains of $2 \times 25\,\mu\mathrm{m}$ HEMTs with 80 nm gate lengths are depicted in figure 4.28 for EP1638, EP1640, EP1641 and EP1609 at the low noise bias point of $V_{\mathrm{DS}} = 0.5\,\mathrm{V}$ and $I_{\mathrm{DS}} = 100\,\mathrm{mA/mm}$.

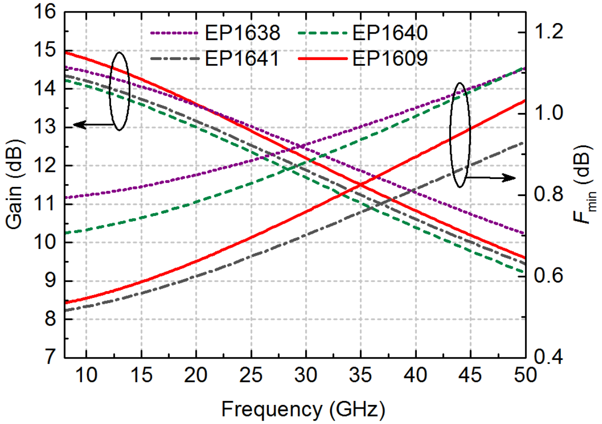

FIGURE 4.28: Gain and minimum noise figure of $2 \times 25\,\mu\mathrm{m}$ HEMTs with 80 nm gate lengths for EP1638, EP1640, EP1641 and EP1609. The noise receiver was implemented according to figure 2.15.

At the low noise bias point, all devices exhibit increased minimum noise figure at lower frequencies due to high gate leakage (above the level required for good noise performance). To fit the model and measured data, additional ideal shot noise current source had to be included on the gate side to account for the contribution of gate leakage. From figure 4.28, it can be observed that devices with 75% In or with 2 nm InAs inset in the channel have lower minimum noise figure compared to the other two epitaxial structures despite more pronounced impact ionization effects.

In conclusion, vertically scaled HEMTs offer higher f_T and f_max, although at a cost of having higher gate leakage increasing the minimum noise figure, especially at lower frequencies. However, at higher frequencies increased gate leakage might not have a significantly large effect, or its impact can be mitigated by improved channel transport properties. Further improvement of performance for vertically scaled HEMTs can be done with the increase of InAs channel inset thickness with addition of wider bandgap InP or InPAs sub-channel to compensate for increased impact ionization effects.

5

CONCLUSION

5.1 SUMMARY OF RESULTS

The performance of InP HEMTs was investigated with respect to several optimizations carried out to improve transistor noise performance. The emphasis was set on the reduction of the access resistances, and on the mitigation of the undesirable effects of impact ionization on noise performance. The most important findings are:

- The small-signal model was extended to account for the effects of impact ionization, and shows a good agreement between the measured and modeled data at room and cryogenic temperatures for the investigated epitaxial layers. For the three-layer $Ga_{0.32}In_{0.68}As/InP_{0.37}As_{0.63}/InP$ channel, an additional circuit had to be added on top of the extended small-signal model to account for different impact ionization rates at different layers. It is possible to effectively resolve in which layer the impact ionization takes place.
- The noise model was extended to account for additional low frequency noise generated by impact ionization, and shows a good agreement between modeled and measured data at room temperature.
- The extent and influence of impact ionization on HEMT performance was investigated and modeled with respect to different ratios of GaInAs and InP thicknesses in $Ga_{0.32}In_{0.68}As/InP$ composite channel. A comparison between standard $Ga_{0.32}In_{0.68}As$ and $Ga_{0.32}In_{0.68}As/InP$ channel devices clearly shows that the composite channel has superior properties at both low and high drain bias.
- A novel $Ga_{0.32}In_{0.68}As/InP_{0.37}As_{0.63}/InP$ composite channel HEMT was implemented and modeled. It features reduced impact ionization rate at high drain bias, and similar performance as the $Ga_{0.32}In_{0.68}As/InP$ composite channel HEMT at a typical low noise bias point.

- The contribution of access resistances on HEMT performance was investigated and modeled for different levels of cap layer doping and for different composition of the composite GaInAs/AlInAs cap layers.
- HEMT epitaxial layers were vertically scaled, and the influence of the channel composition on HEMT performance was investigated and modeled. A clear advantage is visible in RF performance for vertically scaled HEMTs at the cost of a reduced noise performance. For channels with high In content or pure InAs insets, transistor f_{T} and $f_{\max}$ are improved with a drawback of increased impact ionization.

5.2 OUTLOOK

Over the last few decades, vast progress was achieved in RF and noise performance of HEMTs, enabling today the construction of circuits operating at THz frequencies. A variety of semiconductor material alloys have been implemented and tested in an attempt to further improve the channel transport properties. Device dimensions were reduced, in order to increase device bandwidth, up to a point where additional reduction in minimum noise figure resulting from device scaling is not expected. Aggressive scaling of device dimensions and epitaxial layers also deteriorates carrier transport in the channel. To overcome this issue, the channel is engineered to improve carrier confinement, density and mobility by insertion of In-rich or pure InAs layers. However, due to the narrower bandgap, devices with high In content suffer from impact ionization and poorer noise performance. The results presented in the course of this work provide options to mitigate the undesirable effects of impact ionization in narrow bandgap channels.

This work identifies several potential ways to further improve the noise performance of InP HEMTs. It appears the most attractive path toward THz and generally higher operating frequencies is to exploit InAs channels in conjunction with composite channel structures to reduce impact ionization effects. Achieving the optimal HEMT will not be a simple task if one insists on good noise performance: it is a multivariate optimization problem, where small changes easily prove deleterious to noise, as shown in many of the experiments here.

Further decrease of access resistances is certainly a promising measure to reduce the minimum noise figure. Increase of the thickness and doping of the GaInAs/AlInAs composite cap should result in additional reduction of the Schottky potential barrier allowing more electrons to tunnel from the contacts into the channel. However, this is to be weighted against potential loss of the gate control over the channel. Additionally, the gate recess step will pose a challenge for thicker and higher doped cap layers. In order to fully benefit from decreased contact resistance, and to avoid channel depletion by surface traps from the area exposed by recess etching, recess width has to be kept at an optimal value with avoiding any excessive side etching. Lateral scaling of device dimensions such as reduction of source and drain spacing from 1µm to 0.75 or 0.5 µm should also help in reducing the access resistances.

The decrease of the barrier thickness for vertically scaled HEMTs increases the maximum transconductance and brings an undesirable increase of the gate leakage as a consequence of the reduced distance between the gate and the channel. Although the influence of gate leakage might not be deleterious at all operating frequencies, a potential alternative would be to insert a thin layer of insulator such as TiO_2 underneath the gate. From our experiments, with 2.5 nm TiO_2 layer, gate leakage can be decreased by an order of magnitude.

A

APPENDIX

A.1 Y-PARAMETERS OF THE EXDENDED SMALL-SIGNAL INTRINSIC EQUIVALENT CIRCUIT MODEL

Figure A.1 shows the extended small-signal intrinsic equivalent circuit model, used to model the impact ionization in Chapter 4.

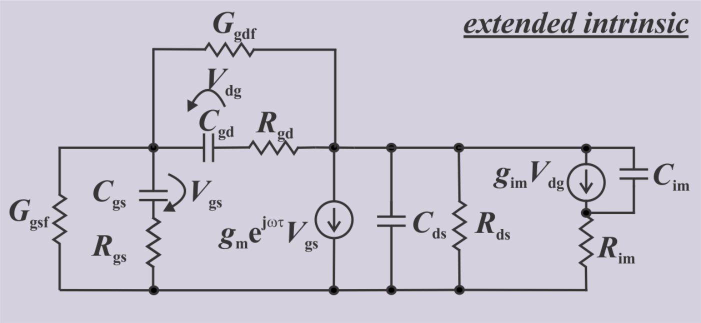

FIGURE A.1: Intrinsic small-signal equivalent circuit including circuitry modeling impact ionization.

The corresponding Y-parameters of the model are calculated as:

$$Y_{11} = \left(G_{\mathrm{gsf}} + \frac{j \cdot \omega \cdot C_{\mathrm{gs}}}{1 + j \cdot \omega \cdot R_{\mathrm{gs}} \cdot C_{\mathrm{gs}}}\right) + \left(G_{\mathrm{gdf}} + \frac{j \cdot \omega \cdot C_{\mathrm{gd}}}{1 + j \cdot \omega \cdot R_{\mathrm{gd}} \cdot C_{\mathrm{gd}}}\right)$$

$$\begin{aligned} Y_{21} = & \left(\frac{g_{\mathrm{m}} \cdot e^{-j\omega\tau}}{1 + j \cdot \omega \cdot R_{\mathrm{gs}} \cdot C_{\mathrm{gs}}}\right) + \left(\frac{g_{\mathrm{im}}}{1 + j \cdot \omega \cdot R_{\mathrm{im}} \cdot C_{\mathrm{im}}} \cdot \frac{1}{1 + j \cdot \omega \cdot R_{\mathrm{dg}} \cdot C_{\mathrm{dg}}}\right) \\ & - \left(G_{\mathrm{gdf}} + \frac{j \cdot \omega \cdot C_{\mathrm{gd}}}{1 + j \cdot \omega \cdot R_{\mathrm{gd}} \cdot C_{\mathrm{gd}}}\right) \end{aligned}$$

$$Y_{12} = -\left(G_{\mathrm{gdf}} + \frac{j \cdot \omega \cdot C_{\mathrm{gd}}}{1 + j \cdot \omega \cdot R_{\mathrm{gd}} \cdot C_{\mathrm{gd}}}\right)$$

$$Y_{22} = \left(\frac{1 + j \cdot \omega \cdot R_{\text{ds}} \cdot C_{\text{ds}}}{R_{\text{ds}}}\right) + \left(\frac{g_{\text{im}}}{1 + j \cdot \omega \cdot R_{\text{im}} \cdot C_{\text{im}}} \cdot \frac{1}{1 + j \cdot \omega \cdot R_{\text{dg}} \cdot C_{\text{dg}}}\right) + \\ + \left(G_{\text{gdf}} + \frac{j \cdot \omega \cdot C_{\text{gd}}}{1 + j \cdot \omega \cdot R_{\text{gd}} \cdot C_{\text{gd}}}\right)$$

A.2 BASICS OF IMPACT IONIZATION

Impact ionization is an electron-hole pair generation process occurring in regions with high electric fields. A carrier traveling through the high field region can gain enough energy and create additional electron-hole pairs during collisions with the lattice. The created electron-hole pair can also have high energy, and trigger additional ionization events. This is called avalanche carrier multiplication because the carrier density can increase uncontrollably. This mechanism is illustrated in figure A.2.

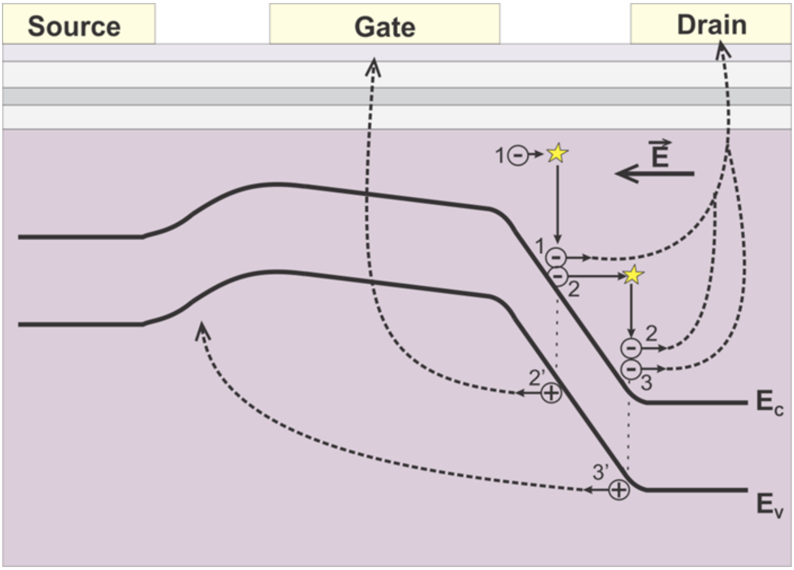

FIGURE A.2: Impact ionization process – additional electron-hole pairs are generated by high energy electrons at the drain side of the device.

The GaInAs/AlInAs/InP HEMTs suffer from impact ionization in the narrow bandgap GaInAs channel. When voltage on the drain contact is high, carriers in the channel gain enough energy to generate additional electron-hole pairs via impact ionization. Generated electrons are collected by the drain contact and cause an increase in the drain current thereby reducing the output resistance of the HEMT. Generated holes flow to the source side of the gate where they can recombine with electrons, raise the potential of the channel on the source side and shift the device threshold voltage. Some generated holes have enough energy to tunnel through the barrier and contribute to the gate current. Consequently, the gate leakage current increases significantly and forms a bell-shape (hump) in the gate current DC characteristic.

Impact ionization is responsible for strong inductive behavior of output reflection coefficient S_{22} at lower frequencies due to the phase lag between applied drain voltage and drain current. Additionally, due to the decrease of the output resistance, the forward gain S_{21} is reduced at lower frequencies. With respect to noise performance, impact ionization leads to an increase of minimum noise figure F_{min} and equivalent noise resistance R_{n} at lower frequencies.

LIST OF FIGURES

LIST OF TABLES

LIST OF ACRONYMS

2DEG	Two-Dimensional Electron Gas
ALD	Atomic Layer Deposition
CF_4	Tetrafuloromethane
DIBL	Drain Induced Barrier Lowering
DUT	Device Under Test
EDS	Energy Dispersive X-ray Spectroscopy
ESA	European Space Agency
FET	Field Effect Transistor
HEMT	High Electron Mobility Transistor
HMIC	Hybrid Microwave Integrated Circuit
LNA	Low Noise Amplfier
LRRM	Line-Reflect-Reflect-Match
MBE	Molecular Beam Epitaxy
MMIC	Monolithic Microwave Integrated Circuit
NIF	Noise Indication Factor
RIE	Reactive Ion Etching
RTA	Rapid Thermal Annealer
SCE	Short-Channel Effect
SEM	Scanning Electron Microscopy
SNR	Signal-to-Noise Ratio

SSEC	Small-Signal Equivalent Circuit
SSEEC	Small-Signal Extrinsic Equivalent Circuit
SSIEC	Small-Signal Intrinsic Equivalent Circuit
STEM	Scanning Transmission Electron Microscopy
TLM	Transfer Length Method
VNA	Vector Network Analyzer

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PUBLICATIONS

Journal Articles:

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