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Design Procedure for Compact Pulse Transformers with Rectangular Pulse Shape and Fast Rise Times

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***Abstract*—µs-range pulse modulators based on solid state technology often utilize a pulse transformer, since it could offer an inherent current balancing for parallel connected switches and with the turns ratio the modulator design could be adapted to the available semiconductor switch technology.**

In many applications as e.g. radar systems, linear accelerators or klystron/magnetron modulators a rectangular pulse shape with a fast rise time and a as small as possible overshoot is required. In reality, however, parasitic elements of the pulse transformer as leakage inductance and capacitances limit the achievable rise time and result in overshoot. Thus, the design of the pulse transformer is crucial for the modulator performance.

In this paper, a step by step design procedure of a pulse transformer for rectangular pulse shape with fast rise time is presented. Different transformer topologies are compared with respect of the parasitic elements, which are then calculated analytically depending on the mechanical dimensions of the transformer. Additionally, the influence of the core material, the limited switching speed of semiconductors and the nonlinear impedance characteristic of a klystron are analyzed.

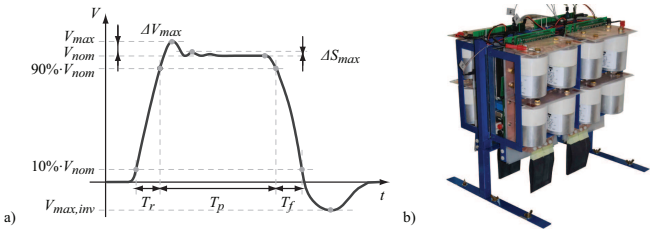

Figure 1: a) Typical pulse waveform. b) 20 MW pulse modulator.

Table I: Specification of the power modulator.

Input voltage V_{in}	1000 V
Output voltage V_{out}	170 kV
Pulse duration T_p	5 µs
Output power P_{out}	20 MW
Rise time T_r	< 500 ns
Overshoot ΔV_{max}	$< 3\,\%$
Turns ratio $N_{pri} : N_{sec}$	1 : 170

I. Introduction

In many application areas, the required output power level of test facilities in laboratories or in industry is rising and in more and more applications solid state modulators deploying for example IGBT modules, with a constantly increasing power handling capability, are utilized. In contrast to the spark gap switches, which can only be turned-on and have a limited life time and switching frequency, available fast semiconductor switches have a limited power handling capability, so that a parallel and/or series connection of the switches is required. The parallel connection of the semiconductors basically offers a more robust design due to the better capability of the switches to handle over-currents compared to over-voltages. In [1] it has been shown, that a modulator based on pulse transformer is the most suitable topology for pulses in the µs-range, since it could offer an inherent current balancing in parallel connected power semiconductors. Additionally, the turns ratio of the pulse transformer offers a degree of freedom that allows adapting the modulator design to the current and voltage ratings of available switch technology.

In applications like radar systems, linear accelerators or klystron and magnetron modulators, where a nearly rectangular pulse shape is needed, also the requirements with respect to rise times, overshoot or voltage droop are high. In Fig. 1 a) the schematic waveform of a typical power modulator's output voltage and in b) a power modulator with the specifications given in Table I are shown. Since the transformer parasitics limit the achievable rise time and define the resulting overshoot, the design of the transformer is crucial. On the one hand, due to non-ideal material properties like the limited permeability ($\mu \neq \infty$) or the limited maximum flux density B_{max} of the core material, the maximum voltage-time-product respectively the minimum cut-off frequency f_u of the pulse transformer is defined. On the other hand, in transformers no ideal magnetic coupling between windings can be achieved, which results in a certain leakage inductance L_σ.

Additionally, parasitic capacitances of the transformer define the transient voltage distribution and result in combination with L_σ in an upper cut-off frequency f_o of the transformer. Often the parasitic capacitances are summarised in one single lumped capacitor C_d as will be shown later.

The output voltage with an almost rectangular pulse shape, however, exhibits a wide frequency spectrum. In order to transfer the voltage pulse with a minimum pulse distortion, especially during the rise time, a maximum bandwidth has to be achieved, which means that the mentioned parasitics of the transformer must be minimized. Consequently, the pulse transformer is one of the key components of pulse modulators, which mainly defines the achievable rise time T_r and overshoot ΔV_{amx} of the output voltage pulse.

In this paper, a general step by step design procedure of a pulse transformer is presented. In **section II** the influence of the parasitic elements L_σ and C_d is analyzed with a standardized pulse transformer model. During the rise time this model can be simplified, which allows to derive basic design equations concerning rise time and overshoot of the pulse transformer. Based on this, in **section III** different transformer topologies are compared with respect to the fastest achievable rise time. In order to define the mechanical dimensions, the leakage inductance L_σ and the capacitance C_d are calculated analytically in **section IV**. In order to achieve faster rise time, transformers with multiple cores can be used, as described in **section V**. In **section VI** the influence of the core material properties like permeability μ, maximum flux density B and the core losses during pulse excitation is evaluated based on experimental results.

Additionally, the design of the pulse

In **section VII** the influence of the limited switching speed of semiconductors and the nonlinear impedance characteristic of a klystron is evaluated. Experimental results of the built pulse modulator are shown in **section VIII**.

II. Pulse Transformer's Equivalent Circuit

In literature numerous electrical equivalent circuits considering LF and HF properties of pulse transformers have been proposed and IEEE standardized the equivalent circuit of pulse transformers [3] as shown in Fig. 2 a). In order to simplify the analysis of the transient behavior for operation with rectangular pulse voltages, the standardized equivalent circuit can be reduced to the equivalent circuit shown in Fig. 2 b) during the leading edge if $n \gg 1$ [4]. Since the pulse rise time T_r is in the range of some 100ns, the influence of the core material, i.e. R_{Fe} and L_{mag}, can be neglected during the rise time.

Therefore, the rise time and the overshoot of the output voltage, are mainly defined by the leakage inductance L_σ and the capacitance C_d. Assuming an ideal step voltage at the primary, the output voltage $v_{out}(t)$ can be calculated with the laplace-transform as described in [4].

$$v_{out}(t) = \frac{V_g R_{load}}{R_g + R_{load}} \left[1 - e^{-at}\left(\frac{a}{k}\sinh(kt) + \cosh(kt)\right)\right] \quad (1)$$

$$\text{with} \quad k^2 = a^2 - b \quad \text{and}$$

$$2a = \frac{R_g}{L_\sigma} + \frac{1}{C_d R_{load}}, \quad b = \frac{1}{L_\sigma C_d}\left(1 + \frac{R_g}{R_{load}}\right)$$

where the damping coefficient σ of (1) is given by

$$\sigma = \frac{a}{\sqrt{b}} = \frac{C_d R_g R_{load} + L_\sigma}{2\sqrt{R_{load} L_\sigma C_d (R_g + R_{load})}}. \quad (2)$$

For pulse modulators based on capacitor discharge, the modulators's impedance R_g usually can be neglected. Thus, the damping coefficient σ can be simplified to

$$\sigma = \frac{a}{\sqrt{b}} = \frac{1}{2R_{load}}\sqrt{\frac{L_\sigma}{C_d}} \quad (3)$$

In Fig. 3 the transient behavior of the normalized output voltage during $T = \frac{\sqrt{b}}{2\pi}t$ is illustrated. A decreasing damping coefficient σ results in a faster rise time T_r. Starting from $\sigma < 1$ a tradeoff between T_r and overshoot is found. Therefore, to achieve a minimum rise time T_r, the damping coefficient σ has to be selected as small as possible while the resulting overshoot has to be still below the maximum allowed value (cf. Fig. 1a and Table I).

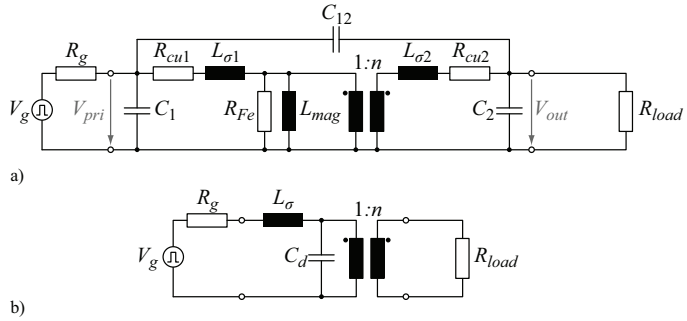

Figure 2: a) IEEE standardized equivalent circuit of a pulse transformer and b) simplified equivalent circuit during the leading edge.

A. Overshoot

Considering (3), σ depends on L_σ and C_d, i. e. on the pulse transformer's mechanical dimensions and on the load impedance R_{load}. In general, R_{load}, for example of a klystron, is defined by the application. Therefore, the pulse transformer's mechanical dimensions must be adjusted in order to fulfill the specifications of the pulse shape. Assuming a klystron load of $R_{load} = 1500\,\Omega$, for a maximum overshoot of 3% a damping coefficient of $\sigma = 0.75$ is needed (cf. (3)). Consequently, with a given R_{load} and σ, the ratio of leakage inductance L_σ and capacitance C_d is fixed by

$$2R_{load} \cdot \sigma = \sqrt{\frac{L_\sigma}{C_d}} \quad (4)$$

B. Rise Time

In addition to the overshoot, the rise time T_r of the output voltage can be derived from (1). As shown in (5), T_r is proportional to the product of L_σ and C_d.

$$T = \frac{\sqrt{b}}{2\pi}t, \quad T_r = 2\pi T_{10\%-90\%}\sqrt{L_\sigma C_d} \quad (5)$$

Factor $T_{10\%-90\%}$ depends on the selected damping coefficient σ and equals the time in which the voltage $v_{load}(t)$ rises from 10% to 90% (cf. Fig. 3). For $\sigma = 0.75$ the factor is $T_{10\%-90\%} = 0.365$. Since the rise time T_r is proportional to $L_\sigma \cdot C_d$, the parasitics have to be minimized in order to achieve the fastest possible rise time. For example, to keep the rise time below $T_r = 500\,\text{ns}$, $L_\sigma \cdot C_d$ has to be smaller than $4.75 \cdot 10^{-14}$ if $\sigma = 0.75$.

Since the load impedance is $R_{load} = 1500\,\Omega$, the ratio of L_σ and C_d is fixed and the maximum values for the specifications in Table I are: $L_\sigma < 490\,\mu\text{H}$, $C_d < 97\,\text{pF}$.

C. Design Criteria

In order to fulfill the requirements for the maximum overshoot and the maximum rise time, both a given ratio of L_σ to C_d and a maximum product of L_σ and C_d have to be guaranteed.

In general, the pulse modulator connected to the transformer's primary as well as the load connected to the secondary winding have a certain inductance L_{gen} / capacitance C_{load}, which also have to be considered. For example, typical capacitance values of klystrons are in the range of $C_{load} = 40$-$120\,\text{pF}$ [14] for the considered

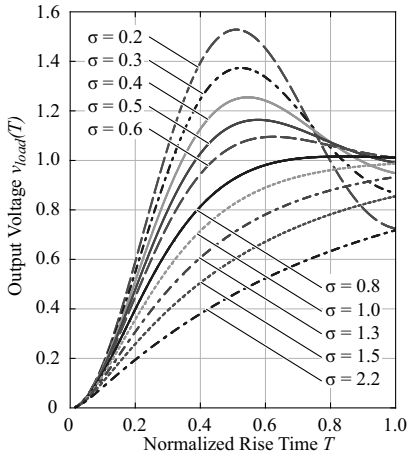

Figure 3: Transient behavior of the normalized output voltage for different damping coefficients σ.

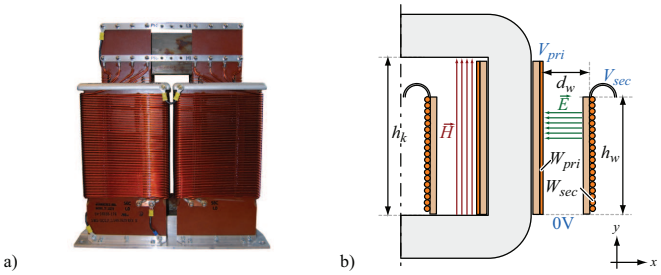

Figure 4: a) Picture of a pulse transformer with parallel winding and b) 2D drawing of one leg with simplified run of the magnetic and electric field lines.

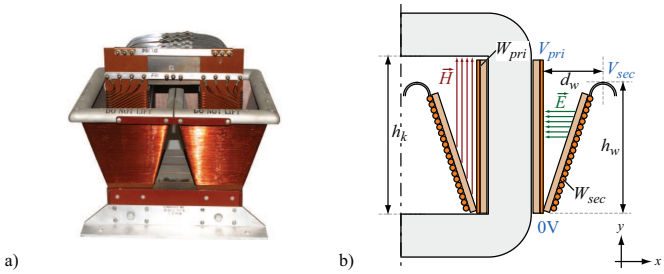

Figure 5: a) Picture of a pulse transformer with cone winding and b) 2D drawing of one leg with simplified run of the magnetic and electric field lines.

application. This means that the capacitance of the transformer must be small to meet the pulse specifications. Therefore, (4) and (5) have to be extended to

$$2R_{load} \cdot \sigma = \sqrt{\frac{L_\sigma + L_{gen}}{C_d + C_{load}}}$$
$$T_r = 2\pi T_{10\%-90\%} \sqrt{(L_\sigma + L_{gen})(C_d + C_{load})} \tag{6}$$

III. Transformer Topology

The ratio of L_σ and C_d can be varied by the mechanical dimensions of the transformer, i.e. the distances, the heights and the lengths of the windings. The product of L_σ and C_d, however, is defined by the transformer topology and can be assumed to be approximately constant [4]. Therefore, first the transformer topology resulting in the smallest $L_\sigma C_d$-product has to be selected. Afterwards, the mechanical dimensions must be calculated to achieve the needed $L_\sigma C_d$-ratio.

In the following, the $L_\sigma C_d$-product of three different transformer topologies is analyzed. The leakage inductance L_σ and the capacitance C_d are calculated with the energy stored in the magnetic & electric field.

$$E_{mag} = \frac{1}{2}\mu \int_V \vec{H}^2 \,\mathrm{d}V \equiv \frac{1}{2} L_\sigma \cdot I_{pri}^2 \tag{7}$$

$$E_{elec} = \frac{1}{2}\varepsilon \int_V \vec{E}^2 \,\mathrm{d}V \equiv \frac{1}{2} C_d \cdot V_{pri}^2 \tag{8}$$

To simplify the comparison, only the energies between the windings are considered. Finally, for the transformer topology with the smallest $L_\sigma C_d$-product a more detailed calculation of the parasitics is presented.

A. Parallel Winding

Due to the simple construction, the parallel winding topology is widely used. The primary and secondary are wound on two parallel bobbins, whose distance is defined by the required isolation. In Fig. 4 a picture and 2D drawing of the parallel winding are shown.

The leakage inductance is mainly defined by the volume and the magnetic field strength between the bobbins (cf. (7)). According to Ampére's law and assuming an ideal core material ($\mu = \infty$), the magnetic field strength $\vec{H}$ in the core window is given by the primary current times the number of turns $N_{pri} \cdot I_{pri}$ and the height of the core h_k.

$$|\vec{H}| = \frac{N_{pri} I_{pri}}{h_k} \tag{9}$$

Using (7) and (9), the stored magnetic energy E_{mag} between the windings W_{pri} and W_{sec} can be approximately calculated by

$$E_{mag} = \frac{1}{2}\mu \left(N_{pri} I_{pri}\right)^2 \frac{l_w \cdot d_w}{h_k} = \frac{1}{2} L_\sigma I_{pri}^2, \tag{10}$$

and the resulting leakage inductance $L_{\sigma,parallel}$ is

$$L_{\sigma,parallel} = \mu \frac{N_{pri}^2 \cdot l_w \cdot d_w}{h_k}. \tag{11}$$

To calculate the capacitance C_d, a linear voltage distribution $V_{pri}(y)$ and $V_{sec}(y)$ is assumed across the windings.

$$V_{pri}(y) = \frac{y}{h_w} V_{pri}; \qquad V_{sec}(y) = \frac{y}{h_w} V_{sec} \tag{12}$$

Therewith, the voltage difference between the primary and secondary winding depending on the vertical position y is $\Delta V(y) = V_{sec}(y) - V_{pri}(y)$.

Due to the voltage difference between the windings W_{pri} and W_{sec}, the electric field lines run approximately horizontally (cf. Fig. 4 b)). Thus, the electric field $\vec{E}(y)$ depending on the y-position is

$$|\vec{E}(y)| = \frac{\Delta V(y)}{d_w} = \frac{V_{pri} \cdot (n-1) \cdot y}{h_w \cdot d_w} \approx \frac{V_{sec} \cdot y}{h_w \cdot d_w}. \tag{13}$$

Considering (8), the stored energy between the windings W_{pri} and W_{sec} and therewith the capacitance C_d are calculated.

$$\begin{aligned} E_{elek} &= \frac{1}{2}\varepsilon \int_0^{l_w} \int_0^{h_w} \int_0^{d_w} \left(\frac{V_{sec} \cdot y}{h_w \cdot d_w}\right)^2 \mathrm{d}x \,\mathrm{d}y \,\mathrm{d}z \\ &= \frac{1}{6}\varepsilon V_{sec}^2 \cdot \left(\frac{l_w \cdot h_w}{d_w}\right) = \frac{1}{2} C_d \cdot V_{pri}^2 \end{aligned} \tag{14}$$

$$C_{d,parallel} = \frac{1}{3} \cdot \varepsilon \cdot \left(\frac{N_{sec}}{N_{pri}}\right)^2 \cdot \left(\frac{l_w \cdot h_w}{d_w}\right) \tag{15}$$

Finally, the $L_\sigma C_d$-product of the transformer topology with parallel windings is

$$L_{\sigma,parallel} C_{d,parallel} = \frac{1}{3} \cdot \varepsilon\mu \frac{N_{sec}^2 \cdot l_w^2 \cdot h_w}{h_k}. \tag{16}$$

B. Cone Winding

Since the distance between the windings of the transformer with parallel winding is constant but the voltage is increasing linearly in y-direction, the electric field between the windings also increases linearly. In order to achieve a constant electric field $\vec{E}(y)$ the distance between the windings d_w has to be linearly decreased for smaller

voltage differences, which results in a cone winding [4], [15] as shown in Fig. 5.

Compared to the parallel winding, the volume between the windings and therefore also the leakage inductance L_σ can be reduced by a factor of two. However, due to the smaller distance between the windings C_d is increases.

To calculate the leakage inductance L_σ of the cone winding, again, a constant magnetic field in y-direction is assumed (cf. Fig. 5), which was confirmed by FEM-simulation as long as $d_w \ll h_w$.

Considering (7), the stored magnetic energy E_{mag} and the resulting leakage inductance $L_{\sigma,cone}$ are

$$E_{mag} = \frac{1}{4}\mu \left(N_{pri} I_{pri}\right)^2 \frac{l_w \cdot d_w}{h_k} = \frac{1}{2} L_\sigma I_{pri}^2 \tag{17}$$

$$L_{\sigma,cone} = \frac{1}{2} \cdot \mu \frac{N_{pri}^2 \cdot l_w \cdot d_w}{h_k}. \tag{18}$$

Due to the linearly increasing distance $d_w(y)$ and the voltage distribution $\Delta V(y)$ in y-direction, the electric field $\vec{E}$ between the winding is constant and runs approximately parallel to the x-direction (cf. Fig. 5 b)).

Hence, the stored electric energy (8) for a cone winding and the capacitance C_d are

$$E_{elek} = \frac{1}{4}\varepsilon V_{sec}^2 \cdot \left(\frac{l_w \cdot h_w}{d_w}\right) = \frac{1}{2} C_d \cdot V_{pri}^2 \tag{19}$$

$$C_{d,cone} = \frac{1}{2} \cdot \varepsilon \cdot \left(\frac{N_{sec}}{N_{pri}}\right)^2 \cdot \left(\frac{l_w \cdot h_w}{d_w}\right) \tag{20}$$

Finally, the resulting $L_\sigma C_d$-product of the cone winding is

$$L_{\sigma,cone} C_{d,cone} = \frac{1}{4} \cdot \varepsilon\mu \frac{N_{sec}^2 \cdot l_w^2 \cdot h_w}{h_k}. \tag{21}$$

Compared to the parallel winding, the $L_\sigma C_d$-product can be reduced by $25\,\%$, which results in an rise time improvement of $13.4\,\%$.

C. Foil Winding

Finally, for the primary W_{pri} and secondary W_{sec} foil windings are considered. The secondary is directly wound on the primary winding as shown in Fig. 6. For the isolation of the turns a material with a low permittivity is used.

The thickness d_{iso} of the isolation can be kept small, since the voltage difference between two consecutive turns is just $V_{w,w} = V_{sec}/N_{sec}$. However, due to the increasing voltage difference between the turns and the core, the winding's height is linearly decreased from $h_{w,1}$ to $h_{w,2}$ (cf. Fig. 6 b)). The total thickness d_w of the winding is defined by the thickness of the isolation d_{iso} and the foil d_{cu} times the number of turns.

The leakage inductance L_σ of the foil winding is calculated again with the stored magnetic energy (cf. (7)). Based on Ampére's law, the magnetic field is gradually increasing with the number of turns n_L, since the enclosed amount of current is increasing gradually (cf. Fig. 6).

$$\vec{H}(n_L) = \frac{n_L I_{sec}}{h_k} \tag{22}$$

The total magnetic energy is the sum of all energies between two consecutive turns, which is

$$\begin{aligned} E_{mag} &= \frac{1}{2}\mu V(n_L) \sum_{n_L=1}^{N_{sec}} \vec{H}(n_L)^2 = \frac{1}{2}\mu \frac{I_{sec}^2}{h_k^2} V(n_L) \sum_{n_L=1}^{N_{sec}} n_L^2 \\ &\approx \frac{1}{4}\mu \left(N_{pri} I_{pri}\right)^2 \frac{l_w \cdot d_w}{h_k} = \frac{1}{2} L_\sigma I_{pri}^2. \end{aligned} \tag{23}$$

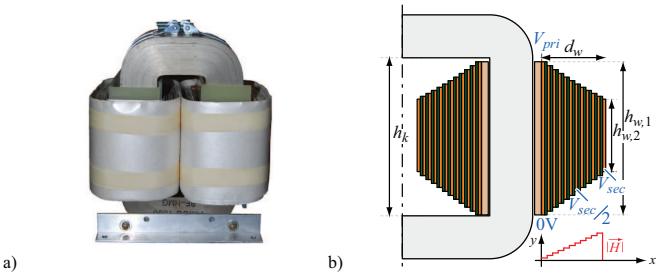

Figure 6: a) Picture of a pulse transformer with cone winding and b) 2D drawing of one leg.

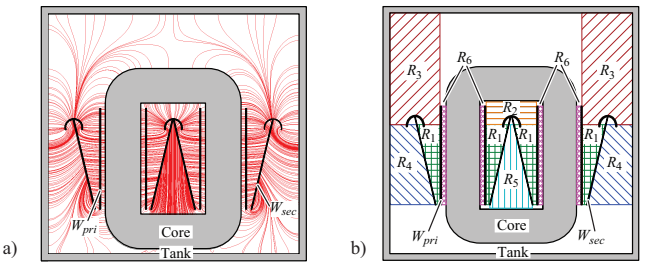

Figure 7: a) Electric field $\vec{E}$ of a transformer with cone winding in a tank. b) Six relevant regions for calculating capacitance C_d.

Thus, the resulting $L_{\sigma,foil}$ is

$$L_{\sigma,foil} = \frac{1}{2} \cdot \mu \frac{N_{pri}^2 \cdot l_w \cdot d_w}{h_k}. \tag{24}$$

Capacitance C_d can be calculated as a series connection of parallel-plate capacitors between consecutive turns $C_{w,w}$. The distance of the plates equals d_{iso}, which can be expressed by the total winding thickness.

$$d_{iso} = \frac{d_w}{(k+1) \cdot N_{sec}} \quad \text{where} \quad k = d_{cu}/d_{iso} \tag{25}$$

Assuming a constant winding height $h_w = (h_{w,1} + h_{w,2})/2$, the capacitance C_d for the foil winding results in

$$C_{d,foil} = (k+1) \cdot \varepsilon \cdot \left(\frac{N_{sec}}{N_{pri}}\right)^2 \left(\frac{h_w \cdot l_w}{d_w}\right) \tag{26}$$

and the $L_\sigma C_d$-product is

$$L_{\sigma,foil} C_{d,foil} = \frac{k+1}{2} \cdot \varepsilon\mu \frac{N_{sec}^2 \cdot l_w^2 \cdot h_w}{h_k}. \tag{27}$$

Considering only the stored magnetic and electric energy between the windings W_{pri} and W_{sec}, the smallest $L_\sigma C_d$-product and therefore the fastest T_r can be achieved for the transformer with a cone winding. Since the considered volume contains the major share of the magnetic and electric energy, the calculated $L_\sigma C_d$-product is a reliable indicator for selecting the best transformer topology.

IV. Parasitics Calculation

In a next step, also the magnetic and electric fields between the winding and the core as well as the electric fields between the windings and the enclosing wall of a tank are considered in order to obtain a more precise model for designing the transformer. For example, in Fig. 7 a) the resulting electric field $\vec{E}$ for a transformer placed in a tank is shown.

Fig. 8 a), which shows a measured and a calculated waveform considering only the energy between the windings, clearly indicates

the mismatch between measurement and simplified calculation of the parasitics. Since only the electric energy between the windings is considered, C_d is too small and results in a too small overshoot predicted by the transformer model.

A. Parasitic Capacitance

To improve parasitics calculation the energy outside the windings is considered in the following. As shown in Fig. 7 b), the space around the transformer is divided into six relevant regions R_1 to R_6. With geometric approximations, the stored energy in each region can then be calculated analytically. In [2] the detailed calculation of the distributed capacitances depending on the mechanical dimensions of the transformer is investigated. The output voltage predicted with the improved model is shown in Fig. 8 b).

The energies in all regions $R_1 - R_6$ have to be calculated and with the total electric energy, C_d can be determined. As an example, in Table II the relative stored electric energy in each region for a transformer with cone winding with and without tank is listed. There, it is assumed, that the distance between the upper end of the secondary winding and the tank is the same as the distance between primary and secondary, which is d_w.

Table II clearly shows that only about a quarter of the total electric energy is stored between the windings. Considering only R_1, in practice, the design of the transformer would result in a too large overshoot, since the real distributed capacitance would be much larger than the calculated one.

B. Leakage Inductance

Compared to the capacitance C_d, the calculation L_σ is more challenging, since there no simple division into subregions is possible. To precisely calculate the stored magnetic energy, FEM simulations are used. In Fig. 9 the energy density for a pulse transformer with cone winding is illustrated.

The simulation shows, that the major part of the magnetic energy is concentrated in the region between the windings and the magnetic field $|\vec{H}|$ is almost constant. Therefore, the simple calculation of L_σ in section II (18) already matches the real leakage inductance well. Compared to FEM simulation the relative error of the simple equation is in the range of $10 - 20\%$ if $d_w \ll h_w$.

Table II: Relative stored electric energy of each region $R_1 - R_6$ with and without tank.

Region	R_1	R_2	R_3	R_4	R_5	R_6
With tank	22.6%	6.4%	44.4%	25.2%	0.6%	0.8%
Without tank	33.9%	9.6%	44.3%	10.1%	0.9%	1.2%

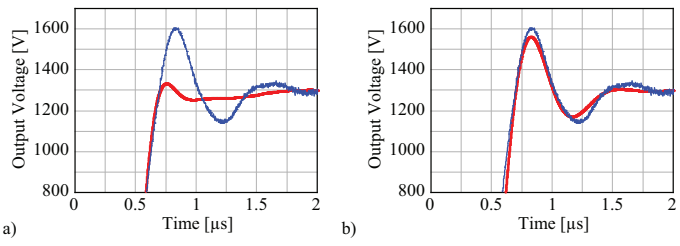

Figure 8: Comparison of measured and calculated output voltage if a) only the energy between the winding and b) the energy in all regions is considered.

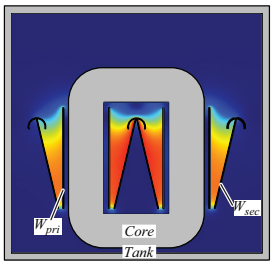

Figure 9: Magnetic energy density for a pulse transformer with cone winding.

V. Interconnection of Pulse Transformers

Instead of one pulse transformer also several pulse transformers could be used, which are connected either in parallel/parallel, parallel/series, series/parallel or in series/parallel on the primary/secondary.

A. Parallel or Series Connection of Pulse Transformers

In Fig. 10 the equivalent circuits of two parallel a) and two series b) connected identical pulse transformers are shown. There, also an interconnection of an arbitrary number of transformers would be possible. However, considering Fig. 10, it is directly obvious that no reduction of the $L_\sigma C_d$-product and the rise time T_r can be achieve by such an interconnection.

With the parallel connection of the secondaries, for example, the total leakage inductance L_σ is halve as big as with one transformer, whereas the total capacitance C_d doubles. The only advantages are the reduction of winding resistance and the more flexible design if several switches have to be connected to the pulse transformer. Additionally, the transformer geometry will change, since the ratio of L_σ to C_d is changed by a factor of four. However, the costs and the losses of the core material will increase.

B. Multiple Core / Matrix Transformers

In contrast to parallel or series connection of multiple pulse transformers a reduction of the $L_\sigma C_d$-product and the rise time T_r can be achieve if a pulse transformer with multiple cores is used, which are usually called matrix transformer, fractional turn transformer, split-core transformer or voltage adder [1], [5]–[10].

In Fig. 11 a) the top view of two in series connected pulse transformers is shown, where $N_{pri} = 1$ and $N_{sec} = n/2$. As mentioned before, by connecting transformers in series or parallel no improvements regarding T_r can be achieved. However, instead

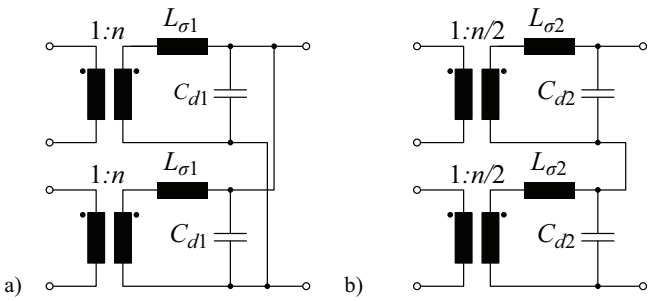

Figure 10: Equivalent circuit of two identical pulse transformers, which are a) connected in parallel and b) connected in series.

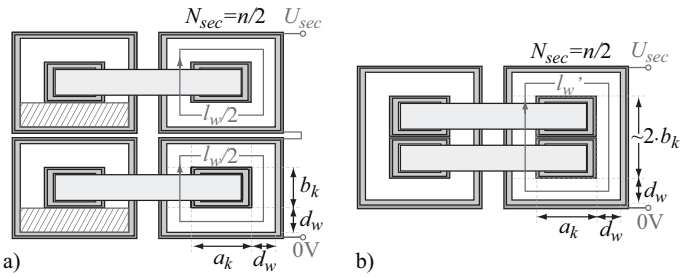

Figure 11: Top view of a) series connected pulse transformers with $N_{sec} = \frac{n}{2}$ and winding length l_w and b) pulse transformer with two cores and reduced winding length l'_w.

of connecting the secondaries in series, both secondaries can be combined to one secondary which encloses both cores, whereas some volume between the primary and secondary winding is saved (cf. Fig 11 b)). The saved volume directly results in a reduced leakage inductance compared to the series connection of the standard transformers. For this transformer configuration the conversion ratio between the primary and secondary voltage is not only defined by the turns ratio n but also by the ratio of enclosed core areas A_{pri} and A_{sec} (cf. (28)) [1].

$$\frac{V_{out}}{V_{in}} = \frac{N_{sec}}{N_{pri}} \cdot \frac{A_{sec}}{A_{pri}}. \tag{28}$$

Since T_r is proportional to the winding length, the reduction of T_r can directly be calculated by the winding length's reduction.

$$\begin{aligned} l_w &= 4 \cdot a_k + 4 \cdot b_k + 8 \cdot d_w \\ l'_w &= 2 \cdot a_k + 4 \cdot b_k + 4 \cdot d_w \end{aligned} \tag{29}$$

For the considered transformer the distance between primary and secondary is $d_w = 2.5cm$ and the core dimensions are $ak = bk = 5cm$. Consequently, the winding length of the transformer was reduced from $l_w = 60cm$ to $l'_w = 40cm$, which results in a T_r reduction of 33%.

In order to further reduce the rise time, additional cores could be used. However, the relative improvement decreases for increasing number of cores, whereas the costs for the core material increase.

VI. Core material

Beside the winding topology, the selection of the core material is crucial, since non-ideal material properties like the limited permeability ($\mu \neq \infty$) or the limited B_{max} directly influence the achievable bandwidth and therefore the performance of the pulse transformer. With a higher B_{max}, for example, the core cross section can be reduce, which results in smaller parasitics and therefore in faster rise times.

In Table III different core materials are listed [11]. There, with cobalt-iron alloys the highest flux densities can be achieved. Due the high prices, however, this materials is mainly used in military or aerospace applications [12]. Iron and silicon-iron alloys are the cheapest core material, where the second highest flux density can be achieved. Unfortunately, these materials also have the highest core losses. Nickel and nickel-iron alloys result in the lowest core losses, which only can be achieved with amorphous and nanocrystalline materials [13].

For the considered pulse transformer only silicon-iron alloys, due to the high flux density and the low cost, as well as iron based

Table III: Core materials and maximum flux density B_{max} [11].

CoFe (35%-65%)	2.43T
Fe	2.16T
SiFe (3%)	2T
Ni (75%)	0.6T
NiFe (50%-50%)	1.6T

Table IV: Analyzed core materials and manufacturer.

Finemet FT3-M (nanocrystalline)	Hitachi
2605SA1 (amorphous)	Metglas
SiFe alloy (3%)	e.g. Magnetics

amorphous and nanocrystalline core materials, due to the low losses, were analyzed (cf. Table IV).

The measured hysteresis curve of the materials listed in Table IV are shown in Fig. 12 for a pulse excitation of $5\,\mu s$. With silicon-iron a $B_{sat} = 1.73T$ was achieved. Since the flux density defines the needed core cross section, compared to Finemet (1.18T) and 2605SA1 (1.47T) the core cross section of silicon-iron would be 46% respectively 17% smaller.

Due to the core losses - which are given by the area of the hysteresis curve - the flux excitation is usually much below the maximum flux density. As shown in Fig 12, SiFe has the largest and Finemet the smallest area in the hystersis curve. Therefore, for a proper selection of the core material beside B_{max} also the core losses have to be considered, since the efficiency can be increased and the cooling effort is reduced. However, it has to be mentioned that the core losses are not only defined by the selected material. As shown in Fig. 13 a), for example, the thickness of the metal tape used in tape wound cores or the pulse duration, as shown in Fig. 13 b), can strongly influence the core losses. Therefore, in order to compare different core materials regarding core losses, the same conditions must be applied.

VII. Design Procedure

As described in section II, T_r and the overshoot mainly depend on the ratio and the product of the total series inductance $L_{gen} + L_\sigma$ and the total capacitance $C_d + C_{load}$. There, the basic equations were derived based on an ideal rectangular input voltage and a resistive load. However, in reality, the switching times of power semiconductors like IGBT modules are in best case in the range of some $100\,ns$. Consequently, due to the reduced voltage slope of the input voltage also the rise time is increased, which results in a decreased overshoot.

In addition, the impedance characteristic of the klystron is non-linear and decreases with voltage, which also leads to an additional

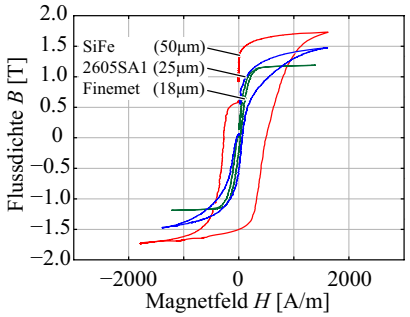

Figure 12: Measured hysteresis curve with flux excitation to B_{max}.

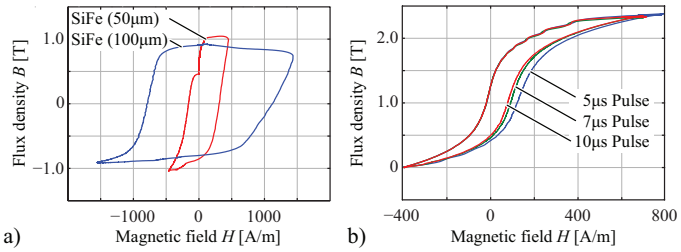

Figure 13: Measured hysteresis curve of a) SiFe alloy with tape thicknesses of $50\,\mu\mathrm{m}$ and $100\,\mu\mathrm{m}$ and b) of 2605SA1 for different pulse durations of $5\,\mu\mathrm{s}$, $7\,\mu\mathrm{s}$ and $10\,\mu\mathrm{s}$.

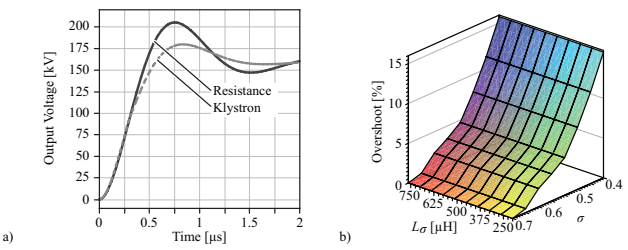

Figure 15: a) Comparison of the transient responses for a klystron load and a resistive load. b) Relative difference in overshoot for a turn-on time of $T_{on} = 300\,\mathrm{ns}$.

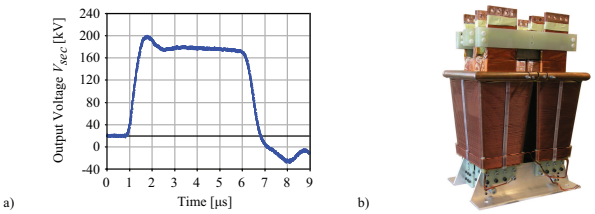

Figure 16: a) Measured output voltage waveform and b) designed pulse transformer for the specifications given in Fig. 1.

damping. Therefore, the influence of these effects has to be analyzed, since the design criteria like the needed damping coefficient σ and the resulting T_r are changed.

A. Influence of Power Semiconductor Switching Speed

To calculate the influence of the limited switching speed of the power semiconductor on T_r and the overshoot, the real input voltage is approximated by a trapezoidal voltage. According to section II, the output voltage $v(t)$ is again calculated with the laplace-transform and the equivalent circuit shown in Fig. 2 b).

In Fig. 14 a) the resulting transient responses of the output voltage for different turn-on times T_{on} respectively voltage slopes of $T_{on} = 0\,\mathrm{ns}$, $T_{on} = 120\,\mathrm{ns}$, $T_{on} = 300\,\mathrm{ns}$ and $T_{on} = 500\,\mathrm{ns}$ and for $L_\sigma = 250\,\mu\mathrm{H}/C_d = 200\,\mathrm{pF}$ are illustrated. Due to the increased T_{on}, T_r is increased whereas the overshoot is decreased.

There, the relative reduction of the overshoot is not only depending on the switching speed T_{on} and the ratio of L_σ and C_d but also on the absolute values of L_σ and C_d (cf. Fig. 14 b)).

As shown in Fig. 14 a), for T_{on} in the range of $\approx 100\,\mathrm{ns}$ the influence of the limited switching speed can be neglected, which in the worst case results in a relative overshoot reduction of less than 0.4%. However, for switching times above $T_{on} \approx 300\,\mathrm{ns}$ the limited switching speed must be considered (cf. Fig. 14).

B. Influence of Nonlinear Klystron Impedance

In general, for the design and the initial operation of the power modulator, the klystron is substituted by an equivalent resistive load R_{load}. On the one hand, this substitution simplifies the design of the system and on the other hand, the klystron is an expensive and sensitive amplifier, which can be easily damaged during initial tests.

However, for the design of the power modulator, especially of the pulse transformer, the nonlinear impedance characteristic of the klystron has to be considered. As described in [16], [17], the klystron results in an higher damping compared to the equivalent resistance,

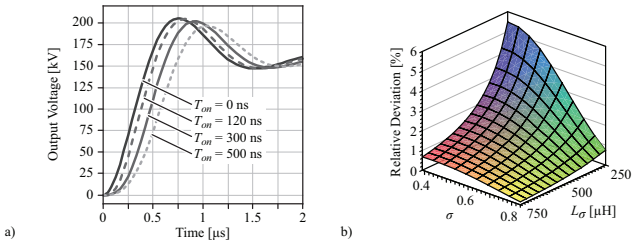

Figure 14: a) Transient responses for different turn-on times T_{on} of the semiconductor and b) relative difference in overshoot for a turn-on time of $T_{on} = 300\,\mathrm{ns}$.

whereas during the rising edge the damping coefficient changes from 0.6 to 0.9 due to the nonlinear impedance. Therefore, with a klystron load a smaller damping coefficient σ is needed compared to the equivalent resistive load.

According to [16], the klystron's impedance can be modelled by

$$I_k = k \cdot V_k^{\frac{3}{2}} \tag{30}$$

where k is the perveance of the klystron.

Considering (30), the klystron current I_k decreases more than linear with increasing klystron voltage, which results in an decreasing resistance for higher voltages and therefore in an decreasing overshoot compared to a linear load. The resulting transient responses for a klystron load and a resistive load are shown in Fig. 15 a) assuming $L_\sigma = 250\,\mu\mathrm{H}$ and $C_d = 200\,\mathrm{pF}$. The klystron leads to a significantly reduced overshoot compared to a resistive load.

Since the overshoot of 3% is specified for a klystron load, for the equivalent resistive load the pulse transformer has to be designed with an much higher overshoot, which is in this case 11%. Compared to the calculation in section II, the damping coefficient has to be decreased from $\sigma = 0.75$ to $\sigma = 0.58$.

In contrast to the limited switching speed, the influence of the klystron load on the overshoot does not depend on the absolute values of L_σ and C_d but only depends on the damping coefficient σ, as shown in Fig. 15 b).

VIII. Experimental Results

In Fig. 16 the measured output voltage and the built pulse transformer for a $20MW$ power modulator with a klystron load is shown. The measured T_r is below $500\,\mathrm{ns}$ and the overshoot with resistive load is 10.4%. Due to the larger damping, with the klystron the resulting overshoot will be below 3%.

IX. Conclusion

In this paper, a step-by-step design procedure of a pulse transformer for rectangular pulse shapes and a fast rise time is presented. Based on the transformer model, it could be seen that the rise time of

transformers is proportional to the product of the leakage inductance L_σ and the parasitic output capacitance C_d of the pulse transformer. This product is calculated for three different transformer topologies: parallel, cone and foil winding concepts and it is shown that with a cone winding the fastest rise time can be achieved.

The resulting overshoot is defined by the $L_\sigma C_d$-ratio. For the calculation of these parasitics an improved calculation procedure is proposed and validated by measurements.

In addition to the transformer parasitics, also the nonlinear impedance characteristic of a klystron and the limited switching speed of semiconductors have to be considered in the design of the transformer as it is shown in the paper and validated by measurement results.

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