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Analysis and design of an efficient, fully integrated 1–8 GHz traveling wave power amplifier in 180 nm CMOS

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Traveling wave amplifiers (TWAs) offer the advantage of broadband amplification and a closed set of equations that allow deriving the RF gain by means of treating TWAs as discrete transmission line approximations. Up to now, however, the significant losses associated with CMOS integrated inductors have been neglected. This work presents a new approach for determining the transmission line losses and phase constants that will bring about an enhanced gain prediction accuracy. The theory is verified by means of a realized design example. The working principle of the integrated DC supply inductor is discussed, whose performance is based on the inductors self-resonance effect. When applying a supply voltage V_{dd} *of 2.4 V, the measured compression point* P_{1dB} *and the power added efficiency PAE at 2.4 GHz amount to 16.9 dBm and 19.6%, respectively. At 5.5 GHz, a value of 16.6 dBm for* P_{1dB} *and an associated PAE of 13.9% are achieved. The peak RF gain for these output power values reaches 11 dB, and values greater than 8 dB are obtained up to 7 GHz.*

Keywords: Distributed amplifiers, Power amplifiers, CMOS analog integrated circuits, Traveling wave amplifiers, Transmission lines

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I. INTRODUCTION

A trend that is developing in recent years is the requirement for mobile RF frontends to accommodate several RF transmission standards. From a power amplifier (PA) perspective, multi-standard signal transmission at frequencies of 2.4 GHz (802.15.1) up to 5.725 GHz (802.11.x) requires broadband amplifiers such as e.g. traveling wave amplifiers (TWAs). The TWA principle, first introduced by Percival [1] and Ginzton *et al.* [2], was at the beginning envisaged for circuit realizations by means of vacuum tubes, discrete inductors, and capacitors. Ayasli *et al.* [3] and Beyer *et al.* [4] developed the original equations set further for the accommodation of the structural conditions that arise when implementing TWAs in GaAs FET technology. With the high substrate resistance of GaAs, the parasitic losses associated with the inductors could be neglected and the dominant loss factor reducing the RF gain versus frequency was the input gate source resistance R_{gs}. Given this background, the developed equation sets were satisfactorily adequate to predict the achievable gain bandwidth product (GBW) of TWAs.

With the rise of CMOS integration as the major circuit technology nowadays, this, unfortunately, is no longer the case. Parasitic series and parallel losses associated with the integrated inductors significantly influence the overall circuit behavior. This is particularly true for TWA architectures, which heavily rely on integrated inductors to approximate the input and output transmission lines.

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In this work, we propose a practical analytical solution for TWA architectures that incorporates the dominant loss factors of CMOS integrated inductors. A discrete transmission line model is presented that comprises resistive, capacitive, and inductive effects occurring in CMOS TWA realizations. Based on this model, the associated transmission line damping factor and phase constant are calculated and used for the derivation of the small signal gain. The RF gain is then weighted with the reductions due to non-ideal matching conditions at the input and output port versus frequency.

Section II will present details of the amplifier design and the derivation of the RF gain function, and treats the impact of the different loss factors on the transmission line. The overall architecture will be discussed and an analysis presented that explains the instrumental self-resonant effect of the DC supply coil in order to decouple the DC path RFwise. Section III compares the analysis, simulation, and measurement results. The work ends with a comparison with the state-of-the-art and the conclusion.

II. CIRCUIT ANALYSIS AND DESIGN

Figure 1 shows a schematic drawing of the TWA. The TWA structure creates a discrete transmission line approximation for the input and output lines by using the transistor input and output capacitances C_{gs} and C_{ds} together with in-series-connected inductors. Additional parallel capacitances C_x in the output line compensate for the smaller C_{ds} values and help achieve balanced phase velocities through all signal paths from the input to the output, assuring constructive RF signal addition. The circuit is realized in 180 nm IBM CMOS technology. The implemented design employs a cascode gain cell, which offers superior amplification in comparison to common source gain cells. The

reason why the number of gain cells is chosen as 4 will be explained later. The DC supply path is realized through the inductor L_{DC}. Figure 1, however, omits the series and parallel losses of the integrated inductors, which are a result of the finite metal conductivity and the capacitive coupling to the substrate, respectively.

Figure 2 shows an inductor equivalent model including the dominant parasitics in the oxide and substrate layer, C_{ox}, C_{si}, and R_{si}. The resulting parallel impedances Y_p to the ground are calculated in equation (1) and transformed into a better manipulating form for later derivations (2). The component values for the applied inductors in the input and output lines were determined using Cadence. The *S*-parameters of the parasitic IBM model were matched to the *S*-parameters of the proposed model in the desired frequency range from DC to 10 GHz. The resulting component values are displayed in the Appendix:

$$Y_{p_{l,r}} = \frac{sC_{ox,l,r}(1 + sC_{si,l,r}R_{si,l,r})}{1 + sR_{si,l,r}(C_{ox,l,r} + C_{si,l,r})}, \tag{1}$$

$$G_{p_{l,r}} = \mathrm{Re}(Y_{p_{l,r}}), \quad C_{p_{l,r}} = \frac{\mathrm{Im}(Y_{p_{l,r}})}{\omega}. \tag{2}$$

Equations (3) and (4) show the obtained equivalent components for an adapted cascode model. For the output side of the cascode, C_{ds} and R_{ds}, respectively, G_{ds} are derived for the accustomed MOSFET small-signal representation. For the input side, the serially connected components R_{gs} and C_{gs} are transferred in a parallel representation G^o_{gs} and C^o_{gs}:

$$\begin{aligned} G^o_{gs} &= \mathrm{Re}(Y_{11}), \quad C^o_{gs} = \frac{\mathrm{Im}(Y_{11})}{\omega}, \\ g^o_m &= \mathrm{Re}(Y_{21}) + j\mathrm{Im}(Y_{21}), \end{aligned} \tag{3}$$

$$Y_{12} \cong 0, \quad C_{ds} = \frac{\mathrm{Im}(Y_{22})}{\omega}, \quad G_{ds} = \mathrm{Re}(Y_{22}). \tag{4}$$

Simultaneously, the transconductance g^o_m remains no longer real but also contains a complex part. The parameters can be read out directly from a Cadence *Y*-parameter simulation. The results are valid for negligible Y_{12} values, being the case for cascode gain cells. The values, simulated with Cadence and shown in the Appendix, are saved as solution vectors from DC to 10 GHz for the complex valued calculations in Matlab and result in a steady-state solution for the frequency range considered.

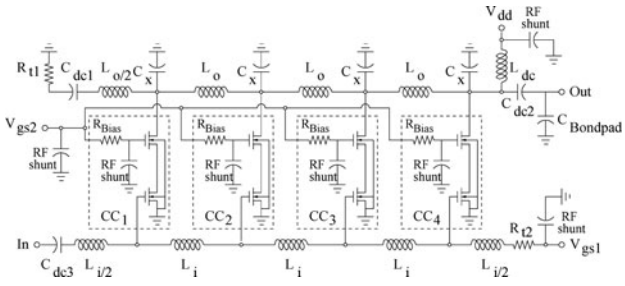

Fig. 1. Schematic representation of the realized TWA structure.

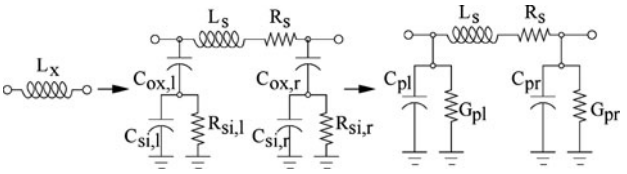

Fig. 2. Inductor model including parasitic losses.

Figure 3 depicts the derived small signal model for the discretized input and output transmission line elements, omitting the complex transconductance. Adding the components up results in the elements $L_{si,o}$, $R_{si,o}$, $C_{pi,o}$, and $G_{pi,o}$ as derived in the following equations:

$$C_{po} = C_x + C_{ds} + C_{pl} + C_{pr}, \tag{5}$$

$$G_{po} = G_{ds} + G_{pl} + G_{pr}, \tag{6}$$

$$C_{pi} = C^o_{gs} + C_{pl} + C_{pr}, \tag{7}$$

$$G_{pi} = G^o_{gs} + G_{pl} + G_{pr}. \tag{8}$$

These equivalent circuits for the input and output lines are the same as those used for the well-known telegraph equation. The complex propagation constant $\gamma_{g,d}$ for the telegraph equation can be calculated by (9); the damping factor and phase constant of the lines can then be derived by extracting the complex square root as shown in (10). The complex roots generally yield four results $\pm\alpha_{g,d} \pm \beta_{g,d}$. Being only interested in the absolute values $\alpha_{g,d}$ and $\beta_{g,d}$, the solution is unambiguous:

$$\begin{aligned} \gamma_{g,d} &= \sqrt{(R_{si,o} + j\omega L_{si,o})(G_{pi,o} + j\omega C_{pi,o})} \\ &= \alpha_{g,d} + j\beta_{g,d} \end{aligned} \tag{9}$$

$$\sqrt{A + jB} = \sqrt{A^2 + B^2}\,\exp\left(\frac{j}{2}\arctan\left(\frac{B}{A}\right)\right). \tag{10}$$

Having derived g^o_m, $\alpha_{d,g}$, $\beta_{g,d}$, Z_d and Z_g and knowing the number of stages n, the equation for the RF-gain G presented by Ayasli *et al.* [3] can be applied, written down, slightly adapted for the complex transconductance, in the following equation:

$$Z_d \cong \sqrt{\frac{L_{so}}{C_{po}}}, \quad Z_g \cong \sqrt{\frac{L_{si}}{C_{pi}}}, \tag{11}$$

$$G = Z_d Z_g \left| \frac{g^o_m \gamma_g [\exp(-\gamma_g n) - \exp(-\gamma_d n)]}{\gamma_g^2 - \gamma_d^2} \right|^2. \tag{12}$$

Equation (12) ideally postulates an infinite number of stages n to approximate the transmission line by discrete line elements. Four elements are considered sufficient to assume idealized transmission line approximation conditions. Furthermore, equation (12) assumes perfect matching conditions and does not consider power reflections that occur

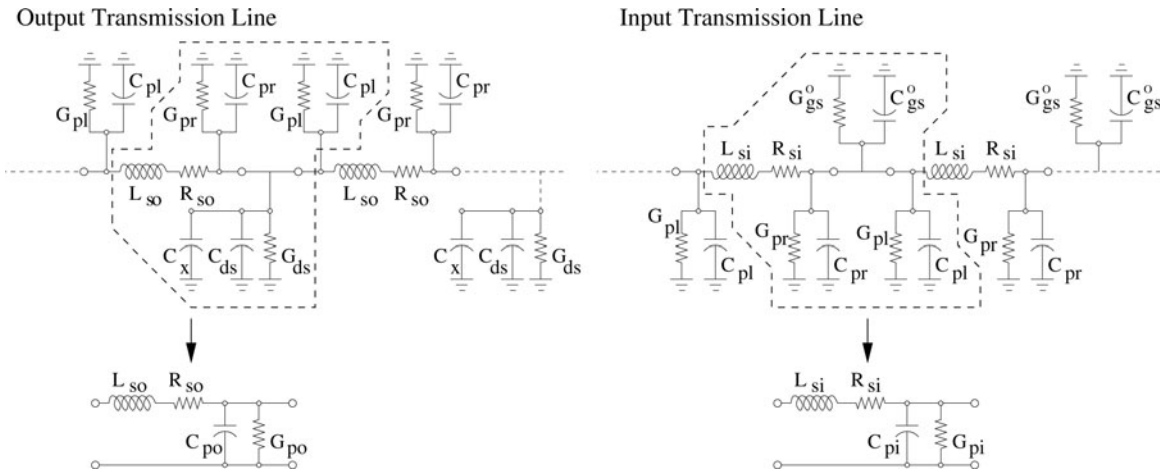

Fig. 3. Complete small signal model for the discrete transmission line components in the input and output line.

with non-ideal matching. By determining S_{11} and S_{22} from a Cadence simulation, the RF gain G can be weighted correspondingly by transforming the S_{11} and S_{22} values into the percentage of transmitted RF power and thereby reduced gain as shown in the following equations:

$$T_{S_{11}} = 1 - |S_{11}|^2, \quad T_{S_{22}} = 1 - |S_{22}|^2, \tag{13}$$

$$G_{weighted} = G T_{S_{11}} T_{S_{22}}, \tag{14}$$

$$G_{weighted,dB} = 10 \log_{10} (G_{weighted}) \,\text{dB}. \tag{15}$$

Another important aspect is how much RF power is lost into the DC supply path. Determining the complex impedances Z_{DC} and Z_L with Cadence, shown in Fig. 4, the RF power into the DC path and to the load can be calculated by

$$P_{TOT} = \text{Re}\left(\frac{1}{2} V_1 I_{TOT}^*\right) = \text{Re}\left(\frac{|V_1|^2}{2Z_{TOT}^*}\right), \qquad Z_{TOT} = Z_{DC} \| Z_L, \tag{16}$$

$$P_{DC,L} = \text{Re}\left(\frac{1}{2} V_1 I_{DC,L}^*\right) = \text{Re}\left(\frac{|V_1|^2}{2Z_{DC,L}^*}\right). \tag{17}$$

Figures 5 and 6 show the analyzed values for the damping factors α_g, α_d and phase constants β_g, β_d of the input and output transmission lines. The values shown were extracted for the cascode gain cell applying gate bias voltages V_{gs1} of 0.5 and 0.55 V, V_{gs2} of 2.0 V, and V_{dd} of 2.4 V as well as the extracted parasitic inductor components. For the inductors in the input and output line being almost of the same size, two things are worth noting. Both α_g and α_d increase significantly for high frequencies, as the capacitive coupling effect on the substrate gets more pronounced for higher frequencies. Although α_g exceeds α_d by 20% at 10 GHz, due to the stronger damping impact of G_{gs}^o versus G_{ds}, the strong damping of the output line shows how significant the no longer negligible impact of the parasitically loaded inductors is. The phase constants of both lines differ by 14% at 10 GHz, due to C_{pi} being larger than C_{po} but still small enough for constructive RF signal addition.

Figure 7 depicts simulated S_{11} and S_{22}, obtained with Cadence, and Fig. 8 depicts the simulated versus calculated RF gain. Shown are the analysis results with and without matching impact (12), (16) as well as the Cadence simulation. One can see the close resemblance and, additionally, the gain reduction due to the degrading port matching conditions for high frequencies.

Figure 9 displays the influence of a G_{gs}^o variation on S_{21} as well as the applied G_{gs}^o values, depicted as a resistance $1/G_{gs}^o$ for better legibility. It can be seen that G_{gs}^o barely influences the low-frequency gain, being very small. For high frequencies, however, G_{gs}^o has a visible impact, if the values are decreased from the original obtained component value for the cascode.

Figure 10 shows the influence on S_{21} if G_{pr} and G_{pl} are simultaneously swept for the input and output lines. A much

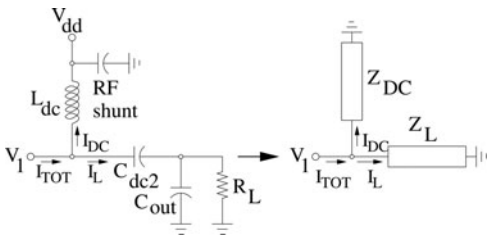

Fig. 4. Equivalent model for DC supply connection.

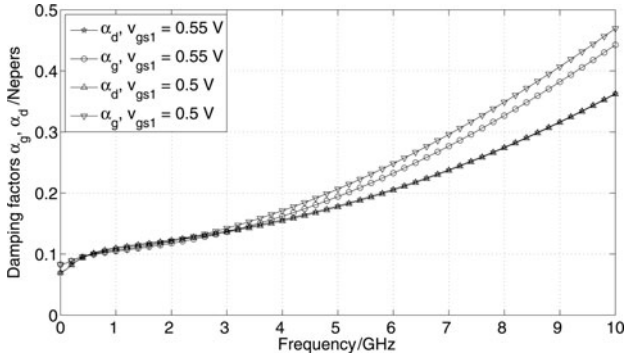

Fig. 5. Analyzed damping factors α_g and α_d.

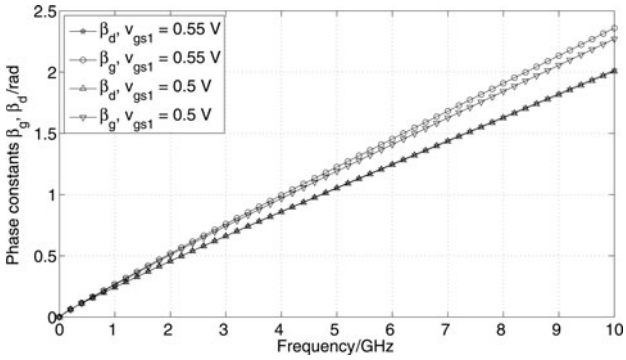

Fig. 6. Analyzed phase constants β_g and β_d.

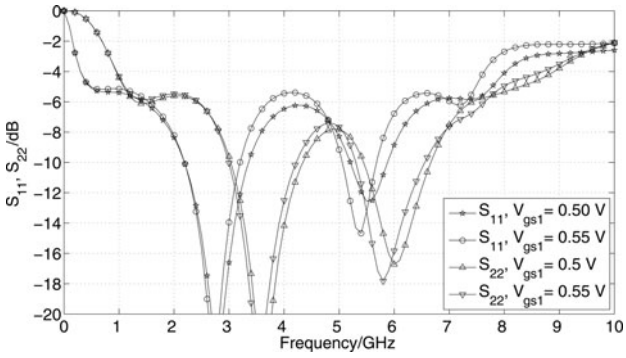

Fig. 7. Simulation port matching S_{11} and S_{22}.

more pronounced impact both for low and high frequencies can be seen when compared to the G^o_{gs} impact. G_{pl} and G_{pr} are both approximately of the same size, also for the input and output lines, and G_{pl}, shown in the lower subplot of Fig. 10, attains the same low resistance values as $1/G^o_{gs}$. Therefore, G_{pl} and G_{pr} influence the RF gain approximately four times as strongly as G^o_{gs}. This illustrates to which point the CMOS integrated inductor losses affect the TWA design.

The upper subplot of Fig. 11 displays the calculated RF power split into the DC supply path and towards the load according to (16) and (17) and the lower subplots display the corresponding resistances and reactances, obtained with Cadence. Most of the RF power is directed towards the load, as the self-resonance effect of the DC inductor acts as an RF block from around 4 GHz onward. From DC to 4 GHz, the

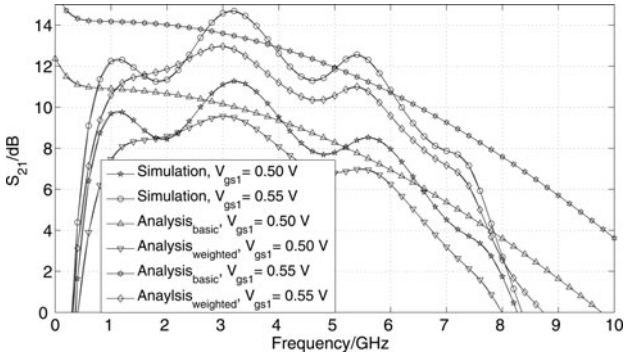

Fig. 8. Analysis and simulation S_{21}, $Analysis_{basic}$ obtained with (12), $Analysis_{weighted}$ obtained with (15).

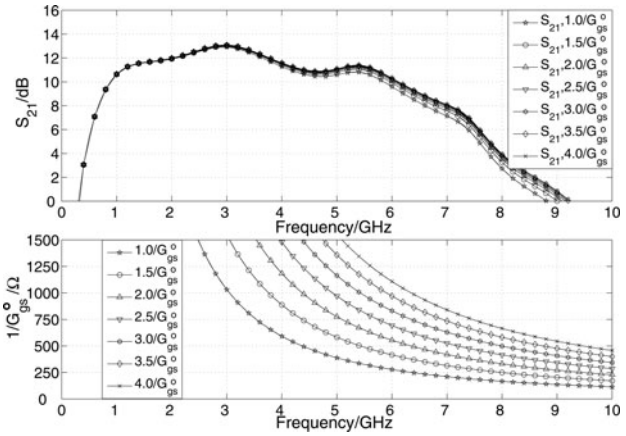

Fig. 9. Analysis of the G^o_{gs} influence on S_{21}, $V_{gs1} = 0.55$ V.

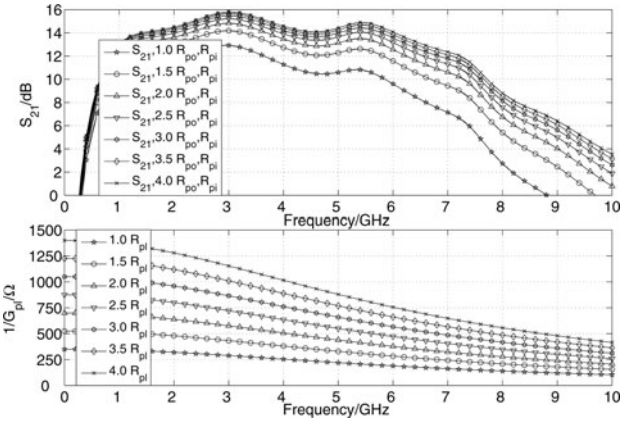

Fig. 10. Analysis G_{po} and G_{pi} influence on S_{21}, $V_{gs1} = 0.55$ V.

Z_{DC} resistance is small in comparison to the real part of Z_L, and insignificant RF and DC real power is lost.

Figure 12 illustrates the variation of S_{21} versus frequency if the number of stages is swept in (12). Depending on the frequency, different numbers of stages result in maximum S_{21}. At low frequencies, the substrate coupling has little influence and adding stages leads to higher amplification. For high frequencies, however, RF power is increasingly lost into the

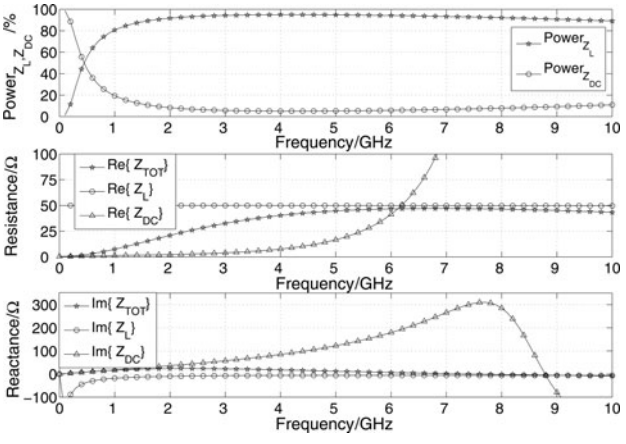

Fig. 11. Analysis of RF power split into DC supply and load.

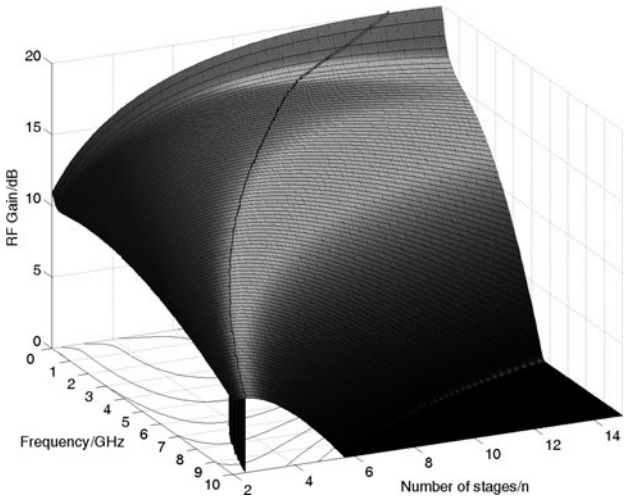

Fig. 12. Analysis S_{21} for differing number of stages, $V_{gs1} = 0.55$ V.

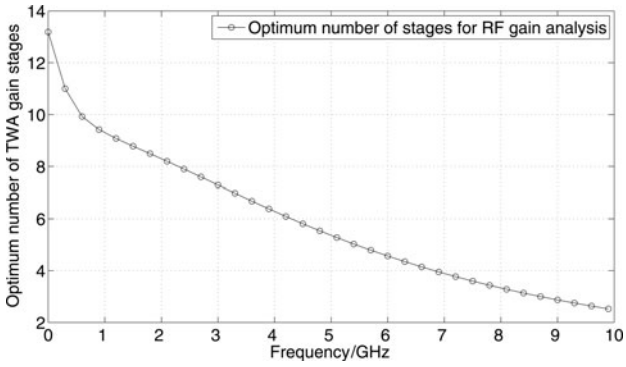

Fig. 13. Analyzed optimum number of TWA gain stages.

substrate. Based on the results shown in Fig. 12, Fig. 13 shows the optimum number of stages for maximum RF gain versus frequency. Up to 6.5 GHz, four stages or more provide maximum S_{21} values, whereas beyond that smaller numbers are advantageous. As a tradeoff for the highest gain over the whole frequency range from 1 to 8 GHz, four stages have been chosen, as the RF gain degrades rapidly for a larger number of stages from 6 GHz onwards.

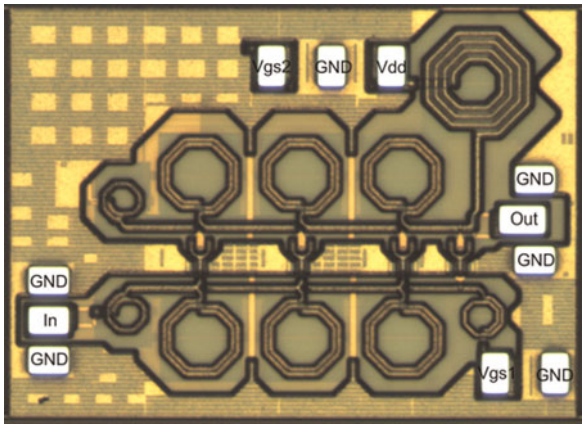

Fig. 14. Realized TWA layout, 1.45×1.0 mm².

The realized layout is illustrated in Fig. 14. The integrated series inductors are optimized for minimum parasitic loss by using pattern ground shields. They are arranged to alleviate mutual coupling and realize a ground plane that minimizes parasitic inductances towards the gain cells to avoid inductive source degeneration and thereby reduced RF gain.

III. RESULTS

An Anritsu 37000D NWA, an NRP Rhode & Schwarz Z-55 power meter, an Agilent 86100C Infiniium DCA oscilloscope, an Agilent 8257D signal generator, a SUESS PM8 probe station PM8, and GGB probes were used for measurements.

All simulations and measurements are obtained for V_{dd} of 2.4 V and a gate voltage V_{g2} of 2.0 V, equivalent to a gate source voltage V_{gs2} of 0.67 V. Figures 15 and 16 show simulated and measured S_{11} and S_{22}.

The matching pattern is maintained, although the matching peaks are slightly shifted to higher frequencies. Improved high-frequency matching is measured, which is the main reason for the improvement of the measured versus simulated RF gain at high frequencies, shown in Fig. 17.

For V_{gs1} of 0.5 V, S_{21} larger than 8 dB up to 7 GHz is measured. For V_{gs1} of 0.55 V, which results in higher g_m, measured S_{21} reaches values greater than 10 dB until 7 GHz. Figure 18 displays simulated and measured S_{12}. A certain discrepancy can be observed; however, the general trend holds and values below −30 dB are measured.

Figures 19 and 20 show the simulated and measured compression point P_{1dB} and the associated PAE for 2.4 and

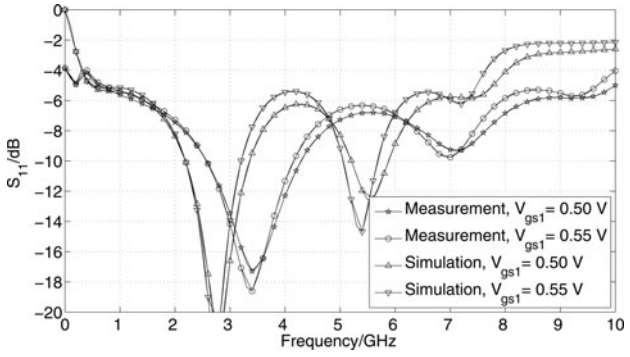

Fig. 15. Measured and simulated S_{11}.

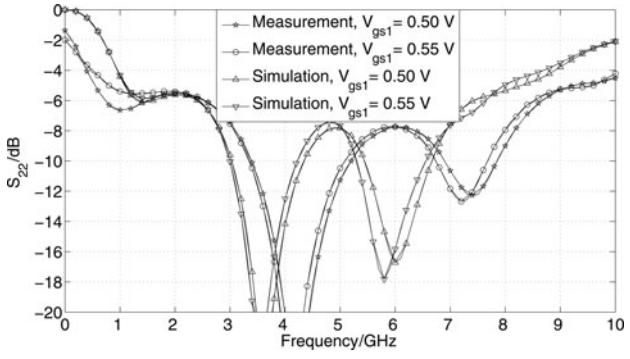

Fig. 16. Measured and simulated S_{22}.

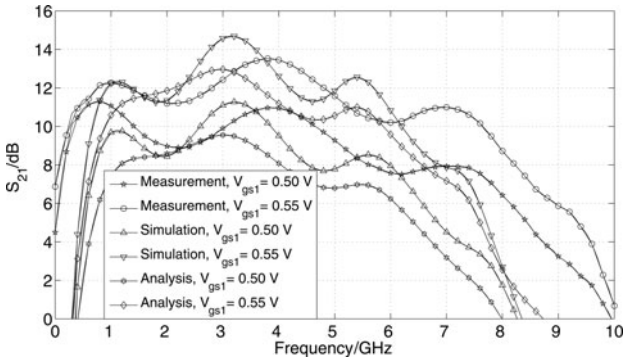

Fig. 17. Measured, simulated, and calculated S_{21}.

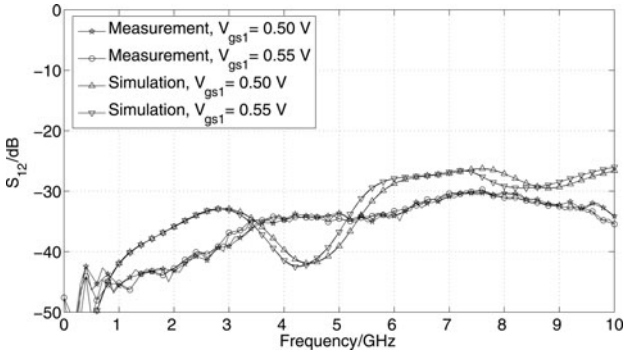

Fig. 18. Measured and simulated S_{12}.

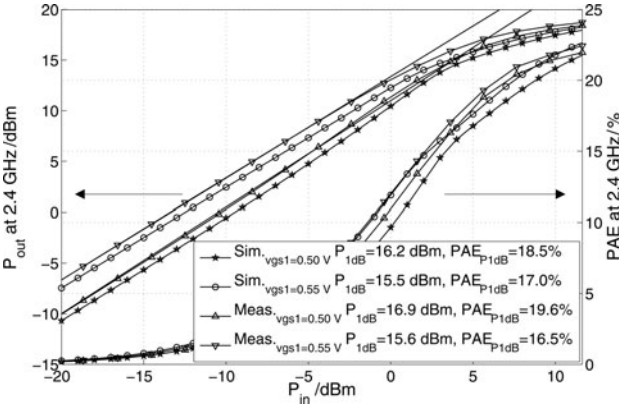

Fig. 19. Measured and simulated P_{1dB} and PAE at 2.4 GHz.

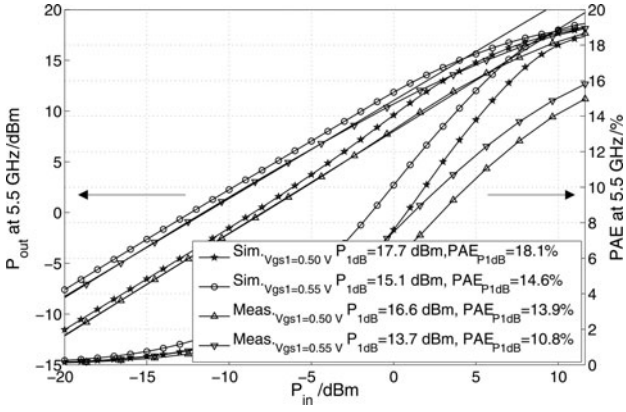

Fig. 20. Measured and simulated P_{1dB} and PAE at 5.5 GHz.

Table 1. Comparison with state-of-the-art.

Ref. Process	[5] 250 nm SiGe BiCMOS	[6] CMOS	[7] 90 nm CMOS	This work 180 nm CMOS	
Freqqency range/GHz	2–12	2–8	0–73.5	1–8	
S_{21}/dB	9	17	14	9 at 2.4 GHz	8 at 5.5 GHz
S_{11}/dB	<−15	–	<−9	<−6	
S_{22}/Db	<−10	<−5	<−9	<−6	
V_{dd}/V	5.0	2.0	1.2	2.4	
PAE/%	9	2.25	2.5	19.6 at 2.4 GHz	13.9 at 5.5 GHz
P_{1dB}/dBm	14	3.5	3.2	16.9 at 2.4 GHz	16.6 at 5.5 GHz
Chip area/ mm^2	1.16	–	1.15 × 1.5	1.45 × 1.0	

5.5 GHz. Highest P_{1dB} values and efficiencies are obtained for the lower gate bias voltage V_{gs1} of 0.5 V. At 2.4 GHz, a P_{1dB} of 16.9 dBm and a PAE of 19.6% are measured, while at 5.5 GHz, P_{1dB} equals 16.6 dBm and PAE attains 13.9%. The measurement results are in close accordance with the Cadence layout extraction simulations.

The two-tone test measurements resulted in OIP_3 values at 2.4 GHz of 24.1 and 24.0 dBm for a V_{gs1} of 0.5 and 0.55 V. At 5.5 GHz, the corresponding measured OIP_3 results amounted to 20.8 and 18.6 dBm.

IV. COMPARISON WITH STATE-OF-THE-ART

Comparing TWAs with each other is challenging, as they are optimized for differing bandwidths, S_{21}, P_{1dB}, efficiencies, and supply voltages, using different technologies such as GaAs, CMOS, BiCMOS, or SOI. The work of Sewiolo and Weigel [5] comes closest to the optimizations targeted here. It applies a four-stage bipolar common source tapered architecture to a V_{dd} of 5 V and achieves a gain of 9 dB up to frequencies of 12 GHz. However, a P_{1dB} of 14 dBm and a PAE of around 9% are obtained at the cost of high V_{dd}. The work of Grewing [6] can also be used for comparison. Although Grewing achieved a satisfying RF gain greater than 10 dB up to 7 GHz, the P_{1dB} of 3.5 dBm and the PAE of 2.25% he obtained are substantially less than the values attained here. To the knowledge of the author, the present work is the first to present a new methodology for assessing all the dominant loss contributions of integrated inductors in TWA designs. Furthermore, very competitive measurement results for a medium supply voltage of 2.4 V have been achieved, as can be seen from the obtained P_{1dB} and efficiency values (Table 1).

V. CONCLUSION

By expanding the present TWA theory with the calculation of the parasitic substrate losses in CMOS integrated inductors,

Table 2. Numerical result vectors from DC to 10 GHz containing the extracted component values.

FET	C^o_{gs}/pF	G^o_{gs}/mS	C_{ds}/pF	G_{ds}/mS	$\lvert g^o_m \rvert$/mS	R_{Bias}/kΩ	Transistor parameters	
$V_{gs1} = 0.50$ V	1.02–1.12	0–9.45	0.48–0.54	0.26	67–83	10.0	$w_g = 2\times305$ µm	
$V_{gs1} = 0.55$ V	0.99–1.05	0–8.75	0.5–0.54	0.4	107–122	10.0	$w_g = 2\times305$ µm	
Inductor	L_s/nH	$C_{ox,l}$/fF	$C_{ox,r}$/fF	$C_{si,r}$/fF	$C_{si,r}$/fF	$R_{si,l}$/Ω	$R_{si,r}$/Ω	R_s/Ω
L_i	1.22	195	190	65	65	350	350	1.2
L_o	1.2	195	185	70	65	350	350	1.0
C_{dc1}/pF	C_{dc2}/pF	C_{dc3}/pF	R_{t1}/Ω	R_{t2}/Ω	L_{DC}/nH	RF_{shunt}/pF	$C_{Bondpad}$/fF	C_x/pF
15	9	8	60	66	2.95	9	32	0.21

an enhanced RF gain prediction accuracy for integrated CMOS TWAs is achieved. Hence, an efficient circuit and inductor optimization is possible. The concept has been verified by a design example of a 1–8 GHz TWA for multistandard applications, realized in 180 nm CMOS technology that exhibits a lossy substrate. A comparison of the analysis, Cadence simulation, and measurement results shows very good agreement among them.

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APPENDIX

The resulting component values are displayed in Table 2.

Joerg Carls (S'07) was born in Bad Schwalbach, Germany, in 1979. He received his diploma degree in electrical engineering in 2005 from the Swiss Federal Institute of Technology, Zurich (ETHZ). After working in Strategic Consulting, he started as a Ph.D. student at the ETHZ in March 2006 and continued his research work at the Chair of Circuit Design and Network Theory at the Dresden University of Technology since September 2006. His main research interests lie in the field of highly efficient low-voltage power amplifiers in CMOS. He is developing the RF transmitter frontend in the framework of the European Union (EU)-funded project RESOLUTION.

Frank Ellinger (S'97-M'01-SM'06) was born in Friedrichshafen, Germany, in 1972. He graduated in electrical engineering (EE) from the University of Ulm, Germany, in 1996. He received MBA and Ph.D. degrees in EE from the ETH Zürich, Switzerland, in 2001, and habilitation degree in high-frequency circuit design from the ETH in 2004.

Since August 2006, he is full professor and head of the Chair for Circuit Design and Network Theory at the Dresden University of Technology. Mr. Ellinger is responsible for several projects funded by the EU. From 2001 to 2006, he has been head of the RFIC design group of the Electronics Laboratory at the ETH, and project leader of the IBM/ETH Competence Center for Advanced Silicon Electronics at IBM Research in Rüschlikon. He is mainly engaged in the design of high-speed analogue integrated circuits for wireless and optical communication.

In the time frame between 2005 and 2006, he served as an associated editor for the IEEE Micowave and Wireless Component Letters. He has published more than 100 refereed scientific papers, most of them IEEE journal contributions, and three patents. He authored the book "Radio Frequency Integrated Circuits and Technologies", which has been published in March 2007 by Springer. For his works he received several awards including the ETH Medal, the Denzler Award of the Swiss Federal Association of Electrical Engineers, the Rohde & Schwarz/Agilent/Gerotron EEEfCOM Innovation Award and a Young Ph.D. Award of the ETH Zürich.

Yulin Zhang was born in Shanghai, China, in 1977. He started his studies at the Dresden University of Technology, TUD, in 2003 and is currently working on his master's thesis at the Chair for Circuit Design and Network Theory, TUD. His main research interests lie in the field of high-frequency CMOS analog integrated circuit design.

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