DISS. ETH NO. 24181

Graphene three-terminal nanojunction rectifiers

A dissertation submitted to
ETH ZURICH

for the degree of
Doctor of Sciences

presented by

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2017

Abstract

In the present work, intrinsic voltage rectification in graphene three-terminal junctions (GTTJs) is investigated, with the goal to advance understanding of physical mechanisms behind this effect. In the first part, finite element simulations based on a field-effect transistor model are made to calculate output-voltage characteristics for realistic diffusive GTTJs. Within this model, rectification is described as an electrostatic effect. The simulations fit well to a substantial number of reported experimental results and provide engineering guidelines for rectification efficiency enhancement, such as good graphene material quality and high capacitive gate coupling. According to the simulations, efficiency in diffusive GTTJs is intrinsically limited to around 60%, as a consequence of the inability to pinch off conductivity in graphene. In the second part, etched GTTJs of different sub-micron constriction widths (down to 100 nm) are fabricated on Si/SiO_2 substrates and characterized electrically at 296 K and 87 K. Reproducibility of the rectification effect is demonstrated. Typical room-temperature rectification efficiencies are 10 to 20% at 100 mV input voltage, whereas efficiencies at 87 K are below 10%. The highest room-temperature rectification efficiency measured in our devices is $\sim 40\%$ (at 400 mV input voltage), which is higher than most efficiencies reported in the literature. Experiments show higher efficiencies at room temperature than at 87 K, in contrast to the predictions of the field-effect simulations. This indicates that mechanisms other than the field effect contribute to the rectification effect. We propose an explanation based on Joule-heating and thermal voltages, as the devices are operated in regimes of high power dissipation. This thermal model predicts thermal voltages which show bias-voltage, gate-voltage, and temperature dependences in conformance with measured output voltages. We conclude that Joule-heating effects need to be considered for GTTJ devices. At the same time, possibilities for alternative GTTJ functionality open up.

Zusammenfassung

In dieser Arbeit wird intrinsische Spannungsgleichrichtung in Graphen-basierten Drei-Terminal-Schaltungen (graphene three-terminal junctions, GTTJs) untersucht, mit dem Ziel das Verständnis der physikalischen Vorgänge hinter diesem Effekt voranzubringen. Im ersten Teil werden auf einem Feldeffekttransistor-Modell beruhende Finite-Elemente-Simulationen durchgeführt, um das Verhalten der Ausgangsspannung für realistische diffusive GTTJs zu berechnen. Innerhalb dieses Modells wird die Gleichrichtung durch elektrostatische Effekte erklärt. Die Simulationen stimmen mit einer erheblichen Anzahl publizierter experimenteller Ergebnisse überein, und liefern technische Richtlinien zur Steigerung der Gleichrichtungs-Effizienz, wie zum Beispiel gute Graphen Materialqualität oder grosse kapazitive Gate-Kopplung. Den Simulationen zufolge ist die Effizienz in diffusiven GTTJs intrinsisch auf etwa 60% beschränkt, als Folge davon, dass man die Leitfähigkeit in Graphen nicht unterdrücken kann. Im zweiten Teil werden geätzte GTTJs verschiedener sub-mikrometer-grossen Verengungsbreiten (bis hin zu 100 nm) auf Si/SiO_2 Substraten hergestellt, und bei Temperaturen von 296 K und 87 K elektrisch untersucht. Die Reproduzierbarkeit des Gleichrichtungseffekts wird gezeigt. Übliche Gleichrichtungs-Effizienzen bei Raumtemperatur sind 10 bis 20% bei 100 mV Eingangsspannung, wohingegen Effizienzen bei 87 K unter 10% liegen. Die höchste Gleichrichtungs-Effizienzen, die bei Raumtemperatur in unseren Bauelementen gemessen wurde, ist $\sim 40\%$ (bei 400 mV Eingangsspannung), was höher als die meisten in der Literatur berichteten Effizienzen ist. Die Experimente zeigen höhere Effizienz bei Raumtemperatur als bei 87 K, im Gegensatz zu den Vorhersagen der Feldeffektsimulationen. Dies weist auf nicht auf den Feldeffekt beruhende zur Gleichrichtung beitragende Mechanismen hin. Wir schlagen eine auf Joule-Wärme und thermischen Spannungen basierende Erklärung vor, da die Bauteile in Bereichen hoher Verlustleistung gemessen werden. Dieses thermische Modell sagt thermische Spannungen voraus, welche Abhängigkeiten von Vorspannung, Gate-Spannung und Temperatur zeigen, die mit denen der gemessenen Ausgangsspannungen übereinstimmen. Wir schlussfolgern daraus, dass Auswirkungen von Joule-Wärme für GTTJ-Bauteile berücksichtigt werden müssen. Gleichzeitig eröffnen sich Möglichkeiten für alternative Anwendungen von GTTJs.

Contents

Symbols and abbreviations

Physical constants	
e	Fundamental charge ($e > 0$)
ϵ_0	Vacuum permittivity
$h = 2\pi\hbar$	Planck constant
k_B	Boltzmann constant

Symbols	
C	Capacitance per unit area
E, E_F	Energy, Fermi energy
ϵ	Relative permittivity
η_F	Normalized Fermi energy
$\mathcal{F}_1$	Complete Fermi-Dirac integral of index 1
G	Electrical conductance
I	Electric current
L	Length
μ	Charge carrier mobility, also electro-chemical potential
ν_F	Fermi velocity
n	Electron density, also charge carrier density
p	Hole density
P	Electric power
S	Seebeck coefficient (also called thermopower)
σ	Electrical conductivity
T	Temperature
V	Voltage
W	Width

Abbreviations	
2D	Two-dimensional
2DEG	Two-dimensional electron gas
AFM	Atomic force microscopy
CVD	Chemical vapor deposition
EBL	Electron-beam lithography
FEM	Finite element method
FET	Field-effect transistor
GTTJ	Graphene three-terminal junction
hBN	Hexagonal boron nitride
HMDS	Hexamethyldisilazane
IPA	Isopropanol
LN_2	Liquid nitrogen
MIBK	Methyl-isobutyl-ketone
PEI	Polyethylenimine
PMMA	Poly(methyl methacrylate)
RIE	Reactive-ion etching
SMU	Source measurement unit
TTJ	Three-terminal junction

Chapter 1

Introduction

Novel nanosized electronic devices

Microelectronics has a safe place among revolutionary technologies that have made a big impact on people's lives. Progress in this field has helped develop computing, communication, as well as entertainment and security technology. Performance increase has relied mainly on down-scaling transistor size, such that field-effect transistors (FETs) in modern computer chips have gate lengths approaching 10 nanometers [1]. However, since this down-scaling approach is increasingly challenging and has physical limitations, the semiconductor industry has been looking for alternative ways to increase performance. One strategy is to replace silicon by high-mobility materials such as (Si)Ge and III–V compound semiconductors material combinations. Also three-dimensional device architectures are investigated. Another strategy is to explore novel device concepts such as tunnel FETs [1].

In the same line, ballistic transport effects have been used for novel device functionality [2–4]. One of the most-studied ballistic nanoelectronic devices is the three-terminal junction (TTJ), also known as Y-branch switch or junction, based on two-dimensional electron gases (2DEGs) in semiconductor heterostructures [5–9]. Its key property is an intrinsic voltage-rectification effect [10]. A growing number of compact nanoscale electronic devices relying on this rectification effect have been realized, including logic gates [4], frequency multipliers [11], mixers [12], and phase detectors [12]. From a technological viewpoint, integration of TTJs into future chip design is in principle possible. TTJ-based nanoelectronic devices with functionality at room temperature are thus promising for future commercial applications.

Graphene as material of choice

With the discovery of graphene in late 2004 [13], a new class of two-dimensional materials [14–17] came on the radar of the scientific and engineering community. Interest arose to investigate fundamental properties (e.g. anomalous quantum Hall effect, Klein paradox in graphene [18, 19]), but also opportunities for device applications were perceived [20]. Due to its high charge carrier mobility graphene is for example attractive as conductive channel of high-frequency transistors [21, 22]. Room-temperature ballistic transport was demonstrated in µm-sized graphene encapsulated between hexagonal boron nitride (hBN) [23]. Such ultra-high mobilities make graphene an interesting material for building TTJs. Additionally, graphene features tunability from n-type to p-type transport, which is not possible in conventional semiconductor heterostructures and thus leads to richer device functionality.

Voltage rectification in graphene-based three-terminal junctions (GTTJs) was demonstrated by Jacobsen *et al.* [24], leading to more reports on the topic [25–34], where the rectification effect was measured in devices made of different graphene types [exfoliated graphene on SiO_2 with and without chemical passivation, graphene grown on silicon carbide (SiC) and by chemical vapor deposition (CVD)]. While the rectification functionality of GTTJs is robust, the statistical variation of the efficiencies between different devices is large. There is still a lack in understanding at a fundamental level the mechanisms causing rectification and the efficiency limitations. This project aims to advance this understanding and to open up possibilities for device engineering and application implementation.

Structure of the thesis

After a short introductory part, background on the research field of three-terminal nanojunction rectifiers is provided, followed by a description of graphene's electronic properties and attractiveness as building block of such nanoelectronic devices (chapter 2). Open questions are addressed and the project goals are defined. Next, finite element simulations are presented (chapter 3) which helped to understand the influence of important parameters such as temperature, geometry, and extrinsic disorder on GTTJ rectification functionality. Ensuing chapters contain the experimental part of the thesis. First, sample fabrication techniques and measurement schemes for electrical characterization are presented (chapter 4). Then experimental results are discussed, considering in particular thermoelectric effects due to self-heating (chapter 5). Experimental raw data of samples of different geometries can be found in appendix A. The manuscript ends with conclusions and outlook (chapter 6).

Chapter 2

Background on the rectification effect in GTTJs

The purpose of this chapter is providing background information on the voltage-rectification effect in GTTJs. First, rectifying properties of 2DEG-based ballistic TTJs are presented. Next, electronic properties of graphene are reviewed. Finally, rectifying properties of GTTJs are presented in a literature overview. The chapter ends with open questions in this research field and the problem definition for this thesis.

2.1 Voltage rectification in ballistic TTJs

Electronic rectifiers are devices converting alternating current to direct current. A diode is an example of a conventional rectifier, relying on the non-linear electrical properties of semiconductor p-n junctions or Schottky barriers. Ballistic rectifiers depart from this paradigm [3, 4]. Their operation principle is based on ballistic electron transport, possible in high-mobility materials with electron mean free paths lager than the device size. The electrons are predominantly scattered by designed geometrical boundaries and not from defects, leading to nonlinear rectifying device functionality. Because of this working principle, very high operation speed can be achieved. Furthermore, these ballistic devices have no intrinsic threshold voltage which must be overcome in conventional diodes to start rectification functionality.

The first experimental demonstration of a ballistic rectifier was carried out by Song and coworkers [35] in a GaAs/AlGaAs 2DEG (figure 2.1). The device consisted of a four-terminal ballistic microjunction with a triangular scatterer in the center. Electrons flowing between the terminals denoted S (source) and D (drain) were deflected by geometric design to terminal L. This led to negative charge accumulation in this terminal, hence to voltage build-up between terminals L and U. This voltage was independent of current direction, which defines the voltage-rectification effect discussed here. Device functionality is similar to that of a bridge rectifier (depicted in the right inset of figure 2.1). The ballistic rectifier is a compact threshold-free alternative to this diode set-up.

In the following years, a simplified three-terminal version of aforementioned device (omitting terminal U) was extensively studied in both experiments and theory [5–10,36]. Typical electrical properties are shown in figure 2.2. The device (shown as inset) was a ballistic T-shaped TTJ with constriction widths below 100 nm, made from an GaInAs/InP heterostructure. A common measurement configuration is shown as inset in figure 2.2: two

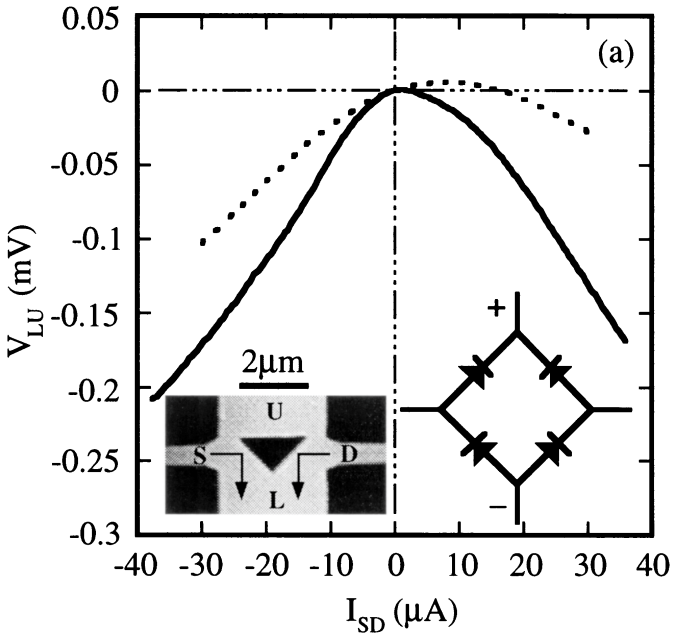

Figure 2.1: Reprinted with permission from [35] Copyright 2017 by the American Physical Society. Electrical properties of a ballistic four-terminal junction rectifier. Left inset: atomic force micrograph of the device. Arrows represent trajectories of electrons and show that the geometry breaks the symmetry of the current path. The voltage between terminals L and U (V_{LU}) showed nonlinear dependence on the current flowing from terminal S to D (I_{SD}). Measurements were done at 77 K (dashed line) and 4.2 K (solid line). Right inset: diode bridge rectifier.

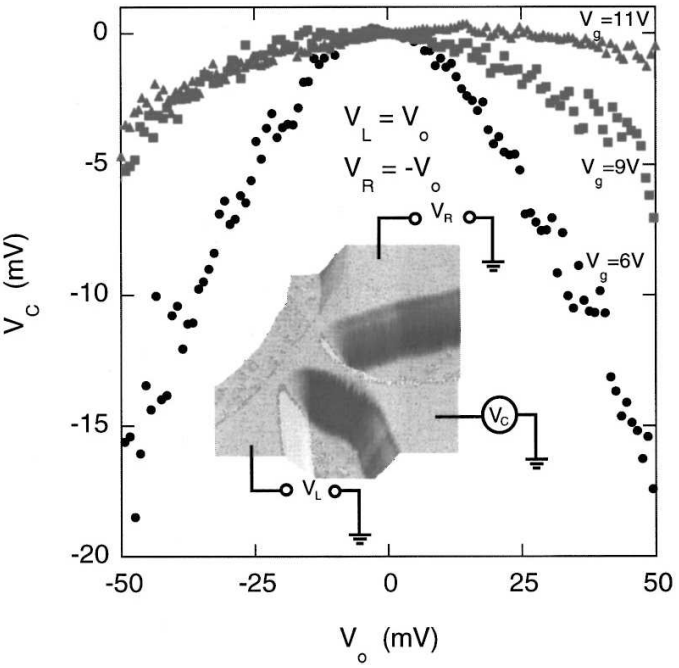

Figure 2.2: Reprinted from [5], with the permission of AIP Publishing. Electrical properties of a ballistic three-terminal junction rectifier at 200 K. Inset: three-dimensional atomic force micrograph of the device with the measurement configuration. A push-pull bias V_0 and $-V_0$ was applied to the left and right terminals, and V_c was measured at the central terminal. V_c showed a parabolic dependence on V_0. The curvature was always negative and could be tuned by a top-gate voltage V_g.

terminals were biased in so-called push-pull configuration with V_0 and $-V_0$ applied to the left and right terminals. The voltage V_c on the remaining floating terminal was probed. For a diffusive symmetric device measured in such configuration $V_c = 0$ is expected for all V_0. Any deviation of V_c from zero indicates non-diffusive behavior. The measurement configuration was specifically chosen for easy observation of such behavior. V_c showed parabolic dependence on V_0 with negative curvature. This curvature showed gate-voltage tunability, and thus dependence on Fermi energy. Rectification was shown to be robust up to room temperature.

TTJ rectifiers with device operation at room temperature were realized in different material systems, demonstrating the robustness of the rectification effect. Most reported devices were fabricated from 2DEGs in semiconductor heterostructures, as for example in InP/InGaAs [36], GaAs/AlGaAs [6], InAlAs/InGaAs [37], InAs/AlGaSb [38], Si/SiGe [39] AlGaN/GaN [40]. Also silicon devices were investigated [41]. Rectifying and switching properties were also observed in three-branched InAs nanowires [42] and in three-branched carbon nanotubes [43–45]. Furthermore, rectification functionality at ultra-high frequencies was demonstrated at room temperature [37,46–48], up to almost 100 GHz [49,50]. Frequency doubling was reported up to the GHz range [50,51]. Electrical response was demonstrated up to 500 GHz by picosecond electrical pulse excitation [52]. Monte-Carlo simulations predicted functionality of the ballistic devices in the THz frequency range [50,53,54]. An impressive number of room-temperature applications for ballistic junctions has been realized building upon the rectification effect, including triodes [7], frequency multipliers [11,50], radio-frequency mixers and phase detectors [12,50], logic AND [55], NAND [7], and NOR [56] gates, set-reset latches [57], and half adders [58]. Tunability of TTJs was also achieved with Schottky wrap gates on the branch regions [59], allowing realization of logic gates [60] and flip-flop devices [61]. Moreover, rectification with both negative and positive output voltages was demonstrated in TTJs [40].

Propositions to explain the nonlinear electrical properties of TTJs and multiple-terminal junctions have mainly been based on ballistic effects. In the simple billiard ball picture [3] electron transport is governed by momentum guiding defined by device geometry. The argument goes that the mean free path of charge carriers is comparable to the junction constriction size and that the carriers pass through the branches by scattering elastically at the boundaries (see inset of figure 2.1). This way the carriers roughly keep their initial energy and the voltage measured in the central terminal is comparable to the voltage of the terminal from which the carriers enter. In a different description of ballistic transport, emphasizing wave nature of electrons, current flow through the constriction is treated as a quantum transport phenomenon (in analogy to photons in an optical waveguide). This can be done when the de-Broglie wavelength at the Fermi energy (Fermi wavelength) of the electrons is roughly equal to the constriction size. The conductance is given by the transmission probability of the electrons from one constriction end to the other (Landauer-Büttiker formalism). For a symmetric ballistic TTJ under assumption of reflection-less electron transport, the following relation holds for small V_0 (eV_0 small compared to the Fermi energy E_F) [10]:

$$V_c \approx -\frac{e}{2}\frac{G_c'(E)}{G_c(E)}\bigg|_{E=E_F} V_0^2 \leq 0, \tag{2.1}$$

where V_0 and V_c are defined as in figure 2.2, e is the fundamental charge, G_c the conductance of the central constriction, and E denotes energy. Theorists showed furthermore that the rectification effect remains robust at higher biases and temperatures [62].

For diffusive rectification devices, bias-induced enhancement of electron mean free path was considered [8]. Other effects proposed as cause for rectification and switching effects in semiconductor TTJs are intervalley electron-transfer process caused by hot electrons in a high electric field [50,63], surface charges [53,64,65], self-gating and capacitive coupling between branches [66,67], and hot-electron thermopower effects [39,68].

2.2 Graphene

Graphene is a 2D crystal of carbon atoms, arranged in an hexagonal lattice [figure 2.3(a)]. Remarkably, it was described theoretically in 1947 [69] but was not discovered experimentally until 2004 [13], produced in a surprisingly simple way by mechanically peeling off layers of graphite. It sparked a huge ongoing scientific interest since [20, 70, 71].

Among graphene's many excellent properties we give as examples its ultra-high room-temperature charge carrier mobility (theoretical limit 200,000 $\mathrm{cm}^2/\mathrm{Vs}$ [72]), high thermal conductivity (3000 $\mathrm{WK}^{-1}\mathrm{m}^{-1}$ [73]), wavelength-independent optical transparency (absorption $\approx 2.3\%$ for normal incident light below 3 eV [74]), and impermeability to standard gases including helium [75]. These properties and others motivated intensive research into technological applications [20, 71] of this fascinating material, ranging from flexible electronics, photodetectors, supercapacitors, to gas sensors. Of particular interest are the electronic properties of graphene. Much progress has been achieved in the fabrication of graphene-based high-frequency FETs, demonstrating cutoff frequencies of above 400 GHz [22]. Graphene is thus promising for THz electronics. Ultra-high room-temperature mobilities of up to 140,000 $\mathrm{cm}^2/\mathrm{Vs}$ were demonstrated for edge-contacted graphene encapsulated between hBN [76]; clearly outperforming state-of-the-art III–V high electron mobility transistors (HEMTs) with high-end mobilities of up to 77,000 $\mathrm{cm}^2/\mathrm{Vs}$ (InSb) [17]. In addition, graphene shows ultra-high current carrying capability. Current densities higher than 10^8 $\mathrm{A/cm}^2$ (assuming a thickness of 0.35 nm) were measured [77–79], which is equivalent to a few mA per µm channel width. In principle, graphene is CMOS compatible and hybrid graphene-silicon circuits are possible developments for future electronics [80]. Aforementioned properties thus make graphene an interesting candidate for electronic device applications.

We are interested in the electronic properties of graphene and its exploitation for rectifying devices. Below, main electronic properties of graphene are summarized.

Electronic properties

The graphene lattice is formed by in-plane σ-bonds and overlapping p_z-orbitals forming π-bonds. In the tight-binding approximation [69, 81], considering only contributions of nearest neighbor atoms, the following dispersion relation is obtained:

$$E(\mathbf{k}) = \pm\gamma\sqrt{1 + 4\cos^2\left(\frac{k_x a}{2}\right) + 4\cos\left(\frac{k_x a}{2}\right)\cos\left(\frac{\sqrt{3}k_y a}{2}\right)}, \tag{2.2}$$

where E gives allowed energy bands, $\mathbf{k} = (k_x, k_y)$ is the wave vector, γ the nearest-neighbor hopping integral, and a is defined in the caption of figure 2.3(a). The band structure is shown in figure 2.3(c). $E = 0$ corresponds to the Fermi level for pristine undoped graphene. The energy spectrum is symmetric with respect to this plane, reflecting

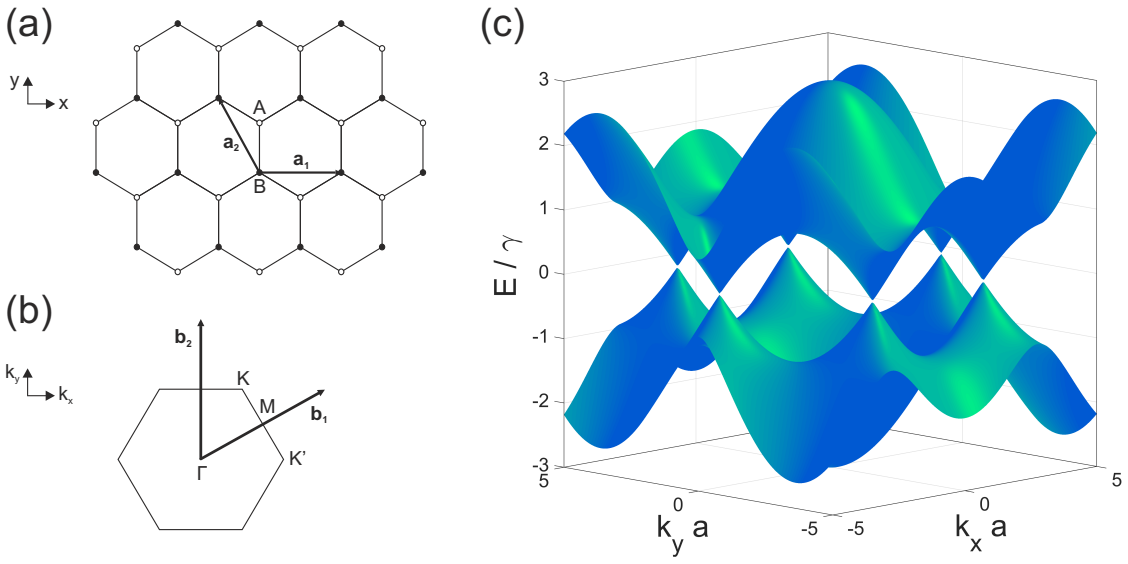

Figure 2.3: (a) Graphene crystal structure, formed by carbon atoms arranged in a planar honeycomb lattice. $\mathbf{a}_1$ and $\mathbf{a}_2$ are the lattice vectors of magnitude $a = 0.246$ nm. The unit cell consists of two carbon atoms, denoted A and B. (b) First Brillouin zone with reciprocal lattice vectors $\mathbf{b}_1$ and $\mathbf{b}_2$. Γ, M, K, and K' are symmetry points. (c) Band structure of graphene calculated within tight-binding approximation [equation (2.2)]. The lower (π-band) and upper bands (π^*-band) touch at the K and K' points (Dirac point). The Fermi energy of pristine undoped graphene corresponds to the plane defined by those points. At low energies the dispersion relation is linear. Graphene is a gap-less semiconductor.

electron-hole symmetry in the material. The valence and conduction bands (also called π- and π^*-bands here) have zero energy gap. Expanding E in (2.2) for small wave vectors around the K (or K') point yields the following linear approximation:

$$E(\mathbf{q}) = \pm\hbar\nu_F\,|\mathbf{q}|\,,$$

where $\mathbf{q} = \mathbf{k} - \mathbf{K}$, $|\mathbf{q}| \ll |\mathbf{K}|$, and $\nu_F \approx 1 \cdot 10^6$ m/s the momentum-independent Fermi velocity [82,83]. Near the Dirac point charge carriers mimic relativistic massless particles (Dirac particles). This is a remarkable property, responsible for the interesting electronic properties of graphene. The density of states D is given by:

$$D(E) = \frac{2}{\pi\left(\hbar\nu_F\right)^2}\,|E|\,,$$

taking into account twofold spin and twofold valley degeneracies (K and K' points). Again, a linear relationship is found. Graphene has zero density of states at the Dirac point. At zero temperature, electron density n as function of Fermi energy E_F (defined for $E_F > 0$) is given by

$$n = \int_0^{E_F} D(E)dE = \frac{E_F^2}{\pi\left(\hbar\nu_F\right)^2}. \tag{2.3}$$

The expression for the hole density is the same (defined for $E_F < 0$).

Electronic transport in diffusive conductors (i.e. sample size larger than mean free path of charge carriers) is generally treated in the Drude picture [81]. When a bias voltage (electric

field **E**) is applied to the conductor, charge carriers undergo random scattering events but move on average with constant drift velocity. The proportionality between drift velocity and applied electric field is called charge carrier mobility μ. The current density **J** is a linear response to the electric field: $\mathbf{J} = \sigma\mathbf{E}$ (Ohm's law), where σ is electrical conductivity. σ is given by:

$$\sigma = e\mu n, \tag{2.4}$$

where e is the fundamental charge and n the charge carrier density. The mean free path l can be calculated with the relation [84] $\sigma = e\mu n = \frac{2e^2}{h} k_F l$, where h is the Planck constant and k_F the Fermi wave vector. With $k_F = \sqrt{\pi n}$ we get:

$$l = \frac{\hbar}{e}\mu\sqrt{\pi n}. \tag{2.5}$$

For $\mu = 10^4$ cm^2/Vs, $l \approx 120$ nm at a carrier density $n = 10^{12}$ cm^{-2}.

Electric field effect

Investigating electronic properties of conducting materials requires tuning of charge carrier density. This tuning is achieved either by applying a bias voltage to the conductor or by creating an external electric field. The latter is created by applying a so-called gate voltage to an electrode separated from the studied conductor by a dielectric layer. The process of a gate voltage inducing charges in the conductor is called field effect. Our graphene nanostructures lied on a silicon substrate with a 285 nm thick SiO_2 layer on top. The capacitor formed by the silicon, the SiO_2 layer, and the graphene was approximated as a parallel-plate capacitor; a common simplification. The induced charge carrier density n is then given by:

$$n = \frac{\epsilon\epsilon_0}{ed}\left(V_G - V_{Dirac}\right), \tag{2.6}$$

where ϵ and d are dielectric constant and thickness of the SiO_2 layer, ϵ_0 the vacuum permittivity, V_G the gate voltage, and V_{Dirac} the gate voltage corresponding to the Dirac point (also called charge-neutrality point). V_{Dirac} is the gate voltage at which the conductivity is minimized. For pristine graphene $V_{Dirac} = 0$. Adsorbed chemical species dope graphene and cause $V_{Dirac} \neq 0$. $n > 0$ in (2.6) represents the electron density and $n < 0$ the hole density (hole density $p \equiv -n$). In our case $\epsilon\epsilon_0/(ed) = 7.6 \cdot 10^{10}$ cm^{-2}/V.

Figure 2.4 shows graphene conductivity determined experimentally. The V-shaped dependence of conductivity on carrier density is characteristic for graphene. The Dirac point was at $V_G \approx 6$ V here, indicating p-doping of the graphene sheet. This doping was presumably due to chemical residues from device fabrication. Carrier mobilities at $n = \pm 10^{12}$ cm^{-2} were calculated from equations (2.4) and (2.6) to be around 2000 and 1000 cm^2/Vs for holes and electrons, respectively.

At the Dirac point, conductivity of graphene is finite despite zero density of states. Typically, a residual conductivity of $\approx 4e^2/h \approx 0.15$ mS is measured for graphene on SiO_2. The quantity $e^2/h \approx 1/(26\ \text{k}\Omega)$ is called the conductance quantum [81]. Residual charges from potential disorder (electron-hole puddles) [85–87] and thermally excited charges [83,88–90] contribute to the residual conductivity. The electron-hole puddles are believed to arise from long-range Coulomb scattering of defects in the substrate and from charged impurities.

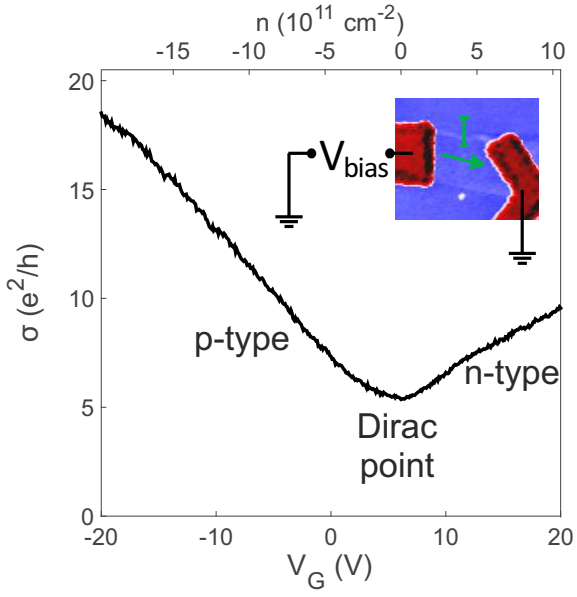

Figure 2.4: Graphene conductivity σ as function of gate voltage V_G and induced charge carrier density n (room-temperature measurement). σ is normalized to the conductance quantum e^2/h. The inset shows the measured device: a graphene sheet in the center ($\approx$ 1 µm x 1µm) and metal contacts (in red) to the left and right. The graphene sheet lied on top of a SiO_2 layer on a silicon substrate. A gate voltage V_G was applied to the silicon. The graphene sheet was biased by $V_{bias} = 1$ mV, driving an electric current I. n was calculated with (2.6) under parallel-plate capacitor approximation. $n > 0$ corresponds to electron (n-type) transport and $n < 0$ to hole (p-type) transport.

2.3 Graphene-based TTJs

The research community working on TTJs has shown high technological and scientific interest in graphene TTJs. Because of its two-dimensionality, graphene is a logical replacement for 2DEGs. In general, graphene devices are easier and cheaper to produce than 2DEG devices. High charge carrier mobility of graphene up to room temperature is promising for device operation at ultra-high frequencies. Tuning ability to both n-type and p-type transport gives additional rectification functionality and opens up possibilities for adaptive electronic devices [91]. Moreover, high current carrying capability allows large operation ranges. From a scientific viewpoint, the physical mechanisms behind the rectification effect are not clarified yet. A major drawback of using graphene for TTJs is the inability to pinch off conductivity in graphene[1]. In 2DEG-based TTJs, pinching off one TTJ branch led to enhanced rectification [5], and also perfect rectification was reported [6,57,95].

Rectification functionality

The following electrical property of GTTJs is referred to as voltage-rectification functionality: under a push-pull bias $\pm V_{in}$ on the left and right terminals of the device [figure 2.5(a)], the voltage on the central terminal (output voltage V_{out}) is negative when operating in the electron regime (negative rectification), positive when operating in the hole regime (positive rectification), and zero at the Dirac point (no rectification). These dependencies remain unchanged for opposite sign of V_{in}. The type of rectification functionality

[1] In the quantum transport regime, however, this is possible in graphene nanoconstrictions [92–94].

can be adjusted by gate-voltage (Fermi-energy) tuning.

Below we present an explanation for the rectification functionality [24], following an argument by Xu for rectification in ballistic TTJs [10]. Generally, a current I flowing between two terminals, say L and R, can be modeled as $I = -\int_{V_L}^{V_R} G dV = (1/e)\int_{\mu_L}^{\mu_R} G(E)dE$, where G is the conductance of the constriction between those terminals, V the voltage, and E the energy. The (electro-)chemical potential of each terminal is given by $\mu_i = E_F - eV_i$ $(i = L, R, C)$, where E_F is the Fermi energy, e the fundamental charge, and V_i the voltage at terminal i. Because the central terminal is floating, no current flows into this terminal. In other words: the current flowing into and out of this terminal cancels out. Assuming a fully symmetric device (all constrictions have identical conductances), one obtains:

$$\int_{\mu_L}^{\mu_C} G(E)dE = \int_{\mu_C}^{\mu_R} G(E)dE. \tag{2.7}$$

The chemical potential in the central terminal adjusts to fulfill this condition. In the zero temperature approximation, using equations (2.3) and (2.4), a parabolic relationship between conductance and energy can be assumed: $G(E) = a \cdot E^2 + b$ with positive constants a and b [figure 2.5(b)]. The current balance (2.7) is represented graphically with the areas of different colors and shadings below the conductance curve. Two electrical configurations are presented on the same curve; one for each type of charge carrier transport. In both cases, μ_C deviates from E_F to fulfill (2.7). V_{out} is given by $(E_F - \mu_C)/e$ and is thus always positive for p-type transport, always negative for n-type transport, and zero at the Dirac point. Note that this is also true for the opposite push-pull configuration. The rectification effect is therefore symmetric with respect to the sign of the input voltage V_{in}.

Solving equation (2.7) for small V_{in} ($|V_{in}| \ll |E_F|/e$) gives

$$V_{out} \approx -e\frac{aE_F}{aE_F^2 + b}V_{in}^2 \equiv -\frac{e}{2}\frac{G'(E)}{G(E)}\bigg|_{E=E_F} V_{in}^2. \tag{2.8}$$

Hence, an approximately parabolic $V_{out}(V_{in})$ dependence is expected [figure 2.5(d)], as for ballistic TTJs [equation (2.1)]. The curvature of this relationship is determined by the sign of E_F. $|V_{out}|$ has two maximum values around $E_F = 0$ and decreases at higher $|E_F|$ [figure 2.5(c)]. Plugging in $a = e\mu/\left(\pi\hbar^2\nu_F^2\right)$ and $b = 4e^2/h$ with μ=10,000 cm^2/Vs, we get $V_{out} = 2$ mV for $V_{in} = 10$ mV at $E_F = 50$ meV.

As figure of merit of GTTJs, or *efficiency*, for a given V_{in} we propose the absolute value of the maximum output voltage over all gate-voltage values, divided by V_{in}:

$$\text{Efficiency} = \text{maximum}\left|V_{out}/V_{in}\right|.$$

The efficiency generally varies with V_{in}. However, in the case of parabolic $V_{out}(V_{in})$ dependence the (maximum) curvature $|\alpha| = |V_{out}/V_{in}^2|$ is best suited as figure of merit because it is independent of V_{in}.

Literature overview

Experimentally, the electrical rectification effect in GTTJs was demonstrated for the first time in 2010 in ref. 24. The authors found that output voltage increases with input voltage, roughly in a parabolic relationship as observed in 2DEG-based TTJs. Furthermore,

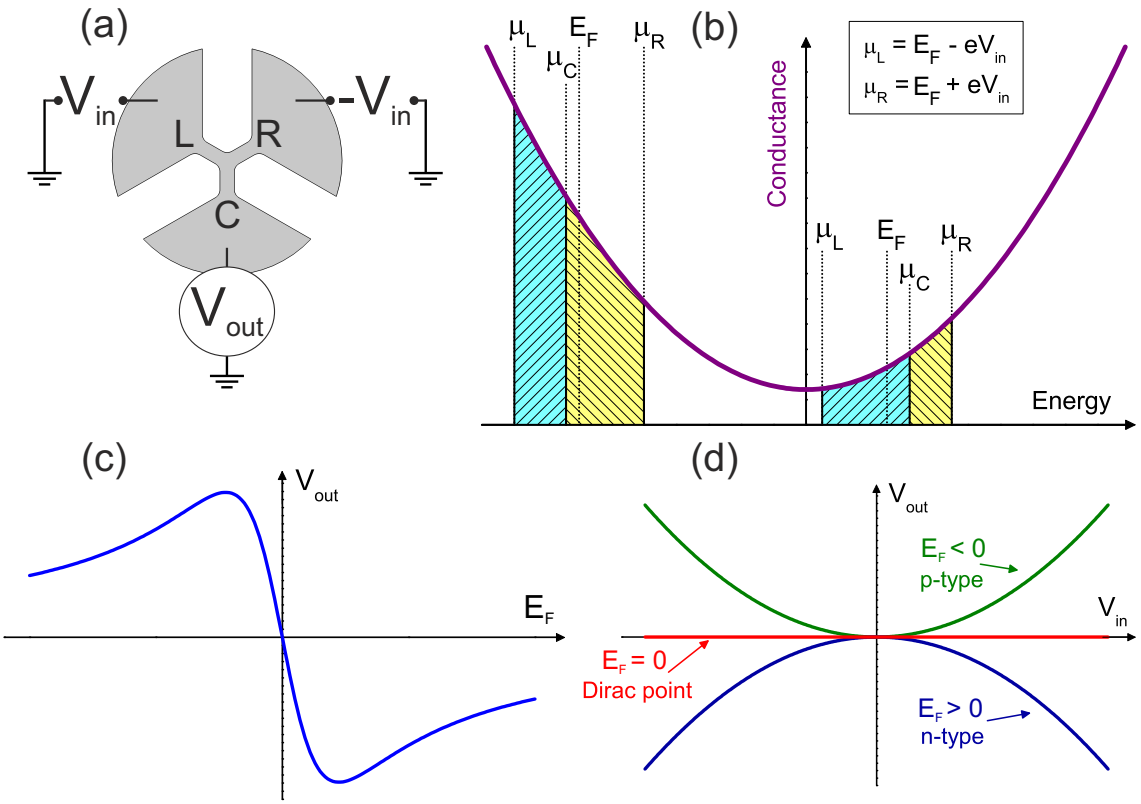

Figure 2.5: (a) Sketch of typical GTTJ rectification measurement configuration: push-pull input bias $\pm V_{in}$ applied to left (L) and right (R) terminals, output voltage V_{out} probed at floating central (C) terminal. (b) Model of the rectification mechanism in graphene [24]. μ_L, μ_R, and μ_C are the chemical potentials of terminals L, R, and C. E_F is the Fermi energy. $V_{out} = (E_F - \mu_C)/e$ is positive for p-type transport and negative for n-type transport, irrespective of the sign of V_{in}. (c) V_{out} as function of E_F and (d) as function of V_{in} for $V_{in} \ll |E_F|/e$ [equation (2.8)].

the authors showed that rectification efficiency is gate-tunable. Most importantly, output-input curves changed curvature sign when charge carrier type was changed from holes to electrons. Gate-voltage tuning showed two maximum absolute values of curvature. These results demonstrated the additional tunability of rectification voltage in graphene-based TTJs. Maximum efficiency, however, was very low (order of 1% at $V_{in} = 100$ mV). Cooling down the sample to 77 K and 4 K led to a slight increase in efficiency ($\sim$ 2-4% at $V_{in} =$ 100 mV).

Several groups around the world have reproduced rectification in a variety of different graphene three-terminal and four-terminal junctions [25–34, 96], using different types of graphene and various geometries. Table 2.1 summarizes published experimental GTTJ data, comparing efficiencies (figures of merit) achieved in those devices. All data sets were obtained at room temperature, and in ref. 24 measurements at low temperatures (77 K and 4 K) were also made. All devices can be considered diffusive, but many authors considered (quasi-)ballistic effects in order to explain observed rectification [25,27,28,30–32,96]. All measurements were made in two-point configuration, with exception of the four-point measurements in ref. 24. On a side-note, low-frequency rectification functionality was demonstrated in a four-terminal junction made from encapsulated graphene [96].

Graphene type, gate dielectric	Device geometry/ Branch sizes W/L (nm)	Efficiency (figure of merit) Max. $\lvert V_{out}/V_{in}\rvert$	Max. curvature $\lvert\alpha\rvert = \lvert V_{out}/V_{in}^2\rvert$	Ref.
Exfoliated, SiO_2 (285 nm)	Y / 200 / 20	1 % (300 K) 2 % (77 K) 4 % (4 K) at V_{in} =100 mV	0.1 V^{-1} 0.2 V^{-1} 0.4 V^{-1}	[24]
Exfoliated, SiO_2 (300 nm)	T / 200 / 200	8 % at V_{in} =500 mV	0.2 V^{-1}	[26]
Exfoliated, SiO_2 (280 nm)	T / 100 / 100 100/100 to 400/400	8 % at V_{in} =400 mV 4 % to 0.5% at V_{in} = 50 mV	0.2 V^{-1} 0.8 to 0.1 V^{-1}	[31]
Exfoliated, PEI passivated, SiO_2 (300 nm) SiO_2 (90 nm)	T / 150 / 300 T / 200 / 400 T / 300 / 300	15 % at V_{in} =100 mV 15 % at V_{in} = 50 mV 40 % at V_{in} =100 mV	1.8 V^{-1} 3 V^{-1} 4 V^{-1}	[27] [29] [34]
Grown on SiC	T / 30 / 220 T / 15-150 / 200 Y / 15-60 / 200	25 % at V_{in} = 2 V 30 % at V_{in} = 2 V	0.2 V^{-1} 0.3 V^{-1}	[25] [28,30]
CVD, Al_2O_3 (30 nm)	T / 4-54 µm / 14 µm	35 % at V_{in} = 2 V	0.3 V^{-1}	[33]

Table 2.1: Overview of published experimental GTTJ data. All measurements were made at room temperature, except where noted differently. W: branch width, L: branch length, Y: TTJ branches with 120° angles, T: TTJ branches with angles 90°-90°-180°.

Reported efficiencies show large efficiency variation, ranging from 0.5% to 40%. Because those efficiencies were attained at different input voltages (ranging from 50 mV to 2 V), direct comparison between devices is done using curvature $|\alpha|$. Also the curvatures show large variation, ranging from 0.1 to 4 V^{-1}. Most devices show low curvature below 1 V^{-1}. High curvatures $\sim$ 2-4 V^{-1} were measured in GTTJs chemically passivated with polyethyleneimine (PEI) [27,29,34]. No apparent effect from TTJ geometry can be seen from the table. Indeed, devices with micron-sized branches [33] showed similar efficiencies than devices with sub-micron-sized branches [26] and devices with sub-100-nm branches [25,28,30]. Whereas the rectification effect was observed mostly in device relying on field-effect tuning, devices without gate showed rectification as well [25,28,30].

In summary, many studies have been made on GTTJs, using different types of graphene and geometries. Reported efficiencies show large variation and no consensus on physical mechanisms has been attained. As major limitation in all but one reports we point out the possible influence of non-linearities due to contact resistances on the observed recification.

Problem definition

Despite extensive research in a couple of groups over several years, engineering and clear understanding of the rectification effect in GTTJs has still not been achieved. While suitability of graphene for TTJ rectifiers has been established, the mechanisms causing the rectification are not well understood, nor are limitations of rectification efficiency.

Important unanswered questions at the beginning and during our investigation were: (i) Is the rectification an electrostatic effect? Is it caused by the electric field effect? Are there quasi-ballistic effects? What are the intrinsic limitations of the efficiency? (ii) To what extent do external sources of disorder (such as disorder due to the substrate or rough graphene edges) limit the efficiency? How do non-linearities from contact resistances influence rectification? (iii) How does temperature affect rectification? How do local heating (Joule heating) and thermoelectric effects influence device functionality?

This project was motivated by two main goals. The first goal was to advance understanding of physical mechanisms causing the rectification effect in GTTJs. In simulations, rectification due to the field effect was calculated. GTTJs on Si/SiO_2 of different junction constriction sizes were fabricated experimentally. Effects from contact resistances were eliminated by measuring in four-point configuration. Our initial idea was to investigate geometry dependence of rectification efficiency. Constriction sizes were chosen to cover two physical length scales: > 100 nm for diffusive transport and 100 nm, roughly equal to carrier mean free path, for quasi-ballistic transport (it was difficult to realize constriction width below 100 nm). However, we stress that the assumption of quasi-ballistic transport has to be taken with a grain of salt, because so far no quantized conductance, which is expected for ballistic transport, has been reported for graphene constrictions on SiO_2. Indeed, for RIE-etched constrictions of 100 nm width and below, edge disorder becomes important, enhancing backscattering of charge carriers [94, 97]. It was therefore unclear what electrical behavior to expect in our devices, especially because in addition we needed to apply large biases (in order to have noticeable rectification efficiency). We realized at a later point that thermal effects due to Joule heating might play an important role and shifted focus in data analysis accordingly.

The second goal was to demonstrate possibility for device engineering and application implementation. In simulations, the influence of material properties, device geometry, and other parameters on rectification efficiency was studied, giving guidelines for device engineering. Most importantly, we wanted to demonstrate high efficiency experimentally in order to prove feasibility of GTTJ applications.

Chapter 3

Finite element simulations of the field effect in GTTJs

The voltage rectification effect in TTJs is not limited to ballistic devices. Diffusive devices also showed rectification functionality [9, 41]. Qualitative theoretical considerations from section 2.3 (bias-induced conductance asymmetry, zero current flowing into the central voltage-probe terminal) are indeed more general. The rectification effect is directly linked to the energy dependence of the conductivity.

In this chapter, simulations of realistic diffusive GTTJs are presented. We investigated the behavior of the rectification effect due to the electric field effect. We chose to use the finite element method (FEM) combined with a theoretical model for graphene FETs. Energy dependence of conductivity was calculated using the electric field effect. The influence on rectification behavior caused by following parameters was explored: temperature (assuming system in thermal equilibrium, no Joule-heating), charge carrier mobility, bias voltage, geometric parameters (dielectric constant and thickness of the dielectric layer, fringing-field effects), and finally potential disorder. The simulations were made with the FEM software package COMSOL Multiphysics.

3.1 Theoretical model

This section presents the theoretical model for graphene FETs from ref. 98 which was taken as framework for the simulations in this work.

Charge carrier densities in a graphene sheet are given by [83]:

$$\begin{aligned} n &= \frac{2}{\pi}\left(\frac{k_B T}{\hbar \nu_F}\right)^2 \mathcal{F}_1(\eta_F) \\ p &= \frac{2}{\pi}\left(\frac{k_B T}{\hbar \nu_F}\right)^2 \mathcal{F}_1(-\eta_F) \\ \eta_F &= \frac{E_F - E_D}{k_B T}, \end{aligned} \tag{3.1}$$

where n and p are electron and hole densities, $\mathcal{F}_1(\cdot)$ the complete Fermi-Dirac integral of index 1, η_F the normalized Fermi energy E_F with respect to the energy level of charge neutrality or Dirac energy E_D, k_B the Boltzmann constant, T the temperature, and $\nu_F = 10^6$ m/s the Fermi velocity of the charge carriers [82, 83]. At the Dirac point ($\eta_F = 0$),

intrinsic (or thermal) carrier density in graphene is given by:

$$n(\eta_F = 0) = p(\eta_F = 0) = n_{th} = \frac{\pi}{6}\left(\frac{k_B T}{\hbar \nu_F}\right)^2, \tag{3.2}$$

which gives $n_{th} \approx 10^{11}$ cm^{-2} at room temperature.

The graphene FET band diagram is illustrated in figure 3.1. Unbiased graphene in thermal equilibrium (and without external perturbations) has its Fermi level at the intersection of valence and conduction band ($E_F = E_D$). A gate voltage $V_G \neq E_F/e$ induces a net charge density $\pm e\,(n - p)$ in graphene, causing E_D to deviate from E_F. Biased graphene has non-constant voltage throughout the graphene structure. $V_{ch} \equiv -E_F/e$ designated the local voltage in the graphene channel. A local charge-voltage balance equation was established:

$$V_G - V_{ch} = \frac{e}{C}(n - p) + \frac{k_B T}{e}\eta_F, \tag{3.3}$$

where V_{ch}, η_F, $n(\eta_F)$, and $p(\eta_F)$ are local quantities (as well as E_F and E_D). C is the capacitance per unit area of the graphene sheet. In the parallel-plate capacitor approximation C is constant and given by $C \equiv C_G = \epsilon\epsilon_0/d$, where ϵ is the dielectric constant of the dielectric layer, ϵ_0 permittivity of free space and d thickness of the dielectric layer. No doping of graphene was considered here, meaning that the Dirac point was equal to 0 V. Furthermore, the work function difference, adding a constant term to the equation, was set to 0 here.
Note that in zero-temperature limit the Fermi-Dirac integral can be simplified: $\mathcal{F}_1(x) \to x^2/2$ for $x > 0$ and $\mathcal{F}_1(x) \to 0$ for $x < 0$. This means no charge carrier smearing around the Dirac point [equation (3.1)] and in accordance with equation (2.3), a square-root dependence of the Fermi energy on charge density is found:

$$\begin{aligned} E_F - E_D &= \hbar \nu_F \sqrt{\pi n} \quad (E_F > E_D), \\ E_F - E_D &= -\hbar \nu_F \sqrt{\pi p} \quad (E_F < E_D). \end{aligned}$$

Equation (3.3) reads in this case

$$V_G - V_{ch} = \frac{e}{C}\frac{(E_F - E_D)^2}{\pi\,(\hbar \nu_F)^2} + \frac{1}{e}\,(E_F - E_D)\,.$$

Charge conservation in graphene yields the static current condition:

$$\nabla \cdot \mathbf{J} = -\nabla \cdot (\sigma \nabla V_{ch}) = 0, \tag{3.4}$$

where $\mathbf{J}$ represents local current density and σ local conductivity. Graphene conductivity σ was modeled as follows:

$$\sigma = e\mu(n + p) + \sigma_{res}, \tag{3.5}$$

where μ denotes the charge carrier mobility and σ_{res} the residual conductivity. Carrier mobility was treated as constant (no dependence on temperature or charge density). For simplicity, the same μ-value was used for electrons and holes. σ_{res} was fixed to $4e^2/h$, as observed experimentally for most graphene devices on a substrate.

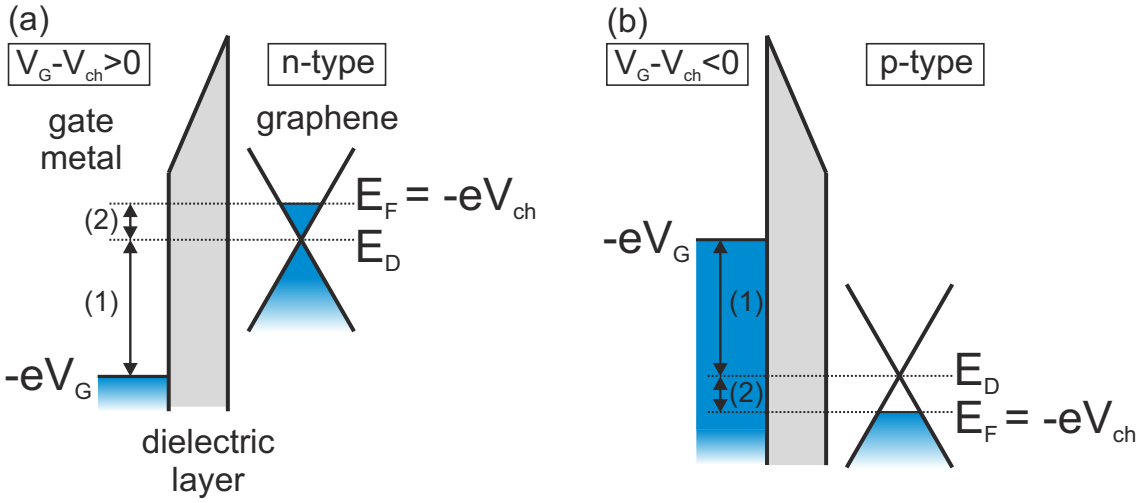

Figure 3.1: Graphene FET band diagram. The graphene sheet and the metal gate electrode are separated by a dielectric material, realizing a capacitor. V_G is the voltage applied to the gate, E_F the Fermi energy in graphene, E_D the energy level of charge neutrality (Dirac energy), and V_{ch} the voltage in graphene (channel). (1) denotes the voltage drop in the dielectric and (2) the voltage drop in graphene. (a) A positive gate voltage (with respect to V_{ch}) induces electrons in graphene. (b) A negative gate voltage (with respect to V_{ch}) induces holes in graphene.

3.2 Simulations

In the first step, simulations were made on a two-dimensional TTJ geometry with the theoretical model from the previous section. Homogeneous gate tuning of charge density in graphene was assumed (plate-capacitor approximation, $C = C_G$). We investigated effects of following parameters on rectification efficiency: temperature, carrier mobility, high biases (i.e. biases up to V_{in} =500 mV), geometric design, and finally potential disorder. In the next step, three-dimensional simulations were made, incorporating fringing effects of the electromagnetic field between gate electrode and graphene sheet. A local capacitance C was first calculated and then used in the same aforementioned 2D simulation. This way the influence of TTJ geometry on rectification efficiency was explored.

The geometry used in our simulations, shown in figure 3.2(a), is a symmetric TTJ with constrictions of equal width W and length L of 300 nm. This length scale is larger than typical mean free paths in graphene on a SiO_2 ($\sim$ 100 nm), such that the assumption of diffusive transport held. As a matter of fact, rectification efficiency does not depend on details of the 2D geometry, as long as the output voltage is probed in the middle of the geometry. For diffusive transport in general, geometric shape of a conductive channel has no influence on the voltage profile along the channel. Thus, the geometry in figure 3.2(a) is representative for all other symmetric junctions. The push-pull bias configuration was used as boundary condition: $V_{ch} = V_{in}$ on the left and $V_{ch} = -V_{in}$ on the right TTJ edge. Remaining edges of the geometry had an electrical insulation boundary condition (i.e. zero current flow perpendicular to the edges). Except for calculations from section 3.2.3, all simulations were made for $|V_{in}| \leq$100 mV, as such bias window had been commonly used in the TTJ research field. First, because 100 mV is well above the noise level of typical measurement systems, and secondly because for such bias critical breakdown current densities

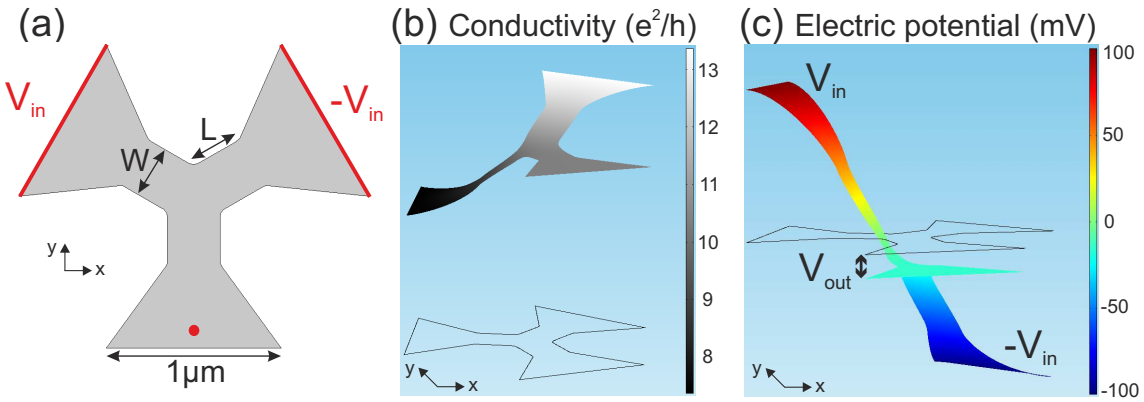

Figure 3.2: (a) 2D TTJ geometry used for rectification simulations. The geometry is delimited by a regular hexagon with common side length of 1 µm. All branches have equal length L and width W of 300 nm, angles between branches are 120°. Push-pull voltages were applied to the colored left and right edges. The dot in the central terminal indicates the output-voltage probe. (b,c) Local conductivity σ and local electric potential V_{ch} in the junction for electron transport. The applied voltages made the left branch more conductive than the right branch, causing V_{out} to be negative. Rectification efficiency was $|V_{out}/V_{in}| \approx 15\%$. This result was obtained for following parameters: V_{in} =100 mV, V_G =150 mV, T =200 K, μ =10^4 cm^2/Vs, ϵ=3.9, d =20 nm.

are not reached (for graphene constrictions those are a few mA/µm [77–79], translating to a critical voltage of a few 100 mV for 300 nm constriction width and using a conductance of 20 e^2/h). V_{out} was probed at the dot in the central branch [figure 3.2(a)]. The exact position of the dot inside the central terminal was not important, because the voltage was constant in the whole central terminal. In most cases, ϵ=3.9 was used as dielectric constant, because it corresponds to values for SiO_2 (ϵ=3.9) and hBN (ϵ=3-5 [99]), typical gate dielectrics used in experiments.

The Fermi-Dirac integral $\mathcal{F}_1(\eta_F)$ was calculated using a numerical approximation given in [100] which assures an error below 0.7% for $-\infty < \eta_F < \infty$:

$$\mathcal{F}_1(\eta_F) = \left(\frac{8}{\left[b + \eta_F + \left(|\eta_F - b|^c + a^c \right)^{1/c} \right]^2} + e^{-\eta_F} \right)^{-1},$$

with $a = 2.93$, $b = 2.41$, and $c = 2.29$. Note that the Fermi-Dirac integrals F_1 from ref. 100 and $\mathcal{F}_1$ from ref. 98 are related by $\mathcal{F}_1 = F_1/\Gamma(2) = F_1$ where $\Gamma(\cdot)$ is the gamma function.

In summary, the set of equations (3.3) to (3.5) with unknowns V_{ch} and η_F was solved over the 2D GTTJ geometry. In most cases, the capacitance C was constant (plate-capacitor approximation), and in section 3.2.4 C was also a local quantity obtained from three-dimensional electric field calculations.

3.2.1 Effect of temperature

First, the effect of temperature on rectification efficiency was investigated (plate-capacitor approximation, C kept constant). Temperature was a global system constant (system in thermal equilibrium) and no Joule-heating effects were taken into account. Simulations

were made between T =4 K and 400 K. The geometry presented in figure 3.2(a) was used. A thin (d =20 nm) SiO_2 or hBN dielectric (ϵ=3.9) was used. Those parameters ensured strong capacitive coupling between graphene and gate electrode. The graphene mobility was set to a typical value of μ=10,000 cm^2/Vs. Calculations for 4 K are made for the sake of completeness. They are not realistic, because universal conductance fluctuations can appear in diffusive graphene devices at 4 K [24].

Figure 3.2(b) shows calculated conductivity in the GTTJ at 200 K. An input bias of 100 mV was applied to the left and -100 mV to the right branch. A positive voltage of V_G=150 mV was applied to the gate, yielding electron transport. The left branch was positively biased and held therefore less electrons than the negatively biased right branch. Thus, conductivity in the left was lower than in the right branch. This asymmetric conductivity distribution throughout the graphene geometry caused a larger voltage drop in the left than in the right branch. This created negative voltage in the central branch [figure 3.2(c)]. In the case of hole transport this voltage would be positive.

Figure 3.3(a) summarizes output voltages calculated for temperatures from 4 K to 400 K with V_{in} =100 mV. The gate voltage range was chosen to show all of the relevant features of the V_{out}-curves. Hole and electron transport regimes are distinguished to the left and right of the Dirac point (here at 0 V), respectively. V_{out} was positive in the hole regime and negative in the electron regime. Each curve crossed zero at the Dirac point because in this configuration hole density in one branch was equal to electron density in the other branch. This yielded the same conductivities left and right, and thus zero output voltage. Further away from the Dirac point in gate voltage, two extrema (of equal absolute value) were seen for each curve. For high absolute V_G voltages, all curves approached zero asymptotically, because such high carrier densities led to small difference in conductivities in the branches when compared to the overall conductivity. Decreasing temperature increased the values of the extrema and moved them closer to the Dirac point. Maximum efficiency $|V_{out}/V_{in}|$ at V_{in}=100 mV increased from 10% at room temperature to $\approx$ 23% at 77 K. $V_{out}(V_{in})$-dependence is shown for different temperatures in figure 3.3(b). For each temperature, the (positive) gate voltage giving highest rectification was chosen. The same curves with opposite curvature are obtained for the opposite negative gate voltages. For high temperatures, the curves were parabolic up to V_{in}=100 mV. For low temperatures, the curves became more linear at higher V_{in}.

Conductances G as function of gate voltage are plotted in figure 3.3(c) for different temperatures. G is given by $|I| \,/\, |2V_{in}|$, where I is the current. With increasing temperature, more thermally excited carrier are generated [see equation (3.2)], leading to an increase in conductance. The less sharp V-shape led to a less efficient rectification. Thus, to conclude, increasing temperature decreased rectification efficiency. From 77 K to 400 K (temperature range relevant for application purposes), the decrease is by a factor $\sim$ 3.

3.2.2 Effect of carrier mobility

In this section, the same parameters as in the previous section were used, but calculations were made with carrier mobilities varying over two orders of magnitude: μ=10^3, 10^4, and 10^5 cm^2/Vs (corresponding to mean free paths of around 10 nm, 100 nm, and 1 µm). Those numbers covered mobility values observed experimentally in graphene devices. For the highest mobility, crossover to ballistic transport can take place. Calculations for 300 K and 77 K are shown in figure 3.4. Increasing mobility increased rectification efficiency

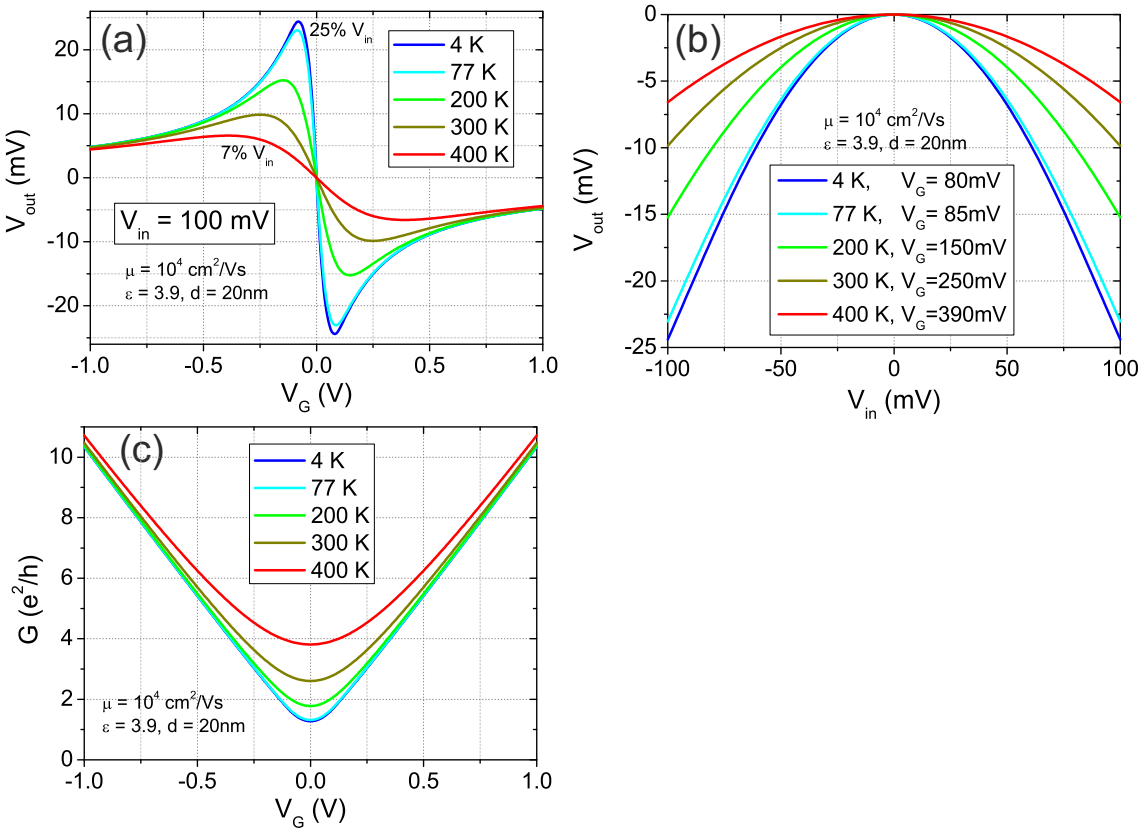

Figure 3.3: Effect of temperature on rectification efficiency. (a) V_{out} vs. V_G and (b) V_{out} vs. V_{in} for temperatures from 4 K to 400 K. Increasing temperature decreased rectification efficiency. Each curve in (b) corresponds to the gate voltage of highest rectification. $V_{out}(V_{in})$-curves for corresponding negative V_G-values are identical with opposite sign. (c) Conductance G vs. V_G for temperatures from 4 K to 400 K. Increasing temperature increased charge carrier densities around the Dirac point.

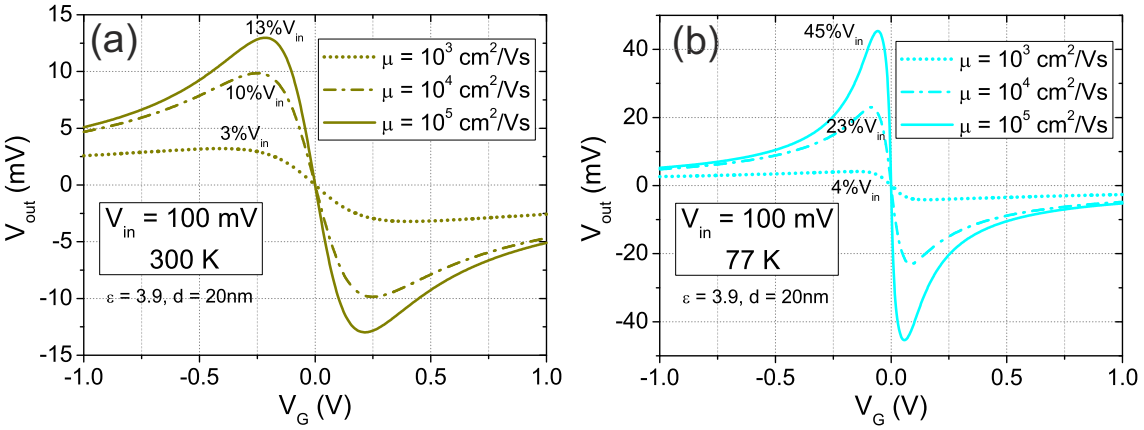

Figure 3.4: Effect of carrier mobility on rectification efficiency. Calculations were made with the same parameters as in 3.2.1, but with μ=10^3, 10^4, and 10^5 cm^2/Vs. $V_{out}(V_G)$-curves for different μ at 300 K (a) and 77K (b). Increasing mobility increased rectification efficiency at both temperatures.

at both temperatures. The increase was more pronounced for 77 K (by factor $\sim$ 10) than for 300 K (factor $\sim$ 4). Almost 50% efficiency was reached at 77 K with ultra-high μ=10^5 cm^2/Vs.

3.2.3 Effect of high bias

Simulations with high push-pull biases V_{in} = 100, 300, and 500 mV were made with the same parameters as in section 3.2.1. Higher biases were not considered, because of critical current densities at such biases. Joule-heating and current-saturation effects were not included in the calculations. Calculations for 300 K and 77 K are shown in figure 3.5(a) and (b). Increasing input bias increased rectification efficiency at both temperatures. Output curves were comparable and showed efficiencies of $\approx$30% at V_{in} =300 mV and $\approx$40% at V_{in} =500 mV.

V_{out} generally showed parabolic dependence on V_{in} for input biases smaller than 100 mV [figure 3.3(b)]. However, for sufficiently large V_{in}, the $V_{out}(V_{in})$-curve changed inflexion. V_{out} still increased with increasing V_{in}, but less pronounced than in the parabolic regime. The dependence was again parabolic over the whole V_{in} range for gate voltages further away from the Dirac point. This behavior is shown in figure 3.5(c) for gate voltages close to the Dirac point. With increasing V_{in}, the curves went from a parabolic to linear to sublinear dependence. This implies that efficiencies $|V_{out}/V_{in}|$ first depended linearly on V_{in}, then saturated at the inflexion point [see figure 3.5(d)]. Increasing V_{in} generally resulted in a stronger rectification. However, when V_G was too close to the Dirac point, such that $|V_{in}| \gg |V_G - V_{Dirac}|$, then the difference in conductivities in the left and right branch was negligible, leading to ineffective rectification.

To conclude, increasing input bias increases efficiency, but eventually leads to efficiency saturation. Between V_{in} = 0 and 500 mV (relevant range for application purposes), the increase is roughly by a factor $\sim$ 2-3.

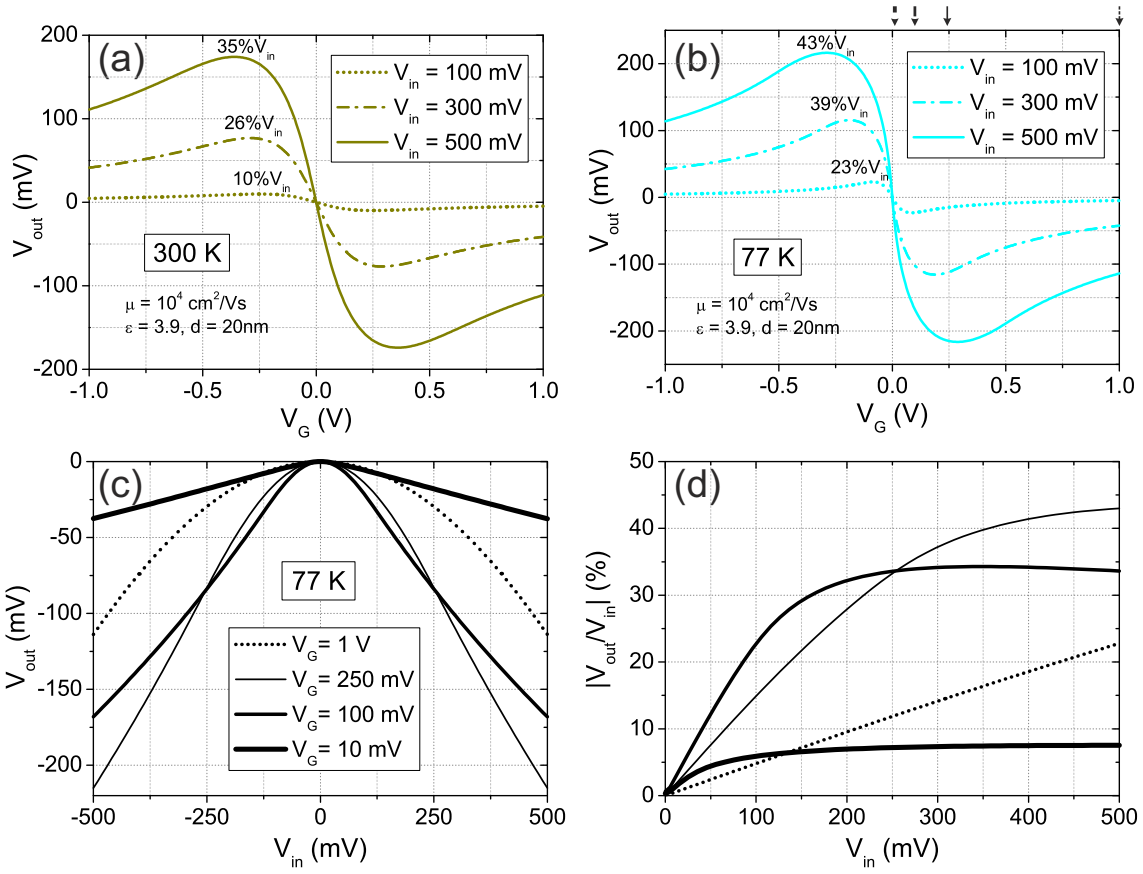

Figure 3.5: Effect of high bias on rectification efficiency. Calculations were made with the same parameters as in 3.2.1, but with V_{in} = 100, 300, and 500 mV. (a,b) $V_{out}(V_G)$-curves for high push-pull biases at 300 K and 77 K. Rectification efficiency increased with V_{in}. (c) $V_{out}(V_{in})$-dependence at gate voltages marked by arrows in (b). (d) Efficiency as function of V_{in} for the gate-voltage values used in (c). The $V_{out}(V_{in})$ curve changed curvature at high bias, leading to efficiency saturation.

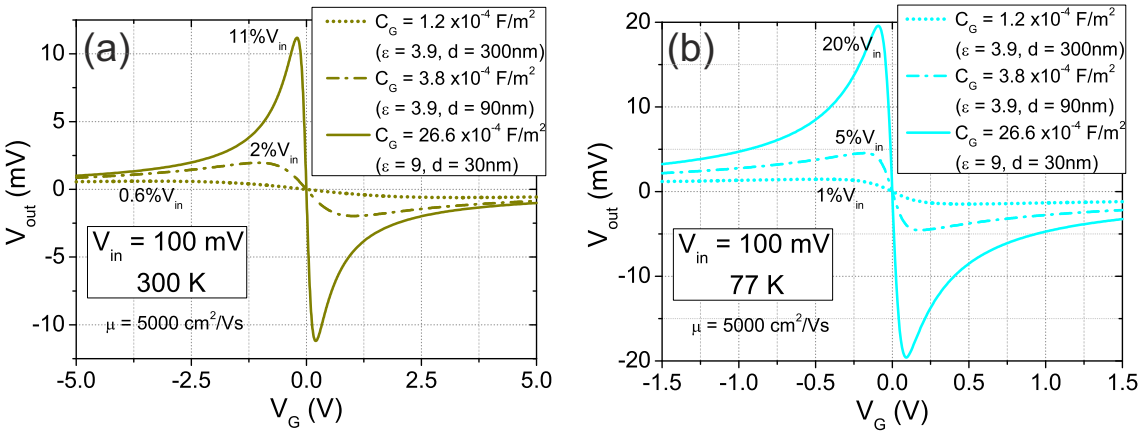

Figure 3.6: Effect of capacitance per unit area $C_G = \epsilon\epsilon_0/d$ on rectification efficiency (plate-capacitor approximation). $V_{out}(V_G)$-curves for different C_G at 300 K (a) and 77 K (b). Increasing C_G increased rectification efficiency.

3.2.4 Effect of geometry

This section deals with the influence of geometry on rectification efficiency. First, in a 2D simulation using the plate-capacitor approximation, we examined how the capacitance (per unit area) $C = C_G = \epsilon\epsilon_0/d$ influences efficiency. Then, calculating local capacitance C due to electric fringing fields at the TTJ branches, 2D simulation with local C were made.

Capacitance in plate-capacitor approximation

The effect of different capacitances C_G on rectification efficiency was calculated, using the plate-capacitor approximation. For this, standard SiO_2 dielectric (ϵ=3.9) with typical thicknesses of d =300 nm and 90 nm was chosen. In addition, calculations for a thin Al_2O_3 dielectric layer (ϵ=9, d=30 nm) were made, corresponding to the gate dielectric used in ref. [33]. The capacitances were $C_G = 1.2 \cdot 10^{-4}$, $3.8 \cdot 10^{-4}$, and $26.6 \cdot 10^{-4}$ F/m^2. μ=5000 cm^2/Vs was used in all cases (a carrier mobility realistically achieved with both dielectric materials). Calculations for 300 K and 77 K are shown in figure 3.6. Increasing C_G increased rectification efficiency at both temperatures. Increasing C_G by a factor 20 showed an increase in efficiency by roughly 20. At the same time, maxima of V_{out}-curves shifted closer to the Dirac point in gate voltage.

In conclusion, rectification efficiency increased with capacitive coupling. Strong increase (factor $\sim$ 20) was observed over a range of C_G-values relevant for application purposes.

Local capacitance due to fringing fields

In this section, we explain the effect on efficiency of local capacitance C, due to electric fringing fields at the TTJ branches. When TTJ channels are small in size compared to gate area, fringing electric field lines (stray fields) become important. They lead to charge accumulation at the graphene edges, so that the plate-capacitor approximation is no longer valid. This is especially relevant if the branch width W is comparable to or smaller than the dielectric thickness d. A theoretical analysis of this effect can be found in references 101 and 102. Experimentally, conductance enhancement at the edge of graphene devices

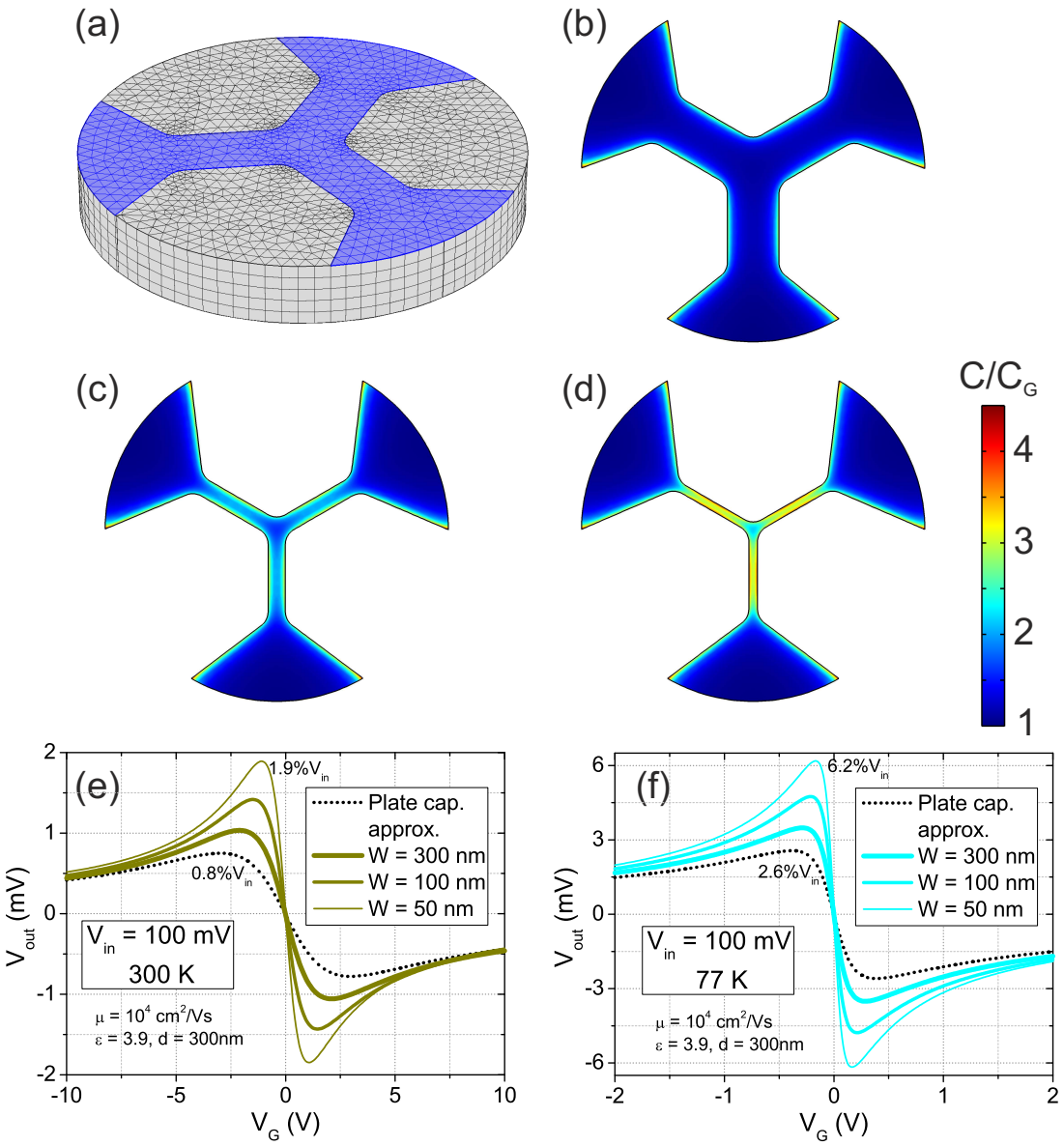

Figure 3.7: Effect of fringing fields on rectification efficiency. (a) TTJ geometry (colored) on top of dielectric slab (1 μm circle radius, 300 nm thickness). At the bottom of the slab, the gate voltage is applied. The mesh shows decomposition of the geometry into finite elements. (b)-(d) Local capacitances per unit area C calculated for junctions with L =500 nm and W =300, 100, and 50 nm (C_G is C under plate-capacitor approximation). Long narrow branches favored enhanced local capacitive coupling. (e,f) V_{out} vs. V_G for different C calculated with geometries (b)-(d) at 300 K and 77 K.

were measured by scanning-gate microscopy [103].

Including fringing fields to our simulations was done by first calculating the local capacitance per unit area C between TTJ geometry and gate electrode, then using C to run 2D simulations. As charge accumulation from stray fields is strongest for large d/W ratio, we choose $d = 300$ nm and $W = 300$, 100, 50 nm while keeping $L = 500$ nm. As in the 2D simulations from the previous sections, the electrical contacts were located roughly 1 µm from the junction center. A dielectric constant $\epsilon = 3.9$ and carrier mobility of $\mu = 10^4$ $\mathrm{cm}^2/\mathrm{Vs}$ were used.

Local capacitances calculated for those parameters are shown in figure 3.7(b)-(d). The capacitances were enhanced at the graphene edges. Decreasing channel width further enhanced C. In panel (d), $C \approx 3 \cdot C_G$ in each branch. In general, regions more than 500 nm away from the edges can be considered as bulk ($C = C_G$). Corresponding rectification curves for 300 K and 77 K are shown in figures 3.7(e) and (f), with rectification curves calculated under plate-capacitor approximation added for comparison. Efficiency increased with decreasing branch width, up to a factor ~ 2 here. At the same time, maxima of V_{out}-curves shifted closer to the Dirac point in gate voltage. This behavior is similar to rectification enhancement seen in the previous section (figure 3.6).

In summary, increasing capacitive coupling between graphene channel and gate electrode enhanced the rectification effect. Strong coupling was achieved either by choosing dielectric parameters for large C_G-values or by designing the TTJ geometry with long and narrow branches and $W < d$.

3.2.5 Effect of potential disorder

Due to substrate-induced disorder, electron-hole puddles are found in graphene on SiO_2. From experiments, standard deviation of disorder charge density n^* was estimated to be $4 \cdot 10^{10}$ cm^{-2} [85], $4 \cdot 10^{11}$ cm^{-2} [86] and $4.3 \cdot 10^{11}$ cm^{-2} [87]. Spatial extension of these puddles was reported as 20 to 30 nm. The puddles are spread randomly over the graphene sheet. Corresponding potential disorder was reported of the order of 100 meV [104]. Those values indicate that electron-hole puddles can affect electronic transport in our devices. They were therefore included in the simulations.

The overall effect of disorder can be thought of as modulation of the applied gate voltage, impacting on graphene carrier density. The electron-hole puddles were thus modeled by adding a disorder 'gate' voltage V^* to the balance equation (3.3). V^* was defined as periodic potential $V^*(x,y) = \left(\frac{en^*}{C_G}\right) \cdot \left[\sin(k \cdot x) + \sin(k \cdot y)\right]/2$, where (x,y) are coordinates in the graphene plane. The spacial frequency k was chosen to yield puddles with a diameter of 30 nm.

Simulations were made with the same TTJ geometry as in section 3.2.1. Figure 3.8(a) shows V^* on the TTJ geometry. V^* induced disorder on normalized Fermi energy η_F^*. The amplitude of $k_B T \eta_F^*$ at the Dirac point defined our potential disorder and was denoted Δ. The Δ-values obtained from the n^*-values used in figure 3.8 are listed in table 3.1. $\Delta = 100$ meV is in agreement with reported experimental values [104]. Figures 3.8(b) and (c) show $V_{out}(V_G)$-curves for different n^* for 300 K and 77 K, respectively. Increasing n^*-amplitudes decreased rectification efficiency. For 77 K, decrease (factor ~ 8) was stronger than for

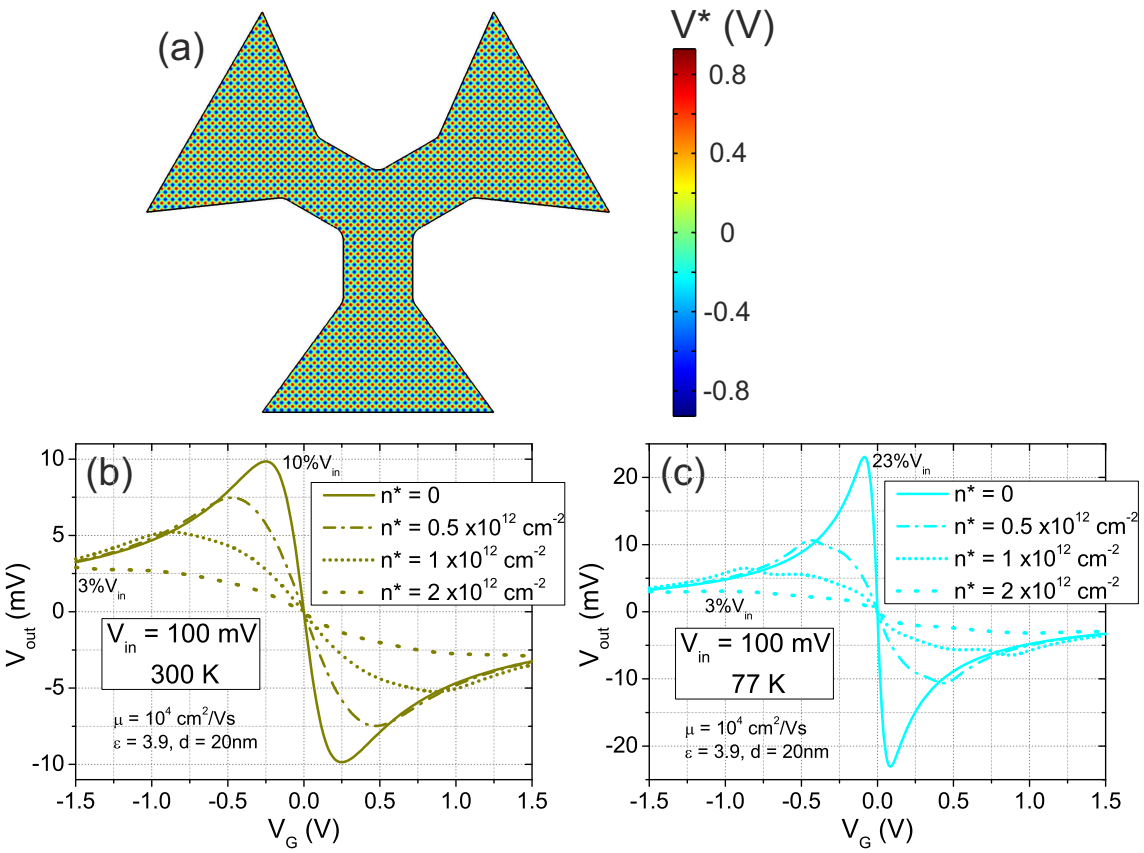

Figure 3.8: Effect of potential disorder (electron-hole puddles) on rectification efficiency. (a) Disorder potential V^* on TTJ geometry with $L = W$ =300 nm. Puddle size was 30 nm. The amplitude of V^* is equivalent to the disorder charge density n^* (see table 3.1). Calculations were made with the same parameters as in section 3.2.1, now including V^*. (b,c) $V_{out}(V_G)$-curves for different disorder densities at 300 K and 77 K. Increasing n^* decreases rectification efficiency.

Amplitudes		
n^* (10^{12} cm^{-2})	V^* (V)	Δ (meV)
0.5	0.5	80
1	0.9	110
2	1.9	170

Table 3.1: Correspondence between amplitudes of n^*, $V^* = en^*/C_G$ ($C_G = 1.7 \cdot 10^{-3}$ F/m^2), and Δ. Those values were used for the calculations shown in figure 3.8.

300 K (factor ~ 4). The output voltage was affected by disorder only within (roughly) the gate-voltage range $\pm V^*$ around the Dirac point. For finite n^*, the maximum of $|V_{out}|$ was given by the value of $|V_{out}|$ at $V_G \approx \pm V^*$, and the maximum of $|V_{out}|$ seen for $n^* = 0$ was not attained.

In summary, increasing potential disorder decreased rectification efficiency. Over the range of experimentally observed n^*-values, the decrease was by a factor ~ 3 at 300 K and ~ 8 at 77 K.

3.2.6 Efficiency limit

In the following, the efficiency limit of our model is calculated by using extreme, yet realistic device parameters. Due to finite graphene conductivity at the Dirac point, rectification efficiency of GTTJs is expected to be intrinsically limited (in addition to other limiting factors such as finite temperature and potential disorder). Taking into account the previous sections, the efficiency limit was calculated for 300 K and 77 K by choosing key parameters appropriately.

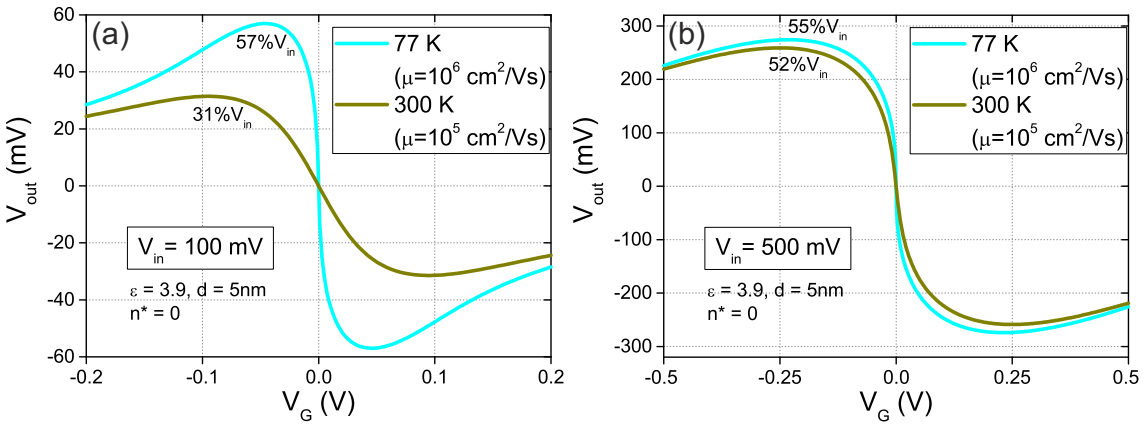

Figure 3.9: $V_{out}(V_G)$-curves for 77 K ($\mu = 10^6$ cm^2/Vs) and 300 K ($\mu = 10^5$ cm^2/Vs); ϵ= 3.9, $d = 5$ nm, $n^* = 0$. (a) $V_{in} = 100$ mV, (b) $V_{in} = 500$ mV.

High efficiency is obtained for high charge carrier mobility, low potential disorder, and high capacitive gate coupling. All those conditions can be achieved in hBN-graphene-hBN devices with thin hBN layer used as gate dielectric. For the latter, 5 nm thickness was chosen because of tunneling currents at thinner layers [105]. Realistic mobilities are 1,000,000 cm^2/Vs at 77 K and 100,000 cm^2/Vs at 300 K [76]. The mean free paths corresponding to such mobilities are ~ 10 µm and ~ 1 µm, implying that our diffusive-transport simulations are only compatible for TTJ channel lengths of several microns. Calculations were made without potential disorder. Figure 3.9(a) shows simulated $V_{out}(V_G)$-curves at V_{in} =100 mV. An efficiency of 57% was reached for 77 K. Panel (b) shows $V_{out}(V_G)$-curves at V_{in} =500 mV. For both temperatures, efficiencies were roughly around $\approx 55\%$. No further increase in efficiency was found from additional simulations with V_{in} >500 mV. Therefore, $\approx 60\%$ efficiency can be considered the efficiency limit of our model.

3.2.7 Comparison with experimental data from literature

In this section, simulation results are compared to the experimental results summarized in table 2.1. In particular, simulations made with device parameters from references 24 and 33 are compared to the respective experimental results.

Using parameters from [24], simulations were made with $V_{in} = 100$ mV, $T = 300$ K and 77 K, $\mu = 4000$ cm^2/Vs, $\epsilon = 3.9$, $d = 285$ nm. The case $T = 4$ K was not considered, because at this temperature universal conductance fluctuations dominate electronic transport properties, and they were not included in the theoretical model. Calculated $V_{out}(V_G)$-curves are shown in figure 3.10. Maximum rectification efficiency without potential disorder was of the order of 1 mV for both temperatures ($|\alpha| \approx 0.1$ V^{-1}) . For $\Delta \approx 100$ meV, efficiencies remained of similar order of magnitude. Maximum efficiencies were achieved at gate voltage a few volts away from the Dirac point. Thus, the field effect can explain experimental findings from [24]. Referring to comparable devices in table 2.1 (graphene on SiO_2 of $\approx$ 300 nm thickness), experimental results from references 26 and 31 can be explained by the simulations as well.

Next, devices from ref. 33 were simulated using V_{in} =2 V, T =300 K, μ=2200 cm^2/Vs, ϵ=9, d =30 nm. Those devices had branch sizes L and W of several microns and were therefore certainly diffusive. Calculated $V_{out}(V_G)$-curves are shown in figure 3.11. Maximum rectification efficiency was $\approx 45\%$, and this value remained roughly the same adding potential disorder. The devices from ref. 33 showed roughly similar efficiencies. Thus, the fields effect can explain the high efficiencies achieved in those diffusive devices.

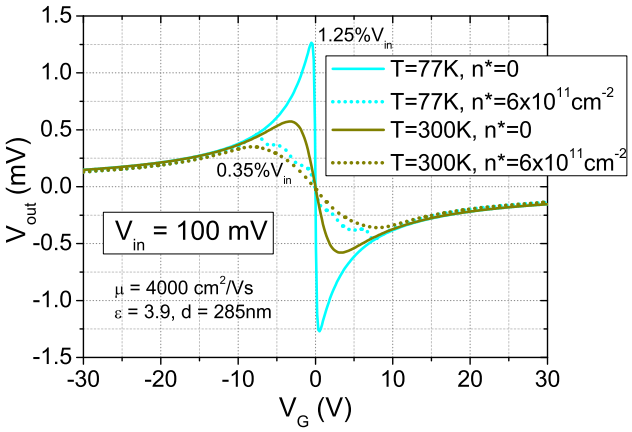

Figure 3.10: Simulation of the device from ref. 24. Calculations were made for 77 K and 300 K, with and without potential disorder. Rectification efficiency was low ($\approx 1\%$ and below). Efficiency decreased adding potential disorder. $n^* = 6{\cdot}10^{11}$ cm^{-2} corresponds to $V^* \approx 8$ V and $\Delta \approx 100$ meV.

Reports of high efficiencies in [27,29,34] cannot be explained using our simulations. However, when comparing efficiencies from [27] and [34], the observed efficiency enhancement by a factor ~ 2 can be explained by the different SiO_2 thicknesses (300 and 90 nm). This geometric dependence is deduced from figure 3.6(a), showing that efficiency increases by a factor ~ 2 going from d =300 to 90 nm ($C_G = 1.2$ to $3.8 \cdot 10^{-4}$ F/m^2).

Our field-effect model is not suited to make predictions for the results from [25, 28, 30], because those devices did not have a gate. However, it is possible to calculate the efficiency for the reported electron density $n = 5 \cdot 10^{12}$ cm^{-2} in [30]. n corresponds to a gate voltage $V_G = en/C_G = 3$ V, yielding $V_{out} \approx$ -0.6 V for $V_{in} = 2$ V and an efficiency $\approx 30\%$,

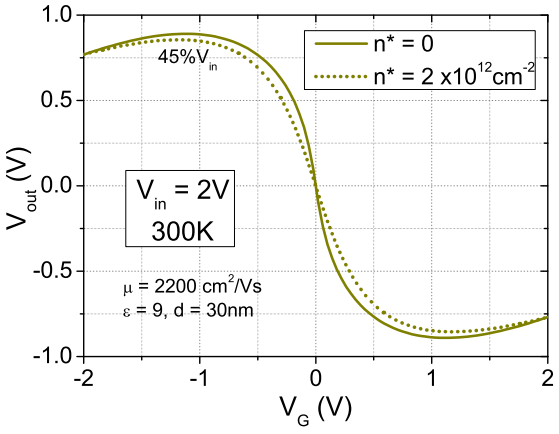

Figure 3.11: Simulation of devices from ref. 33. Calculations were made for 300 K, with and without potential disorder. Rectification efficiency was $\approx 45\%$ without potential disorder. Adding disorder did not decrease efficiency noticeably. $n^* = 2 \cdot 10^{12}$ cm^{-2} corresponds to $V^* \approx 1.2$ V and $\Delta \approx 130$ meV.

in agreement with the experimental results.

In conclusion, our simulations can explain the rectification effect in some of the experimental GTTJ data from literature. This suggests that rectification can be attributed to the field effect in many cases.

3.3 Conclusions

The field-effect model and FEM simulations presented in this chapter can partially explain the rectification effect observed experimentally. The dependence of output voltage on gate and input voltage demonstrated in experiments is well described in the simulations. Also quantitatively, our simulations are able to explain many efficiencies reported in experimental literature. Thus, the field effect can explain the rectification effect in many experiments. In devices with efficiencies considerably higher than in our simulations, other physical mechanisms seem to result in rectification of output voltages.

Following engineering guidelines are derived from the simulations. Generally, in order to achieve high rectification efficiency in GTTJs, a sharp transition from electron to hole transport is desirable. It can be achieved by:

- cooling the device. Cooling reduces thermal charge carrier smearing around the Dirac point, increasing efficiency.
- good graphene material quality. Both high charge carrier mobility and low potential disorder favor high efficiency.
- high capacitive coupling to the gate. It is obtained for thin dielectric layers of large dielectric constant. Fringing fields between TTJ branches, strongest for long and narrow branches (with respect to the dielectric layer thickness), increase capacitive coupling as well.

Furthermore, efficiency saturation at high input voltages was found. All parameter values were varied over ranges realistically achievable in experiments. Optimizing efficiency with these variations resulted in both strong (factor ~ 20) and weak (factor ~ 2) efficiency enhancement, but above all efficiency stayed below 50%. For extreme but still realistic device parameters, the maximum rectification efficiency achievable in our model saturates around $\approx 60\%$.

Chapter 4

Experimental methods

The present chapter describes the experimental methods. First, device fabrication is described. Next, our methods for electrical characterization are presented.

4.1 Device fabrication

In this section, the fabrication steps for GTTJs are presented. Detailed information on the fabrication processes are found in the appendix. In the first step, graphene single crystals (called flakes) were obtained from natural graphite by exfoliation (mechanical peeling/cleavage) with adhesive tape. The device substrate consisted of highly doped silicon chips (dies) with a SiO_2 layer at the surface. The silicon acts as back-gate. In the second step, Raman spectroscopy identified if the graphene flake was a monolayer crystal. In the third step, the graphene flake was scanned by atomic force microscopy (AFM) in order to check cleanliness and flatness of the flake. Subsequently, metal contacts were defined on the flake with electron-beam lithography (EBL), and the flake was then etched into a TTJ geometry. The chip was finally glued to a chip carrier and wire bonding connected the graphene terminals to chip carrier pins.

4.1.1 Graphene flake exfoliation

The fabrication started with a 4-inch oxidized silicon wafer (thermally grown SiO_2 layer of 285±5 nm thickness) from *NOVA Electronic Materials*. A SiO_2 thicknesses of $\approx$ 280 nm was found to yields high intensity contrast between graphene and substrate under white light illumination [106]. This facilitates spotting of graphene flakes in an optical microscope. Standard photo-lithography techniques were used to make metal crosses and pads (100x100 μm^2) on the wafer. This process involves spinning the wafer with photo-resist, exposing it to ultraviolet light under a mask which projects the desired patterns, chemically developing the exposed areas, depositing metal in those areas (physical vapor deposition, 5 nm titanium and 45 nm gold), and finally removing the photo-resist. The photo-lithography process can be completed within four hours. The crosses are helpful for locating graphene flakes and for alignments during EBL steps. The pads were used for wire bonding. The wafer was diced into 7x7 mm^2 chips, which were then cleaned with acetone, isopropanol (IPA), and by oxygen plasma ashing.

The starting material for graphene consisted of mm-sized chunks of natural graphite (*'Graphenium'* by *NGS Naturgraphit GmbH*). They were put on a stripe of adhesive tape (from *Nitto Denko*, typically used for wafer dicing). The stripe was folded onto itself and

then gently peeled off [13]. Repeating this process ten times creates a large density of graphite pieces with smooth surfaces. A chip was pushed with the thumb onto the tape at an area of high graphite density. The chip was pushed vertically as hard as possible for several seconds. Afterward, the chip was gently removed. Mostly graphite was transferred onto the chip, but few-layer graphene as well as bi- and monolayer graphene were found on (almost) every chip. We note that if the graphite density on the tape is too high, the yield of monolayer graphene flakes is very low. At the same time, a chip surface with a lot of graphite can make the flake inaccessible for electrical contacts and can be problematic for the lift-off process (described in section 4.1.3).

4.1.2 Flake characterization

The choice of graphene flakes for device fabrication was based on characterization by optical microscopy, Raman spectroscopy, and atomic force microscopy. Optical inspection takes around 30 minutes per chip. A Raman spectrum takes around 5 minutes and an AFM scan around 20 minutes per sample.

Optical microscopy

After graphite exfoliation and deposition, the chips were inspected in an optical microscope. Graphene flakes with a lateral size of 5 µm or larger were identified and located. Figure 4.1(a) shows an optical image of the surface of a Si/SiO_2 chip covered with thick graphite pieces. The golden areas are metalized areas. The crosses served as orientation and alignment markers and the pads as targets for bonding wires. The frame in the center denotes the location of a monolayer graphene flake, several microns wide and visible to the naked eye under microscope magnification. Figure 4.1(b) shows a close-up of the flake. With a bit of experience it is surprisingly easy to distinguish by eye monolayer from bilayer graphene (and of course from thicker layers). However, in order to be certain about the number of layers, Raman spectroscopy was used in the next step.

Raman spectroscopy

Since the discovery of graphene, researchers have used Raman spectroscopy as highly effective and reliable method to identify the number of layers of graphene flakes [107, 108]. We took a Raman spectrum for each flake, using a confocal Raman microscope from *WITec GmbH* (or *Bruker Senterra*) with a 532-nm laser at 0.5 mW (0.2 mW). A typical spectrum is shown in figure 4.1(e). The characteristic peaks are the G peak at 1580 cm^{-1} and 2D peak at 2670 cm^{-1}. Only for monolayer graphene is the 2D peak more intense than the G peak.

The G peak is due to a one-phonon (first-order) process, associated with an in-plane vibration mode [109]. It involves a high-frequency phonon at the Brillouin zone center. The 2D peak is due to two-phonon (second-order) intervalley processes. It is associated with the overtone of the in-plane breathing modes of the hexagonal carbon-ring. The processes involve two phonons with opposite wave vectors in the highest optical phonon branch near the K point. Whereas the D peak requires a defect for its activation and is only seen in defective graphene, the 2D peak is always seen in the spectrum, because momentum conservation by the two phonons with opposite wave vectors is always satisfied. The third peak in the spectrum in figure 4.1(e), denoted D+D", is due to processes similar to the processes responsible for the 2D peak.

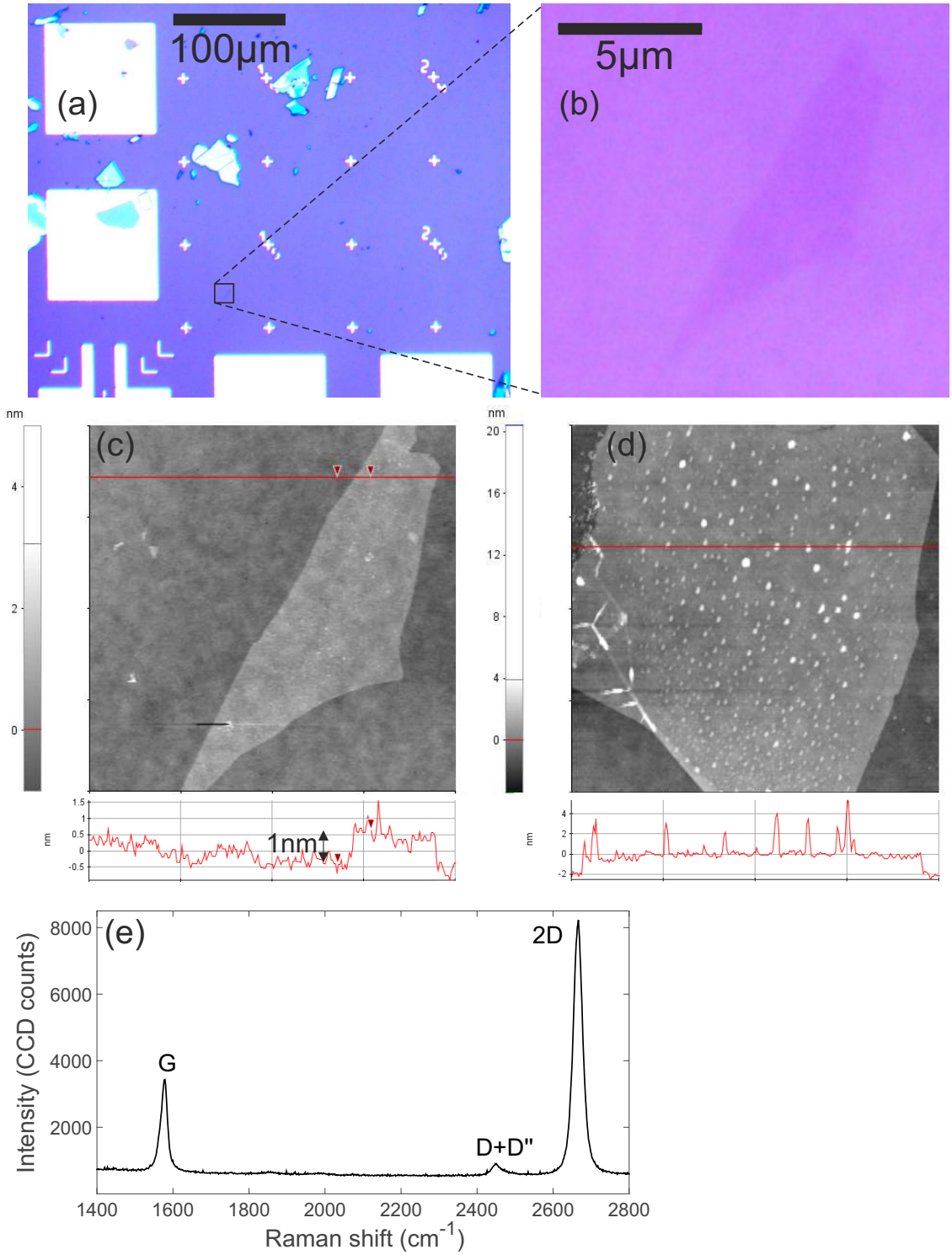

Figure 4.1: (a) Optical micrograph of graphite pieces on a Si/SiO_2 chip with gold markers and bonding pads. (b) Close-up optical micrograph and (c) AFM topography scan (10x10 μm^2) of a graphene flake. Lower part shows flake height of 1 nm. (d) AFM topography scan (10x10 μm^2) of a flake with contaminations or bubbles. (e) Raman spectrum of graphene (532-nm laser) with main peaks at 1580 cm^{-1} (G peak) and 2670 cm^{-1} (2D peak).

In bilayer graphene interaction of the graphene planes causes the valence and conduction bands to split into four bands, with a different splitting for electrons and holes. The resulting four contributions to the 2D peak cause a peak splitting, which results in easily distinguished mono- and bilayer-graphene Raman signatures.

Atomic force microscopy

A topography scan with AFM revealed cleanliness and roughness of the flake. Clean means that there is no or only little glue residue coverage of the flake. Furthermore, flakes with wrinkles or bubbles (air pockets) were discarded. Because of their size (several nm in height and 100 nm in diameter), glue contaminations and bubbles may lead to inhomogeneous devices with unwanted local doping. Flakes with wrinkles tend to detach or crumble during resist spinning. An example of a flake with wrinkles and contaminations or bubbles is shown in figure 4.1(d). An AFM scan also reveals narrow cracks which electrically isolate graphene areas. All of the aforementioned imperfections are generally not evident from an optical picture or from a Raman spectrum.

A further important requirement is flatness of the flakes. Flat means a root mean square (rms) areal roughness of 0.3 nm or less, which is comparable to the roughness of the underlying SiO_2. Figure 4.1(c) shows the topography from an AFM scan of the flake shown in (b). The flake had a rms roughness of ≈ 0.27 nm (SiO_2 roughness ≈ 0.24 nm). This suggests that the flake was free from contaminations and suitable for device processing. A flake height of around 1 nm was typically observed. Also higher steps were measured. Such steps are larger than the theoretical 'thickness' of graphene (0.35 nm), but can be explained by different interaction forces between tip-graphene and tip-SiO_2 or by adsorbed water molecules trapped between graphene and substrate.

4.1.3 Nanostructure fabrication

Electrical contacts were fabricated by standard EBL (*Raith 150 One*): First, the chip was spin-coated with resist. Then a high-energy electron beam exposed the resist locally, defining the areas for electrical contacts. The exposed areas were removed in a developer and leaved parts of the graphene flake and SiO_2 uncovered. The chip was put in a vacuum chamber where metal was sublimated by an electron beam and deposited onto the chip surface (physical vapor deposition). The chip was then put in acetone in order to remove the resist (lift-off process). Electrical contacts remained on the chip surface. Each contact made an electrical connection between a certain area of the graphene flake and a bonding pad located further away from the flake. Fabricated contacts can be seen in figure 4.2(a).

Two layers of Poly(methyl methacrylate) (PMMA) resist were spun: first PMMA 50K ($\approx$ 180 nm layer thickness), then PMMA 950K ($\approx$ 100 nm layer thickness). PMMA 950K was needed for the EBL process. The PMMA 50K layer was added because it is easier to remove than 950K (due to smaller molecular weight) and leaves the graphene surface less contaminated after the lift-off. Moreover, because the critical dose for PMMA 50K is smaller than for PMMA 950K, an undercut profile is created which is favorable for lift-off. The contacts consisted of 1 nm Cr (adhesion layer) and 50 nm Au. The whole process needs around three to four hours.

A second EBL step was made to define the submicron-sized TTJ geometry on the graphene

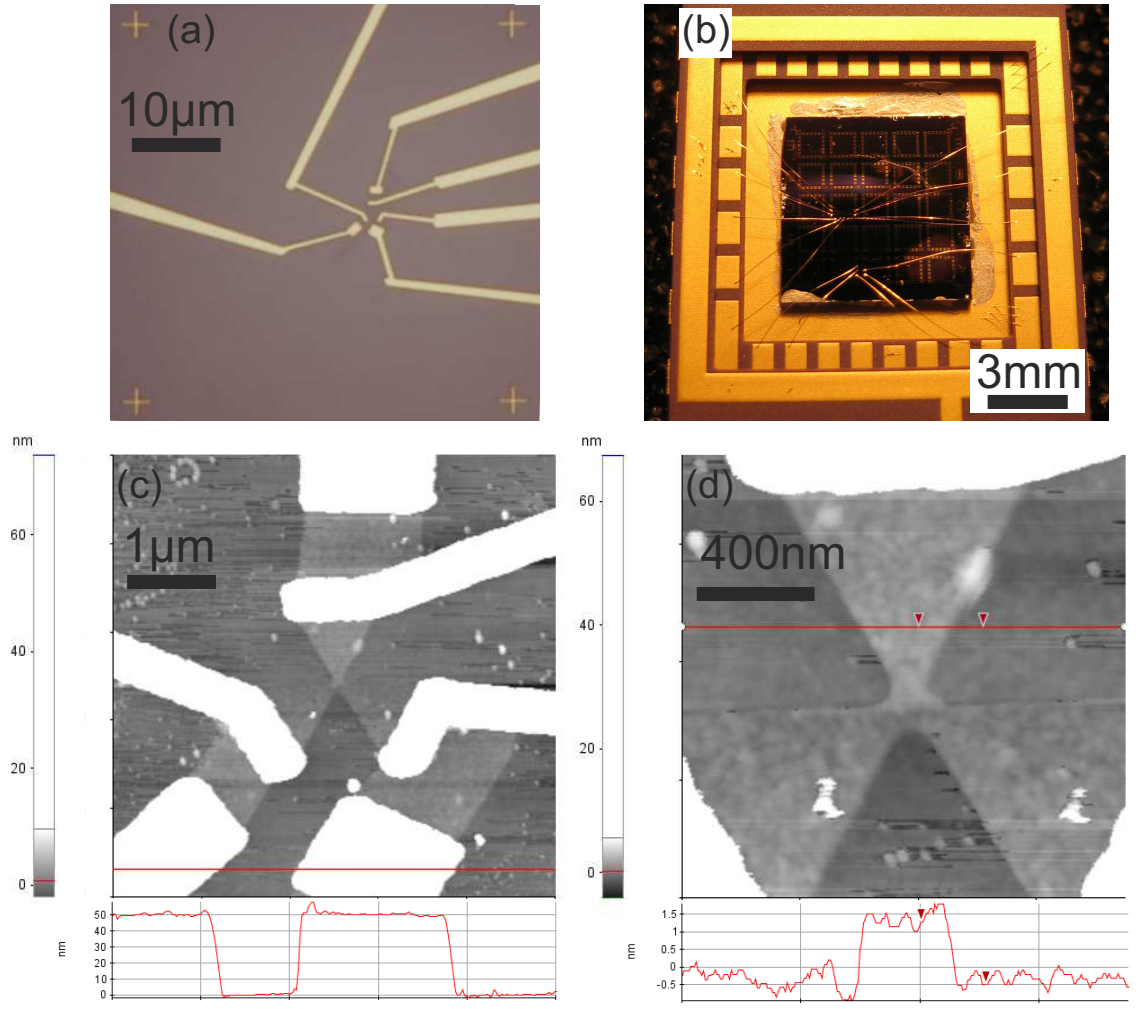

Figure 4.2: (a) Optical micrograph of the graphene flake from figure 4.1(b,c) after evaporation of metal contacts (Cr/Au). The crosses were alignment markers for the etching step. (b) Chip glued to chip carrier. Bonding wires connected carrier pads (pins) to pads on the chip. (c) AFM scan topography of the etched graphene flake and surrounding electrical contacts. In the dark-gray areas graphene is etched away. A few contamination 'dots' are seen. Lower part: cross-section along red line, showing contacts of 50 nm height. (d) Close-up of (c), showing the etched TTJ geometry with constriction widths of $\approx$ 100 nm. Lower part: cross-section along red line, indicating a graphene height of 1.5 nm, comparable to the as-deposited flake [see figure 4.1(c)].

flake. For this, a layer of PMMA 950K resist was spun onto the chip. After electron-beam exposure and development, the chip was put in an Ar/O_2 plasma mixture (reactive ion etching) which etched away unprotected graphene areas. The resist was then removed in acetone. This whole process needs 2 hours. An AFM scan showed the defined geometry which consisted of conductive graphene channels and insulating SiO_2 areas [figure 4.2(c,d)]. In order to compensate for proximity effects, the junction channels were designed about 20 nm shorter and 20 nm wider than the aimed channel sizes. Typical resolution of this EBL patterning method is 20 nm. With the crosses about ±20 µm away from the graphene flake [figure 4.2(a)], an alignment precision with respect to the contacts of about 0.2 µm was achieved.

In order to truly compare electrical properties of different devices, it is important to make all GTTJs with the same contact configuration design. We arranged the contacts centro-symmetrically, as shown in figures 3.2(a) and 4.2(c,d). Each device had at least two contacts per terminal: one to apply voltage and another one closer to the junction to measure the voltage. In this way, contact resistances which may be non-linear were excluded from the measurements. Contact resistances have so far not been excluded in publications on GTTJs, with the exception of ref. 24.

As a final fabrication step, the chip was glued with conductive silver paste to a chip carrier [figure 4.2(b)]. The paste connected electrically the silicon substrate to the carrier. The electrical contact pads on the chip were connected to the chip-carrier pins by wedge bonding with aluminum wires (25 µm diameter). The device was then ready to be measured.

4.1.4 TTJ design

In this section, our TTJ design is discussed. The TTJ geometry was defined by three triangular graphene areas joined together by three constrictions, as illustrated in figure 3.2(a). The junction was characterized by branches of equal length L and width W and an angle of 120° between the branches. The geometry was delimited by a regular hexagon with common side length of 1 µm. The electrical contacts were located at the three outer edges of the geometry. An example of a GTTJ with $L = W = 100$ nm is shown in figure 4.2(d). Measurements were made on GTTJs of different sizes from $L = W = 100$ to 400 nm. The substrate of each graphene device was used as back-gate to tune the charge carrier density in the graphene sheet. The junction area was separated from the nearest contacts by about 1 µm in order to avoid screening of the gate by the contacts.

At least two electrical contacts were made for each terminal [figure 4.2(c)]. That way the typical rectification-measurement set-up with two SMUs, shown and explained in figure 4.6, formed a four-point measurement. Such a measurement configuration ensures that the contact resistances of the contacts at the two biased terminals are excluded from the measured resistance. Each SMU adapts the applied bias at the *force* contacts such that the desired bias voltage $\pm V_{in}$ is measured at the *sense* contacts. These *sense* contacts and the contact measuring V_{out} were positioned symmetrically around the junction.

Contact resistances show generally non-linear behavior and it is therefore important to exclude effects due to the contacts from the measurements. We consider a current-voltage curve as shown in figure 4.3. In this two-point measurement a bias voltage was applied to one contact and another contact is grounded. The contacts were connected via a graphene

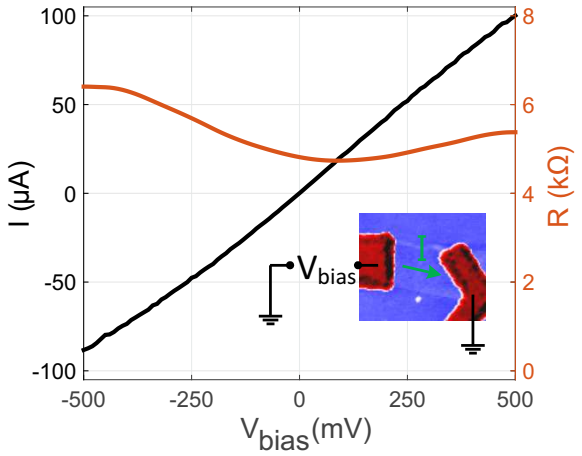

Figure 4.3: Typical room-temperature current-voltage curve (I–V curve) with grounded back-gate voltage. The device is shown as inset. Current I (black curve) and resistance $R = dV_{bias}/dI$ (orange curve) are plotted as function of bias V_{bias} spanning a window from -0.5 to 0.5 V.

channel. The total resistance R contained contact resistances from both contacts. The current I showed saturation behavior at high absolute bias values, and accordingly R showed a noticeable dependence on the bias voltage. For the high applied electric field (0.5 V/μm), current saturation tendencies is expected (see section 5.3.2). However, the fact that I and R were not symmetric with respect to the bias voltage sign points to non-linear contact resistances.

4.2 Electrical characterization

In this section, our methods for electrical characterization of GTTJs are presented. The section includes descriptions of the measurement set-up, comments on conductance hysteresis, the measurement procedure, and the motivation to use the odd and symmetric parts for data analysis. The electrical property of interest to us is voltage-rectification functionality of the devices. This functionality was investigated by applying a push-pull voltage on two terminals and measuring the voltage as function of gate voltage at the third terminal. At the same time, the current flowing through the junction was measured as function of gate voltage in the same measurement. Appendix A presents the raw data from rectification measurements at room temperature and liquid-nitrogen (LN_2) temperature made on GTTJ devices of different sizes.

4.2.1 Measurement set-up

The electrical characterization equipment consisted of three source measurement units (SMUs) *Keithley 236* and a *Keithley 2000* multimeter. The operation principle of an SMU is shown in figure 4.4(c). The user wants to apply a voltage V to a device. At the *force* terminal a voltage V' is applied and simultaneously at the *sense* terminal the voltage is measured. The applied voltage is adapted such that the *sense* voltage equals V. In addition, the current A is measured by an ammeter. This way the contact resistance at the *force* terminal is compensated for.

The chip carrier was plugged into a connector at the end of a metal stick [figure 4.4(a) and

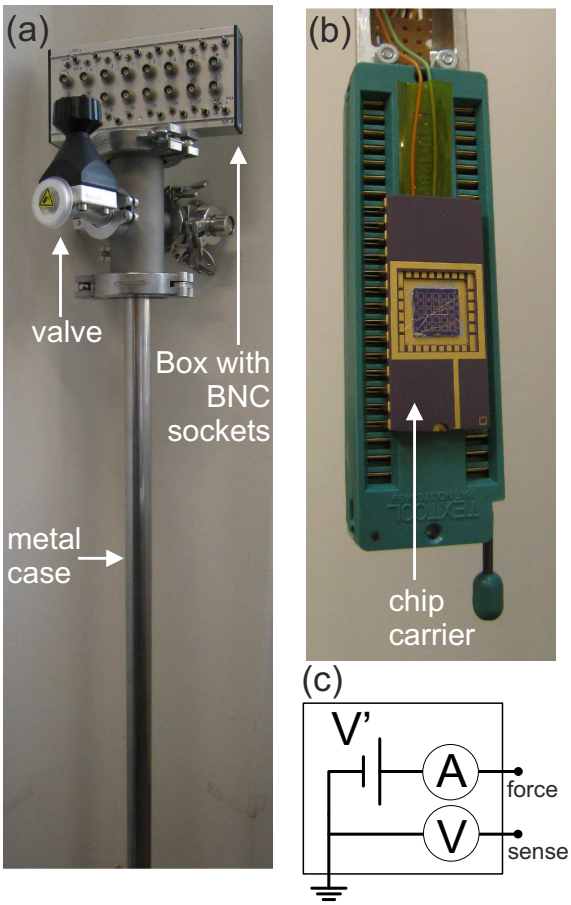

Figure 4.4: (a) Cryogenic measurement stick with BNC sockets (at box on top) and valve for vacuum pump connection. (b) Chip carrier with bonded chip, plugged into the socket at the end of the measurement stick. (c) Operation principle of a source measurement unit (SMU). See main text for explanations.

(b)]. Low-temperature measurements can be made with such a stick by immersing it into a Dewar filled with a cryogenic fluid (common ones are liquid nitrogen and liquid helium). We used liquid nitrogen for our experiments. A connector socket connected the chip carrier pins to BNC sockets. The chip temperature was determined by a *Pt-100* temperature sensor located on the connector below the chip carrier.

In order to create a stable environment for the device, the cryogenic stick was pumped (to $\approx 10^{-4}$ mbar) and then N_2 gas was put inside (to atmospheric pressure). Pumping removes adsorbed water from the graphene (top) surface, because the boiling point is lowered with decreasing pressure. The atmospheric pressure on the inside of the stick prevents air from the outside to leak in, because of the absence of a pressure difference. When cooling down the stick with liquid nitrogen, the gas inside of the stick transfers heat from the chip to the metal case by diffusion. With N_2 gas the device is cooled more efficiently than in vacuum. The gas was put into the stick by flushing the stick with a N_2-gun.

Room temperature corresponded to a chip temperature of 296 K. By inserting the measurement stick into liquid nitrogen, a chip temperature of 87±1 K was obtained. The nitrogen boiling point (77 K) was not reached on the chip, because the chip carrier socket was thermally connected to the outside of the Dewar via the measurement stick.

4.2.2 Room-temperature conductance hysteresis

A major well-known property of graphene-on-SiO_2 FETs at ambient conditions is hysteresis of electronic transport [110]. While hysteretic effects are interesting for memory-device applications, they are generally undesired — as they are in this work. The conductance hysteresis is mainly caused by charge transfer to trap states located at the graphene-SiO_2 interface. The time scales of the trapping mechanisms are comparable to the time scale of gate-voltage sweeps used in our measurements (order of magnitude $\sim$ 1 min). Parameters in our measurements were chosen in order to reduce the influence of hysteretic effects on the studied rectification effect. At liquid-nitrogen temperatures, no hysteresis was observed.

Our measurement set-up determined a certain communication time between measurement instruments and computer software. This step time varied from 0.6 s to 0.7 s, depending on measurement configuration. Setting a certain gate-voltage sweep step (for example 0.1 V per step) then defined a certain sweep rate ($\approx$ 0.15 V/s in this case). We call sweep time t_{sweep} the time taken for the gate-voltage sweep in one direction. The sweep step also set the resolution of the measurement. The sweep step was chosen such that the hysteresis was reduced and that important curve features, mainly sharpness around the Dirac point, were resolved by enough measurement points.

Figure 4.5 shows typical hysteretic behavior of the conductance as function of back-gate voltage at room temperature, as observed in our graphene devices. The gate voltage was swept back and forth around 0 V in a voltage window spanning from -20 to 20 V. Such a symmetric sweep-loop yielded reproducible conductance curves under continuous sweeping. Each curve was recorded for a different sweep time t_{sweep}, or correspondingly for a different sweep rate. A slow sweep of the order of tens of mV/s (t_{sweep}= 20 min) showed large hysteresis, whereas a faster sweep of the order of 1 V/s (t_{sweep}= 48 s) reduced the hysteresis considerably. For t_{sweep}= 26 s the curves from both sweep directions overlapped. This conductance curve without hysteresis revealed that the Dirac point was around 6 V. For long sweep times (t_{sweep}= 20 min) the conductance minimum was obtained at lower gate voltages when sweeping from left to right and higher gate voltages when sweeping from right to left. Such behavior is referred to as positive hysteresis [110].

In the literature, positive hysteresis is attributed to a combination of multiple charge trapping mechanisms, including charge transfer to nearby trap sites and adsorbates, and interfacial redox reactions [110–113]. In all of those processes, charge carriers accumulate at the graphene-SiO_2 interface, leading to gate-voltage screening. Under positive gate bias, electrons are continuously injected from graphene into trap states, so that the graphene sheet consecutively 'sees' a less positive potential than the gate voltage. As a result, the graphene sheet appears increasingly p-doped. Under negative gate bias, this process is reversed: electrons are released from trap states (or analogously: holes are trapped) and the graphene sheet 'sees' a less negative potential, leading seemingly to enhanced n-doping. Thus, sweeping the gate voltage at constant rate in a loop around 0 V leads to continuous charging and discharging of trap states, causing reproducible conductance hysteresis.

The largest contribution to the hysteresis (more than 80%) comes from SiO_2 interface charge trapping [113]. Those are tunneling processes where charge carriers are injected from graphene to SiO_2 interface trapping site such as dangling bonds. In addition, charge carriers can tunnel to water adsorbed at the graphene surface. The Si-SiO_2 interface trap density is typically of the order of 10^{11} cm^{-2} [110]. From experiments the num-

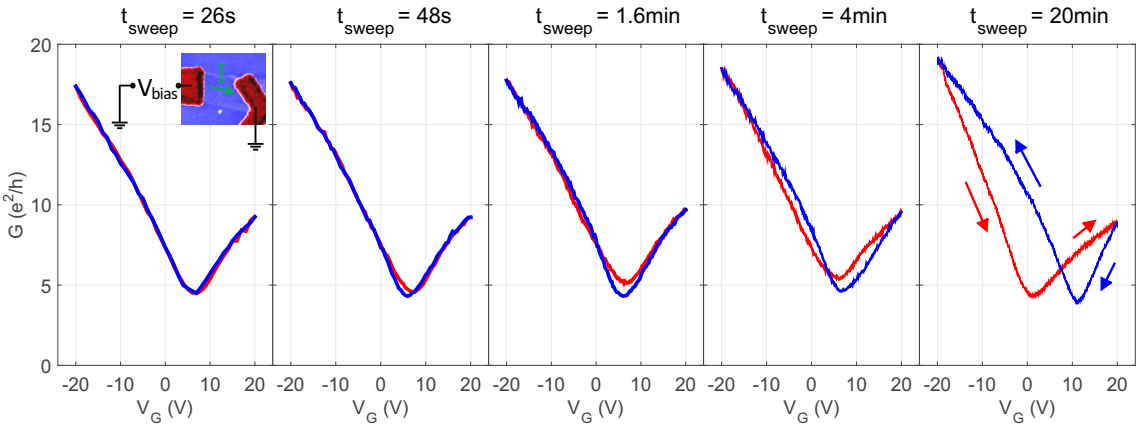

Figure 4.5: Typical room-temperature hysteresis of conductance G as function of back-gate voltage V_G, swept in a loop around 0 V for different sweep times t_{sweep} (time taken for the sweep in one direction). The hysteresis depends on the gate-voltage sweep time (sweep rate). It was pronounced for long sweep times (t_{sweep}= 20 min or a rate of about 30 mV/s) and was not seen for short sweep times (t_{sweep} = 48 s or about 0.8 V/s). Arrows indicate sweep direction. The inset on the left shows the measured device: a graphene sheet on Si/SiO_2 in the center ($\approx$ 1 µm^2) and metal contacts (red) to the left and right. V_{bias} = 1 mV, I is the electric current.

ber of charges trapped per units area is estimated from the shift in Dirac point voltage: $n_{trapped} = C_G \Delta V_{Dirac}/(2e)$. For t_{sweep}= 20 min (in figure 4.5), ΔV_{Dirac}=10 V which gives $n_{trapped} = 4 \cdot 10^{11}$ cm^{-2}.
The other important contribution (about 20%) comes from an interfacial redox reaction due to air enclosed in nano-sized gaps between graphene and SiO_2 [113]. This reaction involves dissociation of adsorbed water and oxygen at the graphene surface (O_2+2H_2O+4e$^-$ $\rightleftharpoons$ 4OH^-). The negatively charged OH^- molecules lead to p-doping of graphene. The above process can explain the net p-doping commonly observed in our devices. Even in experiments with GFETs in vacuum, this doping process can persist due to air pockets below graphene.
Contaminants such as resist residues are believed to cause or mediate charge trapping and can contribute to the hysteresis as well [111]. Charge injection into bulk SiO_2 trap sites can be largely excluded as possible contribution to hysteresis, because such processes need large electric fields (of the order of 0.1 V/nm [110, 112]) to be initiated. For the GFETs used in this work, this corresponds to a gate voltage of the order of 30 V, which is at the upper limit of what we applied. Furthermore, experimentally determined trapping time constants [112] rule out bulk SiO_2 traps.
Improvements in hysteresis suppression should be achievable by using a flat substrate material free of dangling bonds. Also air gaps between graphene and substrate must be avoided during fabrication.

We want to emphasize that the charge-trapping process originates from the properties of the graphene-SiO_2 interface and is not affected by the position of the Dirac point. The electric field between gate and graphene initiates the charge trapping, and the voltage difference between gate voltage and Dirac point is not relevant for this process. In case of graphene with a Dirac point different from 0 V, sweeping the gate voltage in a loop symmetrically around the Dirac point causes continuous drifting of the conductance curves.

Drift direction depends on whether the gate voltage is predominantly positive or negative. While the drift may eventually stop due to trap-state saturation, charge screening yields inaccurate information on intrinsic graphene properties such as Dirac point or charge carrier mobility. Moreover, measuring at high gate voltages has the disadvantage of higher risk of dielectric breakdown. In conclusion, measurements should be made preferentially with gate-voltage sweeps around 0 V.

In summary, this section describes GFET conductance hysteresis at room temperature and presents a measurement strategy which helps reducing the influence of hysteretic effects on electronic transport. We conclude that the hysteresis is not seen while sweeping the gate voltage at a certain rate. The sweep must be done symmetrically around V_G =0 V in order to avoid drifts (Dirac point, carrier mobility drifts).

4.2.3 Measurement procedure

Voltage-rectification measurements aimed at determining the output voltage V_{out} at one terminal of the GTTJ, while the other two terminals were biased by a symmetric input voltage (push-pull bias) $\pm V_{in}$. The current I flowing through the junction was measured simultaneously. Both V_{out} and I were measured as function of back-gate voltage V_G. The measurement scheme is shown in figure 4.6(a) — for more details see the caption of figure A.1. The conductance G was determined by $G = |I| \,/\, |2V_{in}|$. We were mainly interested in the gate and input-voltage dependence of the output voltage. The goal was to determine maximum voltage-rectification efficiency $|V_{out,sym}/V_{in}|$.

The measurement procedure was as follows. In the beginning, all electrical contacts were grounded. Then a push-pull voltage V_{in} was applied and the gate voltage was repeatedly swept symmetrically around 0 V. During the sweeps $V_{out}(V_G)$ and $I(V_G)$ were logged. Next, a different push-pull voltage was applied and the gate voltage was swept as before. This scheme was then repeated for opposite push-pull voltage. Measurements were first made at room temperature, then at liquid-nitrogen (LN_2) temperature (if the sample still worked). Sample F32 was repeatedly measured at both temperatures (thermal cycling).

Gate-voltage sweep repetition leads to reproducible curves. As explained in section 4.2.2, sweeping symmetrically around 0 V avoids system drifts. The V_{out} and I curves were both averaged in order to remove noise contributions from system and sample. Averaging was made over at least 10 gate-voltage sweep cycles. Averaged room-temperature raw data obtained for V_{in} = 100 mV is shown in figure 4.6(b). Error bars correspond to the standard deviation resulting from curve averaging. Typically, the error for the conductance curves was negligible and therefore not shown on the plots; the same applies to all data sets measured at LN_2 temperature. Because no hysteretic effects were seen at LN_2 temperature, it was not necessary to sweep symmetrically around 0 V in that case. Instead, the gate voltage was swept symmetrically around the Dirac point.

From the current $I(V_G)$ electron and hole transport regimes were distinguished. In figure 4.6(b) the Dirac point lies around V_G=1.5 V. The sign of V_{out} changes from positive to negative when going from hole to electron transport. The gate-voltage sweep window was chosen such that the V_{out} swing from positive to negative was clearly seen. An upper limit for gate-voltage values was given by risk of electrical breakthrough via the SiO_2 layer. During the wire-bonding step, cracks in the SiO_2 layer below the bonding pads can form, reducing the critical electric field at which the electrical insulation breaks down. To be on

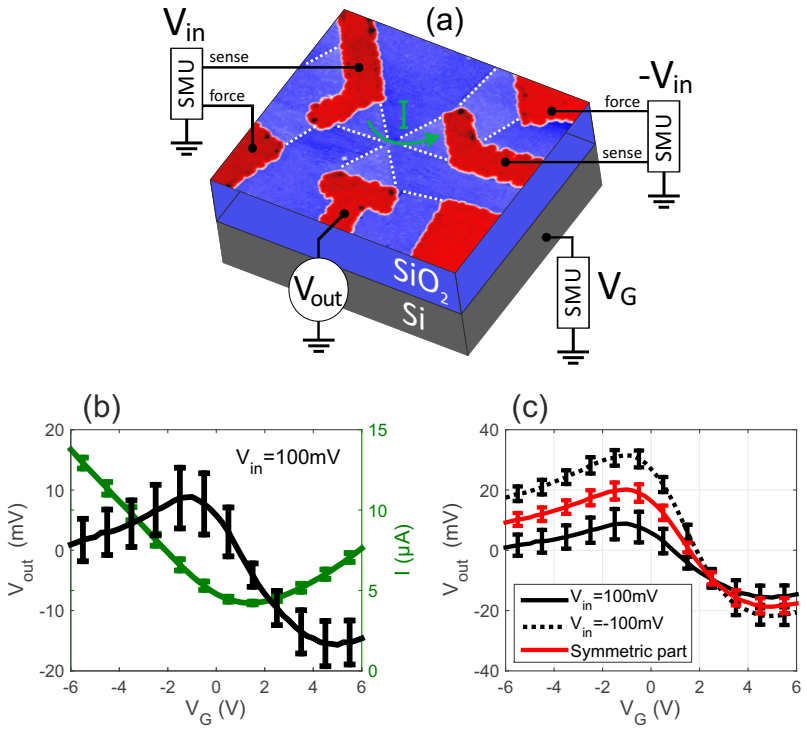

Figure 4.6: (a) Measurement configuration of a GTTJ (4x4 μm^2 atomic force micrograph) on Si/SiO_2. The width of the constriction in the junction center is 100 nm. Graphene terminals are pale blue, SiO_2 dark blue, and electrical contacts in red. Graphene edges are indicated by dotted lines. Graphene connects each inner contact to an adjacent outer one. Push-pull bias $\pm V_{in}$ was applied to two terminals, generating a current I. SMUs with *force* and *sense* outputs formed a four-point measurement. SMU *sense* outputs were connected to inner contacts. V_{out} was probed with a multimeter at the remaining inner contact. The remaining outer contact was electrically disconnected. A back-gate voltage V_G, applied to the silicon substrate, tuned the charge density in the GTTJ. (b) Averaged raw data obtained for $V_{in} = 100$ mV at room temperature: V_{out} and I as function of V_G. The sign of V_{out} changed from positive to negative when going from hole to electron transport. Averaging was made over 50 gate-voltage sweep cycles. (c) Comparison of $V_{out}(V_G)$ for positive and negative input voltage ($V_{in} = \pm 100$ mV), and the symmetric part $[V_{out}(V_{in}) + V_{out}(-V_{in})]/2$. For both negative and positive V_{in}, V_{out} showed similar behavior, demonstrating the rectifying property of the GTTJ. Unwanted contributions to V_{out} stemming from asymmetry are removed in the symmetric part.

the safe side, we did not apply gate voltages larger than 30 V. Gate leakage currents due to non-ideal cables were present at all gate voltages. They were typically of the order of 100 pA at V_G=30 V (corresponding to a cable resistance of 300 GΩ) and could be neglected in all our measurements. We always monitored the leakage current during measurements in order to check that no electrical breakthrough had happened. Another essential limiting factor on the gate-voltage range (and bias-voltage range) is the breakdown current density of graphene constrictions, reported as a few mA per µm channel width [78, 79]. We made measurements at low current densities, staying below 0.2 mA/µm, as well as at high densities, reaching peak values of 1.2 mA/µm.

Figure 4.6(c) compares $V_{out}(V_G)$ for positive and negative input voltage ($V_{in} = \pm 100$mV) and the symmetric part $V_{out,sym} = [V_{out}(V_{in}) + V_{out}(-V_{in})]/2$. For both negative and positive V_{in}, V_{out} showed a swing from positive to negative values when going from hole to electron transport. As this $V_{out}(V_G)$ behavior is similar for V_{in} of both signs, the rectification property of the GTTJ is demonstrated. The reason for calculating the symmetric part is elaborated in section 4.2.4. For the sample shown in figure 4.6, $V_{out,sym}$ was nearly antisymmetric with respect to the Dirac point, featuring extrema of almost identical absolute value for electron and hole transport. Maximum efficiency $|V_{out,sym}/V_{in}| \approx 20\%$.

4.2.4 Odd and symmetric part of output voltage

Unwanted contributions to V_{out} stemming from device asymmetry were removed by calculating odd and symmetric part of V_{out}. Fabricating perfectly symmetric devices was difficult because the EBL nanostructure fabrication step resulted in TTJ geometries shifted with respect to the contacts by up to 200 nm. In addition, constriction sizes deviated from designed sizes by $\approx \pm 20$ nm. Furthermore, it was not possible to assure a perfectly homogeneous Dirac point over the whole graphene area, as residual resist and other contaminations induced local doping. In the following, we show that the odd part of V_{out} contains contributions from device asymmetry and that the symmetric part of V_{out} contains the rectification effect.

V_{out} as function of V_{in} consists of an even (symmetric) and odd part:

$$V_{out} = V_{out,sym} + V_{out,odd}.$$

For $V_{in} \to 0$ those parts are given by:

$$V_{out,sym} = c_0 + c_2 \cdot V_{in}^2 + \mathcal{O}(V_{in}^4),$$
$$V_{out,odd} = c_1 \cdot V_{in} + c_3 \cdot V_{in}^3 + \mathcal{O}(V_{in}^5),$$

with coefficients c_i (i=0,1,2,...). $c_0 = 0$ because $V_{out}(V_{in} = 0) = 0$. As explained below, c_1 was interpreted as the contribution of device asymmetry and c_2 was attributed to the rectification effect. For simplicity, we neglected terms of higher order.

With the data sets $V_{out}(V_{in})$ and $V_{out}(-V_{in})$ at hand, the symmetric part was obtained from experimental data as follows:

$$V_{out,sym} = \left[V_{out}(V_{in}) + V_{out}(-V_{in})\right]/2, \tag{4.1}$$

and the odd part from

$$V_{out,odd} = \left[V_{out}(V_{in}) - V_{out}(-V_{in})\right]/2. \tag{4.2}$$

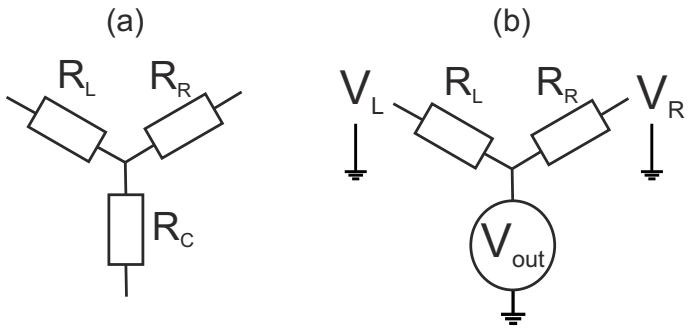

Figure 4.7: (a) TTJ modeled as lumped resistance network. R_L, R_R, and R_C are independent unequal resistances. (b) Typical rectification-measurement configuration: applying biases V_L and V_R to two terminals, probing the output voltage at the remaining terminal. Two more analogous configurations are obtained with biases applied to terminals R and C, and terminals C and L, respectively.

For a proper interpretation of odd and symmetric parts, we modeled the TTJ as node of independent resistances (conductances) $R_L = 1/G_L$, $R_R = 1/G_R$, $R_C = 1/G_C$, shown schematically in figure 4.7(a). In general, these conductances are different from each other ($R_L \neq R_R \neq R_C$) and the TTJ thus asymmetric. This is the case if, for example, the junction constrictions have different widths or if the terminals are doped differently. The typical measurement configuration for determining rectification functionality [shown for example in figure 4.6(a)] is depicted schematically in figure 4.7(b). Under push-pull bias $V_L = -V_R = V_{in}$, V_{out} is given by simple voltage division: $V_{out} = \frac{R_R - R_L}{R_R + R_L} V_{in} = \frac{G_L - G_R}{G_L + G_R} V_{in}$. Analogously, for $V_L = -V_R = -V_{in}$, $V_{out} = \frac{G_R - G_L}{G_R + G_L} V_{in}$. By definition, odd and symmetric parts are thus given by the following expressions:

$$V_{out,odd} = \frac{G_L - G_R}{G_L + G_R} V_{in}, \tag{4.3}$$

and $V_{out,sym} = 0$. For the other two measurement configurations $V_{out,odd}/V_{in}$ is equal to the ratios $\frac{G_R - G_C}{G_R + G_C}$ and $\frac{G_C - G_L}{G_C + G_L}$.

Equation (4.3) shows that for an asymmetric TTJ $V_{out,odd}$ is nonzero and proportional to V_{in}, whereas for a symmetric TTJ $V_{out,odd} = 0$. The ratio $\frac{G_L - G_R}{G_L + G_R}$ corresponds to c_1. We therefore interpreted $V_{out,odd}$ as representing the contribution of device asymmetry. From experiments presented later we saw that $V_{out,odd}$ showed no dependence on higher-order exponents of V_{in}, which justifies neglecting c_3 and higher-order coefficients. c_1 is gate-voltage dependent if $G_L(V_G)$ and $G_R(V_G)$ differ in shape (due to different carrier mobilities or Dirac points).

Irrespective of whether the TTJ is symmetric or not, $V_{out,sym}$ is always zero in the model. Experiments, however, showed that generally $V_{out,sym} \neq 0$. For this reason, we interpreted $V_{out,sym}$ as representing a contribution from the rectification effect. In experiments, $V_{out,odd}$ generally showed a roughly parabolic dependence on V_{in}, and did clearly not depend on V_{in}^4 or higher-order terms. Thus, c_4 and higher-order coefficients were neglected.

Using odd part and total conductance G, it is possible to calculate individual terminal conductances G_L and G_R. G is given by $G^{-1} = G_L^{-1} + G_R^{-1}$. Together with (4.3) one

obtains:

$$G_L = \frac{2V_{in}}{V_{in} - V_{out,odd}} G,$$
$$G_R = \frac{2V_{in}}{V_{in} + V_{out,odd}} G. \tag{4.4}$$

Calculations for the other two measurement configurations are analogous. If the TTJ is characterized in all three configurations, each terminal conductance G_L, G_R, and G_C can be calculated twice, i.e. from two separate measurements.

Chapter 5

Discussion of rectification measurements on GTTJs

In this chapter, the experimental data presented in appendix A is analyzed and discussed. Thermal processes giving rise to rectification effects are proposed. Furthermore, device symmetry is shown to influence rectification efficiency. The conclusions are helpful for the understanding of rectification mechanisms of GTTJs (and TTJs in general) and for future device engineering.

5.1 Rectification functionality and efficiencies

In this section, a typical set of experimental data demonstrating the rectification effect is discussed. For this, room-temperature data from sample F32 [figure 4.6(a)] with 100 nm constriction width is used (full raw data shown in figures A.2 and A.3). Figure 5.1 shows voltage rectification functionality of this device. Under push-pull bias configuration $V_L = -V_R = V_{in}$, for both $V_{in} > 0$ and < 0, the output voltage V_{out} showed a pronounced gate-voltage dependence: V_{out} swung smoothly from positive to negative [figure 5.1(a)]. The Dirac point (≈ 1.5 V) is determined from conductance data, shown in figure 5.2. V_{out} was positive in the hole transport regime, negative in the electron transport regime, and zero at the Dirac point. In both regimes, $|V_{out}|$ had maximum value at a gate voltage close to the Dirac point and decreased for gate voltages further away from the Dirac point. $|V_{out}|$ increased with increasing V_{in}.

The symmetric part of V_{out} [figure 5.1(b)] and V_{out} showed similar gate and bias dependences. The symmetric part was antisymmetric with respect to the gate voltage. Electron and hole efficiencies (plotted in the inset) depended linearly on V_{in}. For this sample, the efficiencies approached 30% at V_{in}= 150 mV. For small input voltages, the rectification effect was too weak to be distinguished: $V_{out,sym}$ was nearly zero at all gate voltages for $V_{in} = 10$ mV. The odd part of V_{out}, shown in figure 5.1(c), gives a measure of how asymmetric the device is. For this sample, the degree of asymmetry was small, because in absolute values the odd part was small compared to V_{out}, especially in the electron transport regime. For all other samples, whether measured at room or LN_2 temperature, very similar $V_{out,sym}$ curves were obtained, even for substantially asymmetric devices (i.e. odd part comparable to V_{out} in absolute values). The dependences of V_{out} and $V_{out,sym}$ on input voltage are shown in figure 5.1(d). Both quantities were approximately zero if the gate voltage was at the Dirac point. For gate voltages in electron and hole regime, quasi-parabolic dependences were seen for low input voltages up to approximately $V_{in} = 100$ mV, and linear

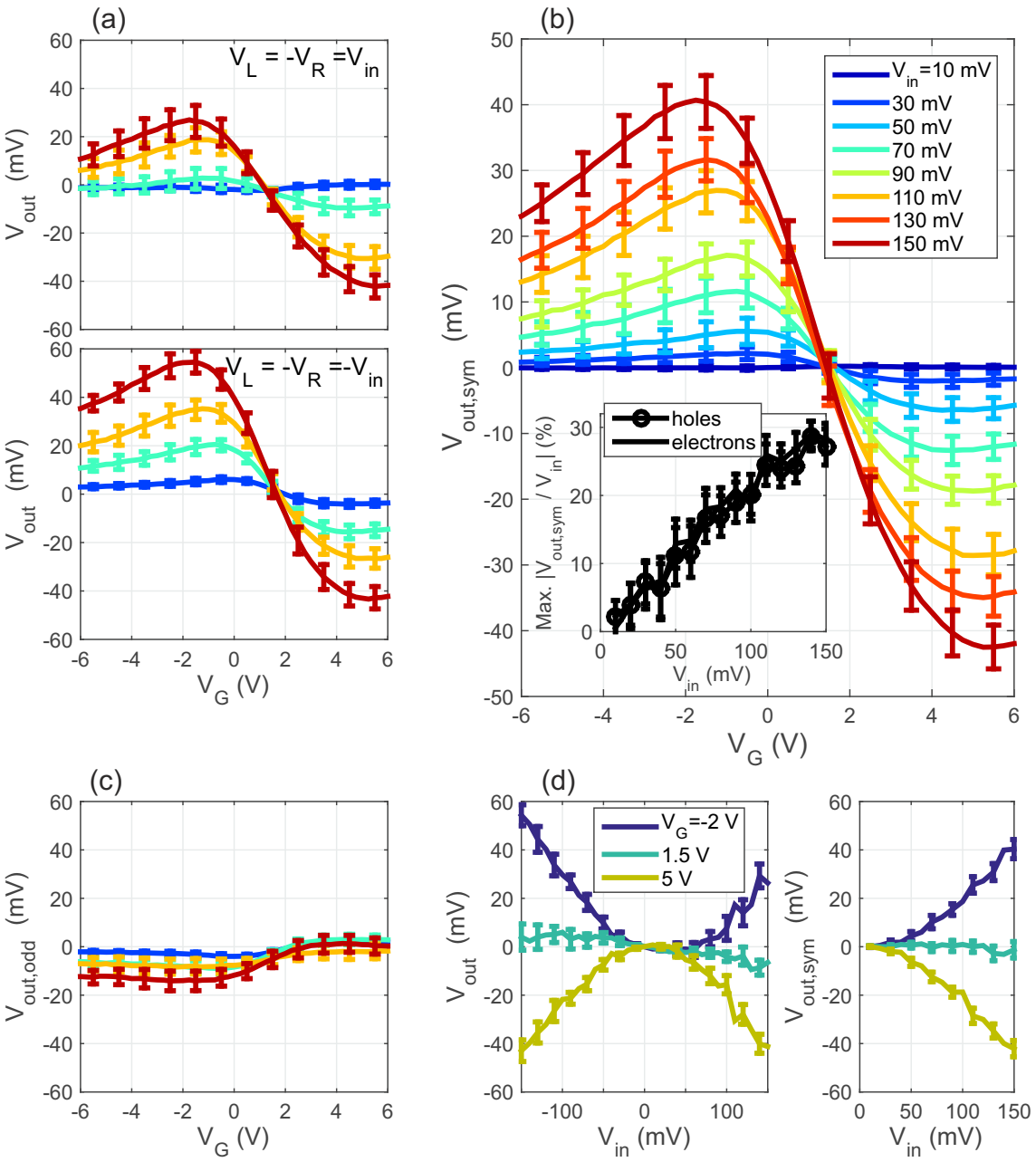

Figure 5.1: Room-temperature output-voltage data from sample F32 (measurement configuration shown in figure A.1). (a) V_{out} as function of back-gate voltage V_G for different input voltages V_{in} and both bias configurations [Same color code as in (b)]. (b) Symmetric part calculated from the raw data in (a). The inset shows the maximum efficiency as function of V_{in}. (c) Odd part calculated from the raw data in (a) [Same color code as in (b)]. (d) Replotting of data sets in (a) and (b) in order to show the dependence of V_{out} and $V_{out,sym}$ on V_{in} at certain V_G-values.

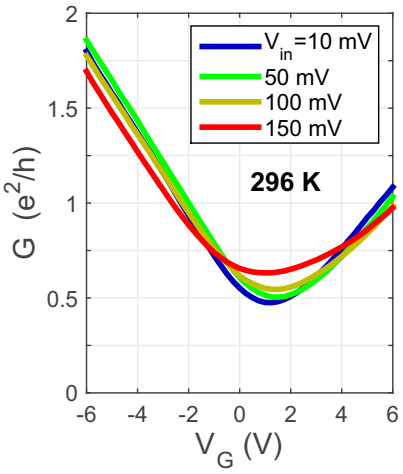

Figure 5.2: Room-temperature conductance data from sample F32 (measurement configuration shown in figure A.1) for $V_L = -V_R = V_{in}$.

dependences for higher input voltages.

Efficiencies from all our GTTJ samples are summarized in table 5.1. Highest efficiency, 40%, was reached at high input biases in two different samples (F32 and F48E4). Efficiencies at $V_{in} = 100$ mV are mostly 10-20% at room temperature, and below 10% at LN_2 temperature. Corresponding curvatures $|\alpha| = |V_{out,sym}/V_{in}^2|$ are shown as well. Such efficiencies are higher than most efficiencies reported in the literature (see table 2.1). They agree with the efficiency reported in ref. 27, and also roughly agree with higher efficiencies reported in refs. 29 and 34, considering enhancement because of 90-nm dielectric layer thickness in those devices (see section 3.2.4).

Sample (branch sizes $L = W$)	Efficiency (figure of merit)		
	Max. $\lvert V_{out,sym}/V_{in}\rvert$	Max. $\lvert V_{out,sym}/V_{in}\rvert$ at V_{in} =100 mV	Max. $\lvert\alpha\rvert$ (V^{-1})
F32 (100 nm)	30 % at V_{in}=150 mV 7 % at V_{in}=200 mV (87 K)	20 % 5 %	2 0.5
	40 % at V_{in}=400 mV 12 % at V_{in}=250 mV (87 K)	18 % 5%(h),9%(e)	1.8 $\sim$ 0.7
F48E4 (100 nm)	27% ; 22% ; 17% at V_{in}=250 mV 40% ; 33% ; 27% at V_{in}=500 mV	14% ; 10% ; 8% 15% ; 12% ; 9%	1.4-0.8 1.5-0.9
F33E2 (150 nm)	19%(h),13%(e) at V_{in}= 80 mV	$\sim$ 20 %	$\sim$ 2
F48E3 (200 nm)	21%(h),30%(e) ; 8%(h),13%(e) ; 8%(h),13%(e) at V_{in}=400 mV	$\sim$ 10% ; 5% ; 5%	$\sim$ 1-0.5
F33C1 (400 nm)	18 % at V_{in}=100 mV 5%(h),9%(e) at V_{in}=100 mV (87 K)	18 % 5%(h),9%(e)	1.8 $\sim$ 0.7

Table 5.1: Overview of highest GTTJ efficiencies and efficiencies at V_{in} =100 mV extracted from experimental data. All data measured at room temperature, except where noted differently. All samples had Y-shaped branches with 120° angles, on Si/SiO_2 (285 nm) substrate. Samples F48E4 and F48E3 were measured in three configurations. h ≡ holes, e ≡ electrons. $|\alpha| = |V_{out,sym}/V_{in}^2|$ for $V_{in} \leq 100$ mV (quasi-parabolic regime).

5.2 Comparison of LN_2-temperature and room-temperature data

In the following, the influence of chip temperature on the rectification property is discussed. Experimental rectification data from measurements at LN_2 temperature (i.e. chip temperature of 87 K) is compared to data at room temperature.

LN_2-temperature data is available for two samples of constriction sizes 100 and 400 nm. The rectification-measurement raw data is presented in figures A.5, A.9, and A.28. Rectification behavior at LN_2 temperature showed the same basic features as the behavior at room temperature described in the previous section. However, noticeable differences with respect to room-temperature data are wiggles in the output-voltage curves and a decreased efficiency.

At LN_2 temperature, output-voltage curves of the 100-nm sample showed reproducible wiggles at input voltages of the order of 100 mV and below. In figure 5.3(a), such features can be distinguished in the curves up to input voltages of about 140 mV. Wiggles are also seen for the 2^{nd} thermal cycle of this sample [figure A.9(b)] for $V_{in} = 50$ mV, then disappear at larger input voltages. In contrast, no wiggles can be distinguished in the data from the 400-nm sample at input biases below 100 mV [figure 5.3(b)]. Electron-hole puddles are a possible origin of the wiggles. For the 100-nm device the constriction size is comparable to the typical size of these puddles [85–87], leading to distortions of the output voltage. The constriction size of the 400-nm device exceeds the puddle size, leading to averaging of the potential disorder. The energy scale at which the wiggles were observed, 100 meV, corre-

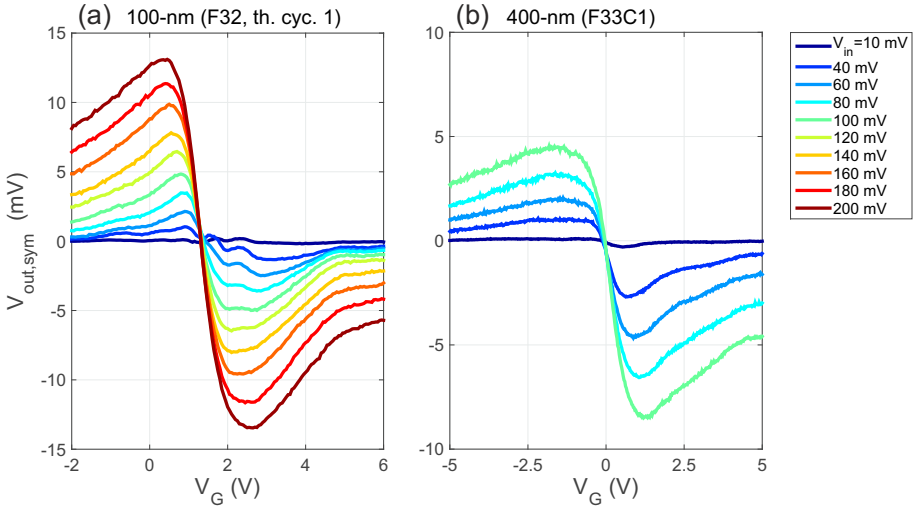

Figure 5.3: LN_2-temperature output-voltage curves (a) from 100-nm sample (F32, thermal cycle 1) and (b) from 400-nm sample (F33C1).

sponds to the typical magnitude of potential disorder in graphene on SiO_2 [104]. Thus, electron-hole puddles are the likely origin of the wiggles. From an application viewpoint, the potential disorder hinders proper usage of GTTJs on SiO_2 as rectification devices at LN_2 temperature and at input voltages below 100 mV.

The rectification efficiency observed at LN_2 temperature is lower than at room temperature. Output-voltage curves at both temperatures are compared for largest V_{in}-values in figure 5.4(a)-(c), showing the decrease in efficiency with deceasing temperature for both samples. Output-voltage curves for $V_{in} = 100$ mV from those samples are shown in figure 5.5. Comparable electrical behavior and efficiencies are observed. Thus, no noticeable effect from geometry is found between the 100-nm and 400-nm samples.

In the next step, experimental data is compared to field-effect simulations. Those simulations were made as described in chapter 3. The temperatures used in the simulations were $T = 296$ K and 87 K, corresponding to the experimental values. Parameters for the SiO_2 layer were $\epsilon = 3.9$ and $d = 285$ nm. An upper bound for the efficiency was calculated. For this purpose, simulations were made with zero potential disorder and a carrier mobility $\mu = 10{,}000$ cm^2/Vs (high-end for graphene on SiO_2 [94]), because decreasing potential disorder and increasing charge carrier mobility increases efficiency (see sections 3.2.5 and 3.2.2). We varied the input voltage V_{in} from 0 up to 500 mV.

The experimental results at room temperature cannot be explained by the field effect, as experimental efficiencies were substantially higher than simulated ones. This discrepancy in efficiency is seen in figure 5.5(a): experimental curves reach efficiency of 15-20% at $V_{in} = 100$ mV, whereas for simulations the efficiency is an order of magnitude smaller. At larger biases, an order of magnitude difference is also observed: an efficiency of almost 40% was measured for $V_{in} = 400$ mV in experiments [figure 5.4(b)], compared to $\approx 4\%$ in simulations [figure 5.6(b)]. The experimental results at LN_2 temperature can be partly understood by the simulation results. For $V_{in} = 100$ mV [figure 5.5(b)] as well as for $V_{in} = 400$ mV [figures 5.4(b) and 5.6(b)] experimental and simulated efficiencies roughly agree with each other. However, the simulated output voltage is an upper bound, such that a

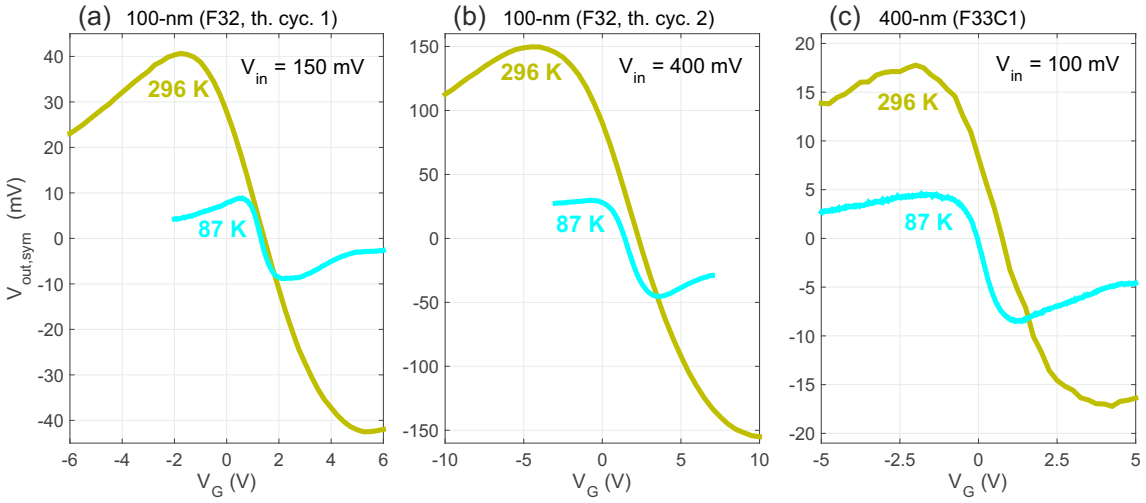

Figure 5.4: Comparison of output-voltage curves from measurements at room and LN_2 temperature. (a,b) Data for largest input voltage from 100-nm sample (F32, thermal cycles 1 and 2) and (c) from 400-nm sample (F33C1).

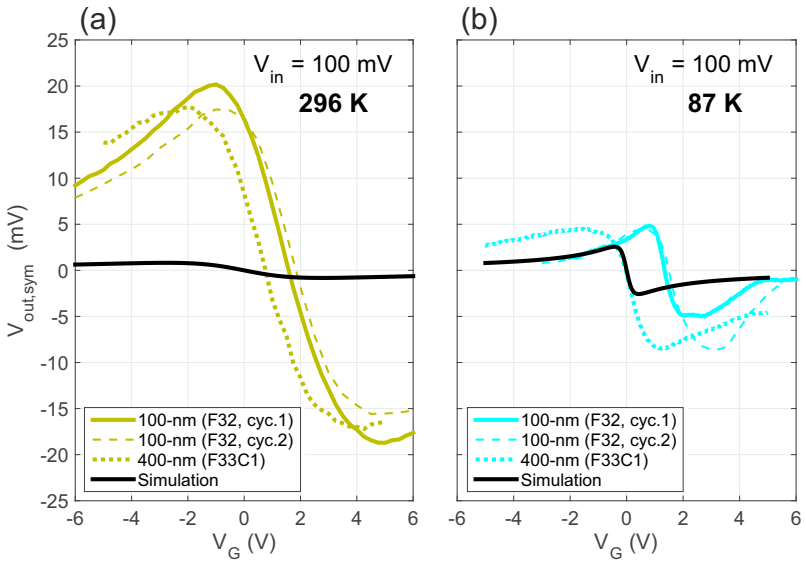

Figure 5.5: Comparison of output-voltage curves from measurements and FEM simulations for V_{in} =100 mV at (a) room temperature and (b) LN_2 temperature. Experimental data stems from 100-nm sample (F32, thermal cycle 1 and 2) and from 400-nm sample (F33C1).

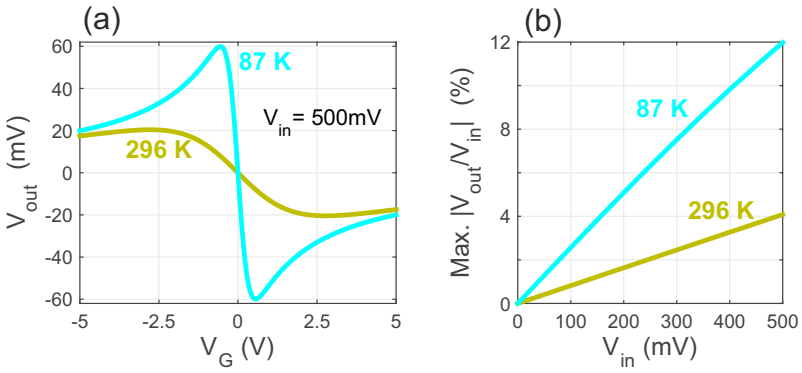

Figure 5.6: FEM-simulated output-voltage curves at room and LN_2 temperatures for high input voltages up to $V_{in} = 500$ mV. Refer to chapter 3 for details of the simulations. (a) V_{out} as function of gate voltage for $V_{in} = 500$ mV. (b) Efficiency as function of V_{in}. Efficiency increased with decreasing temperature.

lower efficiency is expected in realistic devices. Thus, also at LN_2 temperature a discrepancy between simulations and experiments could be stated. Simulations and experiments agree in the observation that the extrema of the output-voltage curves were closer together in gate voltage at LN_2 temperature than at room temperature.

To conclude, we found experimentally that the rectification efficiency was higher at room than at LN_2 temperature. Strikingly, this is contrary to the results from our field-effect simulations. These findings indicate that the rectification observed in our experiments is caused by other effects. In the next section, thermoelectric effects due to Joule heating are discussed as a possible cause.

5.3 Joule heating and thermal voltages

In this section, our experimental findings are analyzed in a picture incorporating Joule heating (self-heating) and thermal voltages. The output-voltage signal is interpreted as thermal voltage (or is thought to have large contribution from a thermal voltage), caused by thermal gradients in the TTJ due to Joule heating. Two major indications led us to this assumption. First, the thermal-voltage response to temperature gradients, the Seebeck coefficient, grows with temperature and is thus in agreement with higher efficiency at room temperature than at LN_2 temperature. Secondly, the Seebeck coefficient in graphene [114–116] and the output voltage from our experiments show very similar gate-voltage dependence. In the following, we argue that effects due to Joule heating are substantial in our measurements, estimate temperature rise in the devices, and compare output-voltage curves to calculated thermal voltages.

5.3.1 Thermal voltages in GTTJs

In order to get useful rectification efficiencies out of our GTTJ devices, we needed to operate them at biases of the order of 100 mV and larger. At such biases, large current densities and large electric fields built up in the constrictions. FEM calculations showed that in a TTJ geometry with $L = W = 100$ nm an average electric field above 1 V/µm is created in the constriction channel for $V_{in} = 500$ mV. In our experiments, high current densities of several hundred µA/µm were typically reached, and 1 mA/µm in one case.

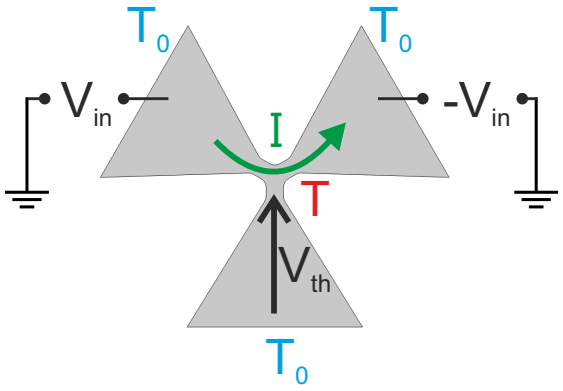

Figure 5.7: Sketch of a TTJ with push-pull bias configuration, current I, chip temperature T_0 at electrical contacts, Joule-heating induced temperature $T > T_0$ in the constrictions, and thermal voltage V_{th} in the floating terminal. The direction of V_{th} depends on temperature gradient and the sign of the Seebeck coefficient.

As mentioned in previous chapters, current densities above a few mA/µm are reported to lead to breakdown of graphene constrictions or ribbons [78,79]. Thus, Joule heating of the constrictions can be expected, and in the following we discuss how it could affect output voltages.

Formation of a Joule-heating induced thermal voltage in the TTJ is shown schematically in figure 5.7. We assume that due to a high current I the constrictions in the TTJ center heat up significantly (temperature T) above the chip temperature T_0. The electrical contacts are thermal anchors for the graphene system, such that the temperature at the contacts is assumed equal to T_0. Due to the temperature difference between the TTJ center and the contact used to probe the output voltage, a thermal voltage V_{th} builds up between those regions. The rectification effect due to the field effect is neglected and thus the voltage in the TTJ center is assumed to be zero. This is justified because simulations in the previous section are calculated for zero disorder, whereas in a realistic device the rectification effect is suppressed due to potential disorder. Thus, under this assumption the measured output voltage is V_{th}. In spite of a temperature difference between the TTJ center and the biased terminals, no thermal voltage builds up in those terminals because the voltages are fixed (four-point measurement configuration).

The Seebeck coefficient S (also called thermoelectric power or thermopower) is defined in linear-response approximation as the voltage difference due to a temperature gradient across a conductive sample: $S = -dV/dT$ [116]. For metals at low temperatures ($k_B T \ll E_F$), S is given in the Boltzmann picture by the Mott-formula:

$$S_{Mott} = -\frac{\pi^2 k_B^2 T}{3e} \frac{G'(E)}{G(E)}\bigg|_{E=E_F}, \tag{5.1}$$

where T is temperature, G conductance, E energy, and E_F Fermi energy. This relation was used successfully to explain experimentally determined thermopower in graphene [114,115]. The graphene thermopower can be tuned from negative to positive by Fermi-energy (gate-voltage) tuning. The Mott-formula remains largely accurate up to room temperature [114–116]. We used it to calculate an estimate of the Seebeck coefficient of our samples. Conductance curves at low bias (< 100 mV) were used in order to stay in the linear regime (conductance roughly equal to differential conductance) and so that T remains close to chip temperature. Furthermore, a relationship between gate voltage and Fermi energy is needed to calculate S_{Mott}. For this we took into account the shift in chemical potential due to charge carrier redistribution at finite temperatures [see equation (3.3)]. For simplicity, we calculated S_{Mott} assuming constant temperatures T =296 K and 87 K, respectively. Figure

5.8(a) shows calculated Seebeck coefficients at both temperatures. Conductance data at $V_{in} = 10$ mV was used for the room-temperature curve. For the LN_2-temperature curve, conductance data at $V_{in} = 50$ mV was used because less wiggles from potential disorder were seen in the curve (curves at lower biases were similar, showing more wiggles). S_{Mott} shows gate-voltage dependence reminiscent of output-voltage curves. The low-temperature curve is smaller in magnitude than the room-temperature curve by a factor ~ 3, corresponding to the temperature ratio $296/87 \approx 3$. The calculated Seebeck coefficient is in agreement with literature results [114–116].

The thermal voltage V_{th} depicted in figure 5.7 is obtained by integration over temperature:

$$V_{th}(T) = -\int_{T}^{T_0} S(T')dT', \tag{5.2}$$

where T is the temperature in the TTJ center and T_0 the chip temperature. Using the Mott-formula (5.1), we obtain

$$V_{th}(T) = -\frac{\pi^2 k_B^2}{3e}\frac{G'(E)}{G(E)}\bigg|_{E=E_F}\frac{1}{2}\left(T^2 - T_0^2\right). \tag{5.3}$$

Calculated thermal voltages are compared to measured output voltages for $V_{in} = 100$ mV in figure 5.8(b). At room temperature, V_{th} matches $V_{out,sym}$ fairly well using $\Delta T \equiv T - T_0 = 100$ K ($T_0 = 296$ K). At LN_2 temperature, $\Delta T \equiv T - T_0 = 60$ K ($T_0 = 87$ K) is needed in order to match the experimental data. The question arises whether such temperature differences are realistic. To find an answer to this, we consulted literature reports linking Joule-heating induced temperature rise to dissipated power density in graphene FETs.

Several groups have investigated the relationship between temperature rise and dissipated electric power in graphene FETs on Si/SiO_2 at room temperature [117–121], allowing us to estimate the temperatures reached in our experiments. On the other hand, for temperatures other than room temperature no literature for temperature-rise estimation is available. The data sets from the aforementioned publications are summarized in figure 5.9. In all of them, Raman spectroscopy (2D-peak shift, intensity ratio of Stokes and anti-Stokes G peaks, G-peak shift) was used to measure the graphene lattice temperature. Some groups complemented Raman data with infrared-emission spectra, from which the electron temperature is determined. Charge carriers and phonons are assumed to be in thermal equilibrium. The power density is defined as total dissipated power per graphene surface area. Joule heat in graphene supported on SiO_2 is widely thought to be dissipated vertically through the bulk SiO_2 [117–124] (the silicon substrate is considered a thermal reservoir at chip temperature). Only a small part is carried away by metal contacts [117,121], despite the high thermal conductivity of graphene. All devices from which data is plotted in figure 5.9 have SiO_2 layer thicknesses comparable to the SiO_2 thickness of our devices, yielding comparable thermal resistance. Hence, the relationship between temperature rise and power density remains valid for our experiments. The radiation heat loss is a negligible portion of the total power dissipation: estimating for $T = 1000$ K (corresponding to a total power dissipation of the order of mW/µm^2) with the Stefan-Boltzmann law gives a loss of $\varepsilon\sigma T^4 \approx$ nW/µm^2 (ε=2.3% is the emissivity of graphene, assumed equal to the graphene absorption [74], and $\sigma \approx 5.7 \cdot 10^{-8}$ W K^{-4}m^{-2} the Stefan-Boltzmann constant).

The data sets in figure 5.9 show large spread in temperature. All data sets follow roughly a linear relationship within a deviation of $\sim \pm 200$ K, except for the data from Chae *et*

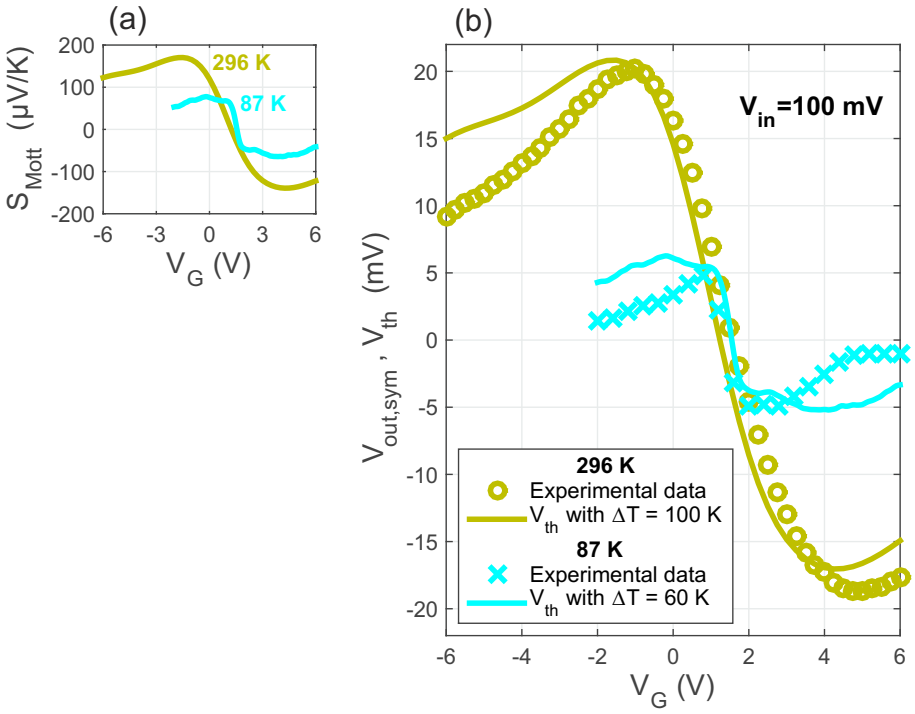

Figure 5.8: (a) Seebeck coefficient calculated with the Mott-formula (5.1) from conductance data of 100-nm sample (F32, thermal cycle 1). (b) Comparison of experimental $V_{out,sym}$ data for V_{in}=100 mV to calculated thermal voltages V_{th} using equation (5.3).

al. [118] (green stars) which follows roughly a square-root relationship and shows temperature values several hundred K larger than in the other data sets. We explain this discrepancy by pointing at two major differences between measurements from this publication and the rest. First, the device from ref. 118 was a (rectangular) constriction of width 0.6 µm, whereas all other devices (also rectangular) are large-area graphene sheets wider than 1.5 µm. In the constriction, edge roughness might affect electronic transport more than in wider devices [94,97], resulting in an enhanced temperature rise. Secondly, data in ref. 118 was obtained from a four-point measurement, whereas data in all other references was obtained from two-terminal devices. As contact resistances are of the same order of magnitude as graphene channel resistances ($\sim$ kΩ), power dissipated at the contacts is appreciable and might therefore be responsible for underestimating the temperature rise. From all devices presented in the figure, the device from ref. 118 is most similar to our devices, in terms of channel sizes and by the fact that it was measured in a four-point configuration. For this reason we compare our data to the data set from this reference.

In the following paragraphs, calculation of power dissipation is explained in detail. Dissipated electric power P was calculated as the product of applied voltage and current: $P = 2V_{in}I$. It showed the same gate-voltage dependence as I with a minimum at the Dirac point. The surface area over which the power is dissipated is influenced by two factors: geometric design and lateral heat spreading. Our geometric design with constrictions implies that both electric field and current density have largest absolute values in the two constrictions through which current flows. Power density is therefore largest in those constrictions, leading to the formation of a hot spot. Thus, in our devices, electric power was dissipated mainly over the area of two constrictions. Next, we check that lateral

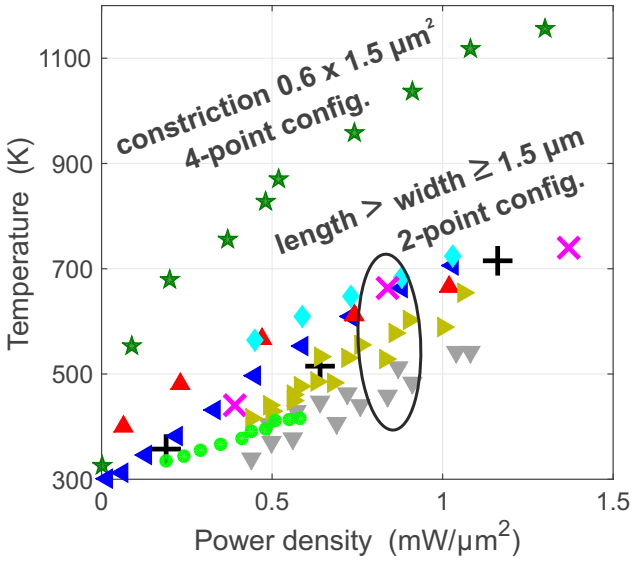

Figure 5.9: Temperature as function of power density (power per graphene surface area), digitized from references cited below. 0.6 x 1.5 µm^2 device [118]: stars (Raman G-peak Stokes/anti-Stokes ratio). 1.5 x 2.7 µm^2 device [117]: plus signs (Raman 2D-peak shift). 1.6 x 3.6 µm^2 device [120]: crosses (Raman G-peak Stokes/anti-Stokes ratio). 1.5 x 4.2 µm^2 device [119]: left-pointing triangles (Raman 2D-peak shift), upward-pointing triangles (Raman G-peak Stokes/anti-Stokes ratio), diamonds (infrared emission). 4 x 7 µm^2 device [121]: downward-pointing triangles (Raman 2D-peak shift), right-pointing triangles (Raman G-peak shift), dots (scanning thermal microscopy).

heat diffusion from the hot spot to the metal contacts was negligible at room temperature. Modeling temperature diffusion along graphene on SiO_2 with the one-dimensional heat equation [125] gives a characteristic length scale L_h of temperature decrease away from a heat source. It is given by $L_h = \sqrt{\kappa_{gr} t_{gr} t_{SiO_2} / \kappa_{SiO_2}} \approx 200$ nm, where $\kappa_{gr} \approx 600$ WK^{-1}m^{-1} is the thermal conductivity of graphene on SiO_2 [126], $t_{gr} \approx 0.35$ nm the graphene thickness, t_{SiO_2} =285 nm and $\kappa_{SiO_2} \approx 1.4$ WK^{-1}m^{-1} [117, 122] the SiO_2 layer thickness and thermal conductivity. Thus, heat spread up to roughly 200 nm away from the TTJ branches (heat source). As this distance is smaller than the separation of the branches to the contacts, no excess heat escaped from the electrical contacts. In conclusion, power dissipation in our devices was tightly localized to the device centers.

Considering the above, we estimated the power dissipation area A by adding the area of two constrictions ($2 \cdot L \cdot W$) to the area spanned by lateral heat diffusion on both sides of the two constrictions ($\sim 4 \cdot 0.2$ µm $\cdot W$). For the 400-nm device this gives $A = 0.64$ µm^2. Likewise, the areas of the other devices were estimated. For the 100-nm devices the hot spot has an area $A \approx 0.1$ µm^2.

With above power-dissipation areas, power densities can be calculated. For our 100-nm device (F32), total power dissipation for $V_{in} = 100$ mV was around 2 µW (at gate voltage of maximum efficiency), yielding a power density ~ 0.02 mW/µm^2. According to the data set from ref. 118 (figure 5.9, close-up in figure 5.11), such power density corresponds to a temperature rise of $\Delta T \approx 100$ K. Thus, the output voltage at room temperature shown in figure 5.8(b) can indeed be explained by thermal voltages. The highest power dissipation in our experiments was reached in the measurement shown in figures A.14 to A.16 for a

different 100-nm sample (F48E4). Current exceeded 100 µA and power reached 0.1 mW, resulting in a current density of 1 mA/µm and a power density of 1 mW/µm^2. This corresponds to a temperature of $\sim$ 1000 K [118] and explains the strong broadening of the conductance-curve minimum (figure A.14).

To summarize, Joule heating is relevant in our devices since they were operated in a regime of high current density and large electric fields. Thermal voltages can be expected to be a major contributing factor to the output voltages. Encouraged by this first result, we calculate below in more detail temperature rise and thermal voltages at room and LN_2 temperatures in order to verify if a quantitative analysis holds up to the experimental results.

5.3.2 Temperature-rise estimation

Changes in conductance curves for various input voltages are used to determine the temperature in the graphene constrictions (thermal equilibrium of lattice and charge carriers is assumed). First, trends of conductance curves are presented and explained. Next, a model for temperature estimation is put forward. Finally, extracted temperatures are compared to literature data.

Conductance as function of gate voltage showed two noticeable trends for increasing input voltage: increase of the conductance minimum (and associated: broadening of the minimum of the conductance curve around the Dirac point) and decreasing slope at gate voltages away from the Dirac point (i.e. decrease in carrier mobility). Those trends are common to the conductance data of all our samples at both room and LN_2 temperature. As an example, LN_2-temperature conductance data from a 100-nm sample (F32) and the corresponding I–V curves are plotted in figure 5.10. I–V curves were not measured directly, but are extracted from $I(V_G)$-curves, which were measured at several input voltages. The conductance used in this work is the linear conductance $G = I/V_{bias} = I/(2V_{in})$. In general, the linear conductance is not equivalent to the differential conductance dI/dV_{bias} due to non-linearities in the high-bias regime. However, we found that using the differential conductance (calculated from I–V curves) instead of G for the analysis in this section leads to very similar results. Thus, for simplicity, the linear conductance was used.
The increase of conductance minimum is seen in figure 5.10(b) as super-linear current, and the decreasing slope as (onset of) current saturation. In the next paragraph, the physical mechanisms behind these trends are explained.

High electric fields lead to drift-velocity saturation (current saturation) and self-heating. According to literature reports, such conditions are obtained in graphene FETs on Si/SiO_2 at fields of around 1 V/µm [122–124], with saturation tendencies appearing already at lower fields. The physics behind this behavior is significant inelastic phonon scattering. This process reduces the charge carrier velocity and dissipates energy from the carriers to the graphene lattice, causing temperature rise of the lattice (Joule heating). The lattice heating in turn causes the electron temperature to rise as well. In the same way, high current densities cause Joule heating. The main scattering channels are not intrinsic graphene phonons [such as optical phonons at the K point ($\sim$ 150 meV) and Γ point ($\sim$ 200 meV)], but surface optical phonons of SiO_2 ($\sim$ 60 meV) [124]. We attribute the super-linear behavior around the Dirac point to Joule-heating induced increase of thermally excited charge carriers [see equation (3.2)]. Likewise, the broadening of the conductance curve minimum around the Dirac point is thermal broadening.

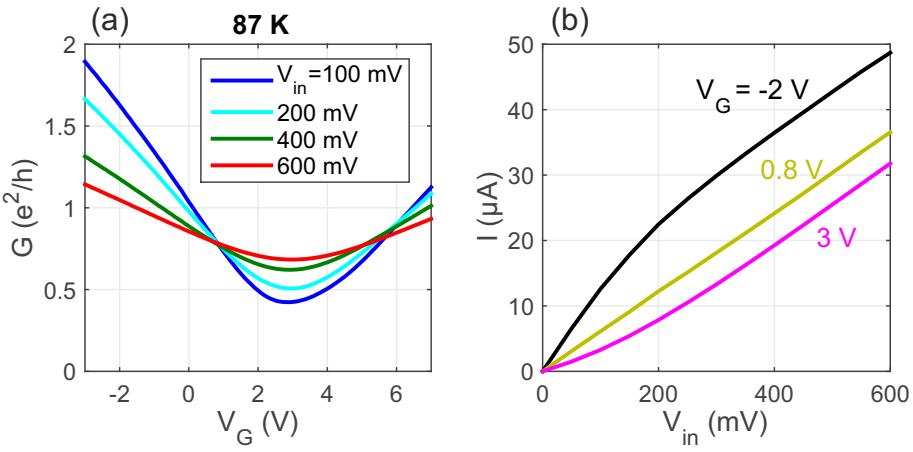

Figure 5.10: (a) Conductance as function of gate voltage for several V_{in} at 87 K (100-nm sample, F32, cyc. 2, figure A.8). (b) I–V curves (current I as function of V_{in}) from the same data set.

For completeness, we mention that electrostatics (field effect) is another mechanism for non-linear current behavior in graphene FETs [98, 127]. As seen from simulation results in chapter 3, at high-bias operation a substantial charge carrier density gradient is obtained between source and drain. A distinctive feature of I–V curves in such a regime is the appearance of a kink, caused by transition from one charge carrier type in the graphene channel to two separate channel regions for holes and electrons. In relation to this, a local hot spot forms in the graphene channel, corresponding to highest local electric field and lowest local carrier density [119, 121, 125, 128]. Generally, such behavior is achieved more easily in graphene FETs with relatively thin gate dielectrics and high dielectric constants (e.g. 15 nm HfO_2 [127]). According to our simulations, electrostatic effects are negligible in our experiments.

In summary, high-bias effects are important for our experiments because we applied fields ~ 1 V/μm. Consequently, the current saturation tendency in the I–V characteristics can be explained by phonon scattering and self-heating.

In the following, a method for estimating temperature from conductance data is presented. The conductance at the Dirac point, G_{Dirac}, was assumed to be proportional to the total carrier density at the Dirac point:

$$G_{Dirac}(T) \propto 2n_{th}(T) + n^*,$$

where T is the temperature, $n_{th}(T) \propto T^2$ the thermal carrier density given by (3.2), and n^* the residual carrier density due to potential disorder. Furthermore, conductance was assumed to be proportional to carrier mobility $\mu(T)$ (equal for electrons and holes). The conductance curve for lowest input voltage (negligible Joule heating) was associated with chip temperature T_0. By rearranging the ratio $G_{Dirac}(T)/G_{Dirac}(T_0)$, the temperature T was obtained:

$$T = \frac{\hbar \nu_F}{k_B} \sqrt{\frac{3}{\pi} \left[\frac{G_{Dirac}(T)\mu(T_0)}{G_{Dirac}(T_0)\mu(T)} \left(2n_{th}(T_0) + n^*\right) - n^* \right]}. \tag{5.4}$$

$\mu(T)$ and $\mu(T_0)$ were obtained from linear fits to the conductance curves for gate voltages away from the Dirac point, taking the average of electron and hole mobility. n^* was

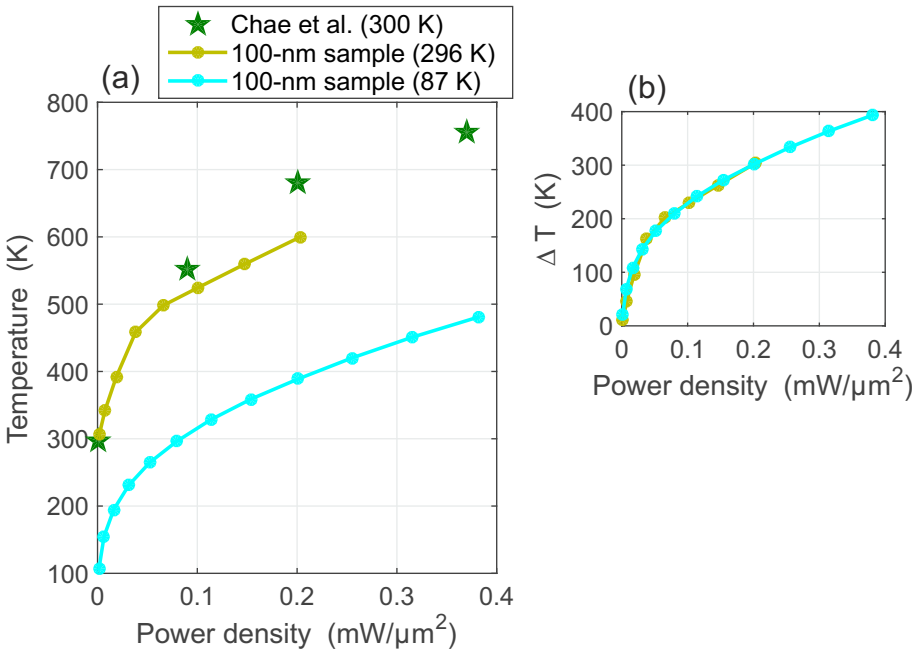

Figure 5.11: (a) Temperature as function of power density (power per graphene surface area) of 100-nm sample (F32, thermal cycle 2), temperature extracted with (5.4) from conductance data presented in figures A.6 (room temperature) and A.8 (LN_2 temperature). Star markers: data from Chae *et al.* [118]. (b) Data from (a) shown for ΔT.

estimated from a log-log-plot of conductance vs. carrier density by the method from ref. 129, using the conductance curve for smallest input voltage. $n^* \approx 10^{11}$ cm^{-2} was found. With equation (5.4), a rough temperature estimate could thus be obtained from conductance data.

Temperatures extracted with (5.4) from room-temperature conductance data show good agreement with temperatures predicted by literature. Figure 5.11(a) shows a comparison between data from the 100-nm sample and from Chae *et al.* [118]. Panel (b) shows that temperature rise is comparable at room and LN_2 temperature, pointing to similar Joule-heating mechanisms at both temperatures. In figure 5.12, the temperature rise in the 100-nm and 400-nm devices are compared. Similar temperature rises are seen for both devices.

5.3.3 Thermal-voltage estimation

Based on temperature-rise and Seebeck-coefficient estimates obtained from the previous sections, thermal voltages were calculated for devices of different constriction sizes and compared to output voltages. If rectification is caused by thermo-voltages due to Joule heating, contrast in rectification efficiency is expected by comparing efficiencies at different temperatures and efficiencies for different constriction sizes. This is because different temperatures yield different Seebeck-coefficient values, and different geometries yield different Joule heating. In this section, data from a 100-nm and 400-nm device are compared for room and LN_2 temperature in order to show this contrast. However, our geometric design yields only low contrast, as will be explained first. In a second step, thermal voltages are calculated and compared.

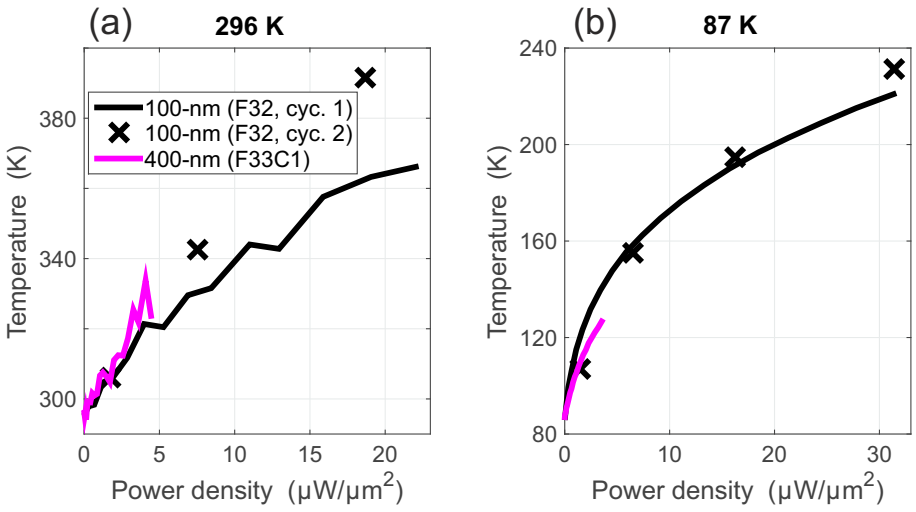

Figure 5.12: Temperature as function of power density of 100-nm sample (F32) and 400-nm sample (F33C1) at (a) room temperature and (b) LN_2 temperature.

We first explain why in our devices efficiency is similar for different geometries. For the same input voltage, power dissipation P is larger in the wide-constriction device than in the narrow-constriction device, due to larger conductance. FEM calculations show that decreasing W in our geometries from 400 to 100 nm changes the 'aspect ratio' $a = G/\sigma$ from 0.3 to 0.16. Power density is given by $P/A = GV_{bias}^2/A = a\sigma V_{bias}^2/A$, where A is the power dissipation area. From figure 5.11 we see that roughly $\Delta T \propto \sqrt{P/A}$ is valid at both room and LN_2 temperature. The thermal voltage is roughly $V_{th,max} \approx S_{max}\Delta T$, and thus given by:

$$V_{th,max} \propto S_{max}\sqrt{\frac{a\sigma V_{in}^2}{A}}. \tag{5.5}$$

S_{max} is a thermal parameter, whereas a and A are geometric parameters. The Seebeck coefficient is not affected by geometry, as can be seen from the Mott-formula (5.1) where aspect ratio cancels out. Indeed, Seebeck coefficients calculated from data sets of different samples turned out to be comparable.

Comparing efficiencies (at same input bias) of the same device but for two different chip temperatures, an efficiency ratio of $V_{th,max,T_1}/V_{th,max,T_2} = S_{max}(T_1)/S_{max}(T_2) = T_1/T_2$ is obtained. In particular, $V_{th,max,296K}/V_{th,max,87K} \approx 3$. This result shows that for the same device, efficiency at the same input voltage grows with increasing temperature. Comparing efficiencies (at same input bias) of devices with different geometries but for the same chip temperatures, an efficiency ratio of $V_{th,max,1}/V_{th,max,2} = \sqrt{\frac{a_1}{a_2}\frac{A_2}{A_1}}$ is obtained. In particular, $V_{th,max,100nm}/V_{th,max,400nm} \approx 2$. Thus, roughly similar efficiencies are expected in those devices, even though constriction widths differ by factor 4. As a consequence, similar efficiencies are expected for all of our samples. This is indeed in agreement with our experimental results (see table 5.1). In conclusion, the comparable rectification efficiencies observed in our devices (with different TTJ geometries) can be explained in the Joule-heating scenario.

In the next step, efficiencies from a 100-nm (F32, thermal cycle 1) and 400-nm device (F33C1), at both room and LN_2 temperature, are compared to calculated thermal volt-

ages. An input-voltage range below 100 mV is considered, because already for $V_{in} = 100$ mV high efficiencies ($\approx 20\%$) were seen in both devices. First, the temperature T was calculated from conductance minima [equation (5.4)], giving T as function of power density for these devices. In order to compare efficiencies of calculated thermal voltages ($V_{th,max}$) to efficiencies of output voltages, the power density at gate voltages of maximum $V_{out,sym}$ was used for calculation of temperature rise. Temperature-dependence of the Seebeck coefficient is given by the Mott-formula (5.1): $S \propto T$. Maximum thermal voltage, $V_{th,max}$, was calculated using (5.2):

$$V_{th,max}(T) = -\int_{T}^{T_0} S_{max}(T')dT' = \frac{S_{max}(T_0)}{2T_0}\left(T^2 - T_0^2\right).$$

S_{max} was calculated from conductance curves and was given for both devices as $S_{max}(T_0) \approx 150$ µV/K (at $T_0 = 296$ K) and $S_{max}(T_0) \approx 50$ µV/K (at $T_0 = 87$ K). Thermal-voltage efficiency is given by $V_{th,max}/V_{in}$.

Rectification efficiencies at room temperature are compared to efficiencies of $V_{th,max}$ for each device in figure 5.13(a) and (b). At $V_{in} = 100$ mV, a temperature rise of ≈ 40 K was estimated from conductance curves for both devices, contributing to roughly half of the output voltage. The temperature rise estimated from literature is about twice this value and roughly covers the output voltage. The relatively large discrepancy between T-values from conductances curves and literature is due to relatively large discrepancies at low power density [see figures 5.11 and 5.12]. In figure 5.13(c) and (d), rectification efficiencies at LN_2 temperature are compared to efficiencies of $V_{th,max}$ for each device. At $V_{in} = 100$ mV, a temperature rise of ≈ 70 K was estimated from conductance curves for both devices, covering the output voltage for the 100-nm device and most of the output voltage for the 400-nm device.

Overall, figure 5.13 shows that efficiencies were higher at room temperature than at LN_2 temperature by a factor ≈ 3, which agrees with the ratio $V_{th,max,296K}/V_{th,max,87K}$ from above. The figure also shows that devices with different constriction sizes had comparable efficiencies at both temperatures, whereas according to above estimate $V_{th,max,100nm}$ / $V_{th,max,400nm} \approx 2$ could be expected. Nevertheless, we conclude that thermal voltages can explain experimental rectification efficiencies in both devices; they contribute substantially to the efficiencies.

In the next step, thermal voltages are estimated for high power densities (high temperatures, $T \gg 300$ K). According to theoretical literature, the graphene Seebeck coefficient saturates at high temperatures ($k_B T > E_F$) [116]. For typical $E_F \sim 50$ meV, this corresponds to $T \sim 600$ K. For screened charged impurities (dominant scattering mechanism in graphene on SiO_2), the temperature-independent (maximum) saturation value for the Seebeck coefficient is $S_{sat} \sim 200$ µV/K. Using this value, the thermal voltage $V_{th,max}$ was estimated from (5.2) as follows:

$$V_{th,max}(T) = -\int_{T}^{T_0} S_{max}(T')dT' = S_{sat}\left(T - T_0\right).$$

For sample F32 (thermal cycle 2, room temperature) at $V_{in} = 400$ mV, dissipated power at maximum efficiency was ≈ 30 µW, giving a power density ≈ 0.3 mW/µm^2. According to figure 5.9, T was then ≈ 700 K. Finally, the thermal voltage $V_{th,max} \approx 80$ mV. This value

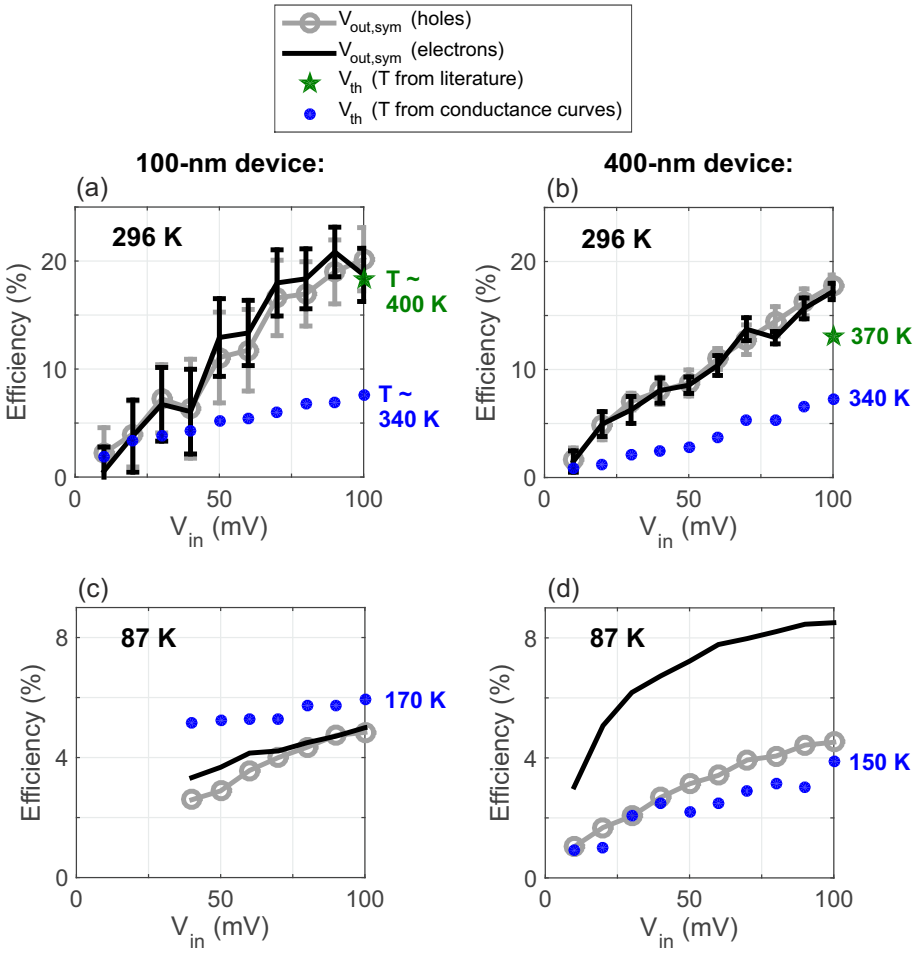

Figure 5.13: Comparison of rectification efficiencies, from $V_{out,sym}$, with efficiencies of estimated thermal voltages, $V_{th,max}$, for (a,c) 100-nm sample (F32, thermal cycle 1) and (b,d) 400-nm sample (F33C1), at room and LN_2 temperature. $V_{th,max}$ was calculated using temperature estimates from literature and conductance curves. Temperature values are indicated for $V_{in} = 100$ mV.

is only half the maximum $V_{out,sym} = 150$ mV. For sample F48E4 at $V_{in} = 500$ mV, dissipated power at maximum efficiency was ≈ 60 µW, giving a power density ≈ 0.6 mW/µm^2. T was then 900 K and $V_{th,max} \approx 120$ mV. Again, this value is only half the maximum $V_{out,sym} = 200$ mV. These results could imply that S_{sat} is larger than 200 µV/K, or that the temperatures in the constrictions were actually higher than estimated from conductance curves. Thus, although saturation tendency of the rectification efficiency can be understood by Seebeck-coefficient saturation, the calculated thermal voltages do not fully explain the measured output voltages.

In the following paragraph, we comment on how non-equilibrium hot charge carriers might influence electrical properties of our devices. Whereas at room temperature and higher temperatures graphene lattice and electrons are thermalized [119, 120], some groups [130–134] found evidence of hot carriers in graphene over a lattice-temperature range from 4 to 300 K. The carriers were generated by photo-excitation or Joule heating and showed cooling lengths of the order of micrometers. Sierra *et al.* detected thermoelectric voltage signals several µm away from the current injection point (acting as heat source) in graphene on

SiO_2 [134]. The power dependence of the thermal voltages proved the presence (absence) of hot carriers at temperatures below 100 K (at room temperature). Thus, it might be possible that in our LN_2-temperature experiments hot carriers, while still at an elevated temperature, reached the probing electrical contact, where they thermalized to chip temperature. The value of the thermal voltage is not affected by the presence of hot charge carriers because it is defined by the difference in temperature (T and T_0). However, hot charge carriers might transfer heat to the contacts, which reduces the temperature rise generated by Joule heating. To summarize, the argumentation above suggest that at LN_2 temperatures Joule heating might be less efficient than at room temperature because of hot charge carrier diffusion to the contacts.

5.3.4 Conclusions

Joule-heating induced thermal voltages were proposed as mechanism behind the rectification effect in GTTJs. Due to high power dissipation (~ 0.1 mW/µm^2), Joule heating was shown to be relevant for our devices. The heating was shown to be localized to the submicron TTJ constrictions because heat dissipates mainly vertically for graphene on SiO_2. Temperature rise (several hundered K) was estimated from conductance curves and was comparable to temperature rises reported in the literature. Thermal-voltage estimates gave considerable contributions to the output voltages. Gate-voltage and temperature dependences of the latter could be explained by the corresponding dependences of the graphene Seebeck coefficient. We linked comparable efficiencies of samples with different constriction sizes to comparable heat generation due to geometric design. Finally, efficiency saturation could be explained by saturation of the graphene Seebeck coefficient.

5.3.5 Outlook

For proving that rectification can be induced by Joule-heating, we propose the following experiment, where electrical and thermal effects on rectification are separated. Devices must be designed to give large differences in power density at the same bias voltage. This can be achieved using T-junctions with rectangular terminals of same width W (e.g. 300 nm) but different total channel lengths L (e.g. short $L_s = 1$ µm and long $L_l = 10$ µm). The central branch, used as non-invasive voltage probe (channel width 100 nm), can be kept the same in all devices. As conductance depends on geometry (for rectangular sheets the conductance $G = \frac{W}{L}\sigma$, with conductivity σ), operating both devices at the same bias gives smaller current and power dissipation P in the long device than in the short one: $P_l/P_s = L_s/L_l < 1$. For power density the influence of geometry is even more pronounced, because the area $A = L \cdot W$ of the long device is larger than the area of the short device: $\frac{P_l/A_l}{P_s/A_s} = \left(\frac{L_s}{L_l}\right)^2 < 1$. Thus, self-heating induced rectification effects should be seen more prominently in the short device. Using the estimate (5.5), the expected thermal voltage ratio is $V_{th,l}/V_{th,s} \approx L_s/L_l < 1$. The contribution due to electrostatic rectification is expected to be the same for both devices.

5.4 Effect of device symmetry on rectification

In this section, influence of device symmetry on rectification efficiency is shown. For this, we turn to data from an asymmetric sample (F48E4), presented in figures A.12 and A.13. This data is summarized in figure 5.14. Sample F48E4 was measured in three measurement configurations, which allows comparing efficiencies for different 'degrees' of asymmetry.

Figure 5.14(a-c) shows that V_{out} depended strongly on measurement and bias configurations. For the measurement configuration in (a), V_{out}-curves for both bias configurations were very similar, and correspondingly the odd part, shown in (d), was negligible with respect to V_{out} (in absolute values). On the other hand, for the measurement configuration in (b), V_{out}-curves were larger than corresponding curves in (a) for $V_{in} > 0$ and smaller for $V_{in} < 0$ (in absolute values). For the measurement configuration in (c), the opposite was true. Odd parts in (e) and (f) were comparable to V_{out}-curves in those measurements (in absolute values). Symmetric parts of V_{out}-curves from (a) to (c) are shown in (g) to (i). $V_{out,sym}$-curves from the different configurations were comparable, but showed different efficiencies, plotted in (k). Efficiency was largest for case (a).

In order to interpret these asymmetric output characteristics, the individual terminal conductances G_L, G_R, and G_C were calculated (figure 5.15), using the relations (4.4) derived in section 4.2.4. They were thus calculated from conductance data [shown in figure A.11(a-c)] and $V_{out,odd}$-data [shown in figure 5.14(d-f)]. G_L and G_R calculated from the measurement in configuration $V_L = -V_R = V_{in}$ [figure 5.15(a)] are largely overlapping conductances at all V_{in} values, especially in the gate-voltage range from 0 to 15 V inside which the V_{out}-extrema were seen. In that case efficiency was largest. Panel (b) shows that G_R and G_C had dissimilarities: their Dirac points were apart by a few volts, and also their slopes in the hole transport regime were different. Panel (c) shows that also G_C and G_L had their Dirac points slightly apart. For the cases (b) and (c), efficiencies were smaller than in (a). Efficiency is thus influenced by device symmetry. Overall, the main source of asymmetry was the doping level in terminal C, which was closer to 0 V than the doping levels of the other terminals. The device asymmetry could be used for an alternative diode-like functionality, as can be seen in figure 5.14(j).

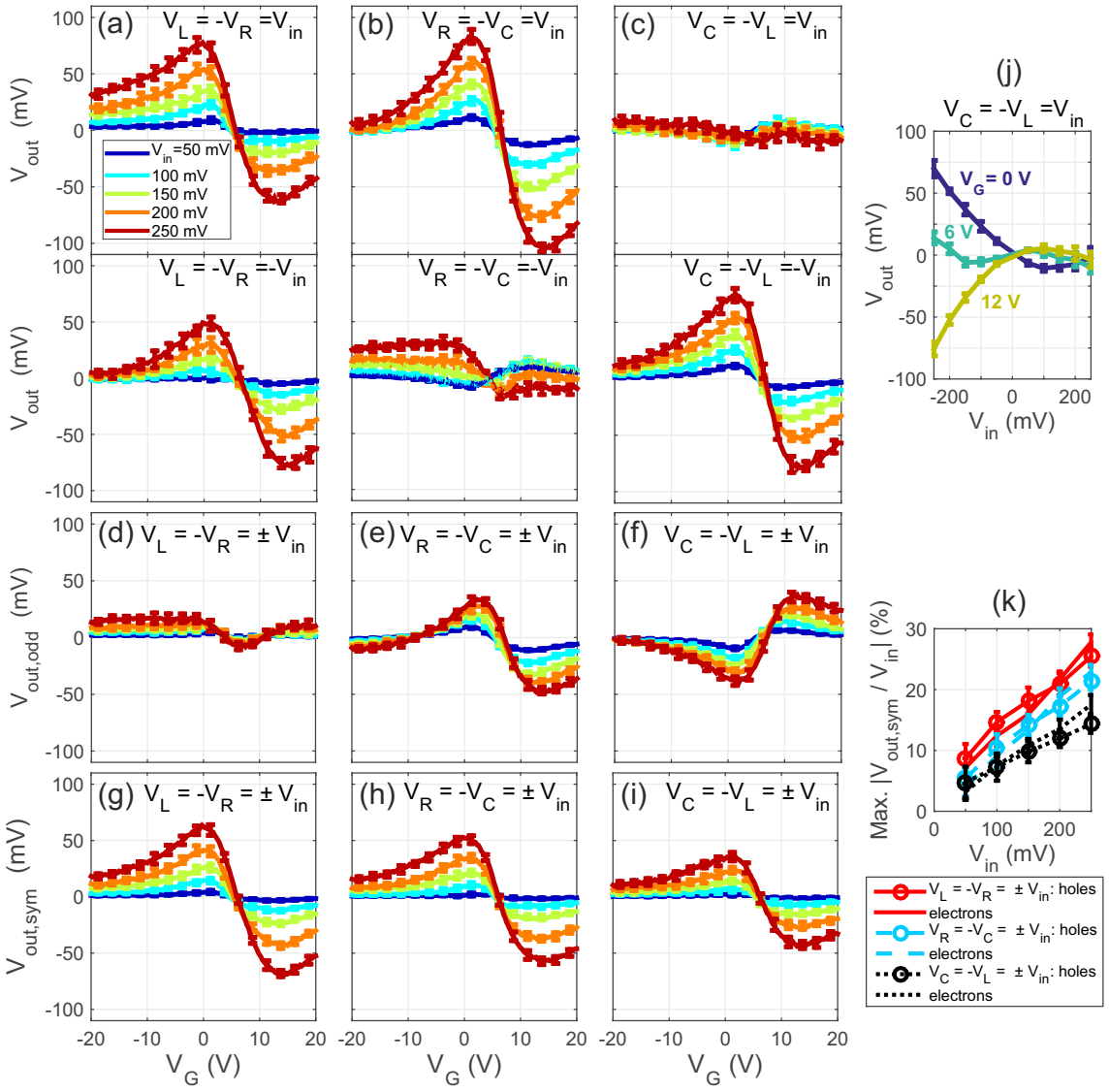

Figure 5.14: Room-temperature output-voltage data of 100-nm device (F48E4). (a-c) V_{out} as function of back-gate voltage V_G for different input voltages V_{in} and both bias configurations, respectively for each measurement configuration. (d-f) Corresponding odd parts. (g-i) Corresponding symmteric parts. Same color code for plots (a-i). (j) Replotting of data set in (c) in order to show the dependence of V_{out} on V_{in}. (k) Efficiencies as function of V_{in} for all measurement configurations.

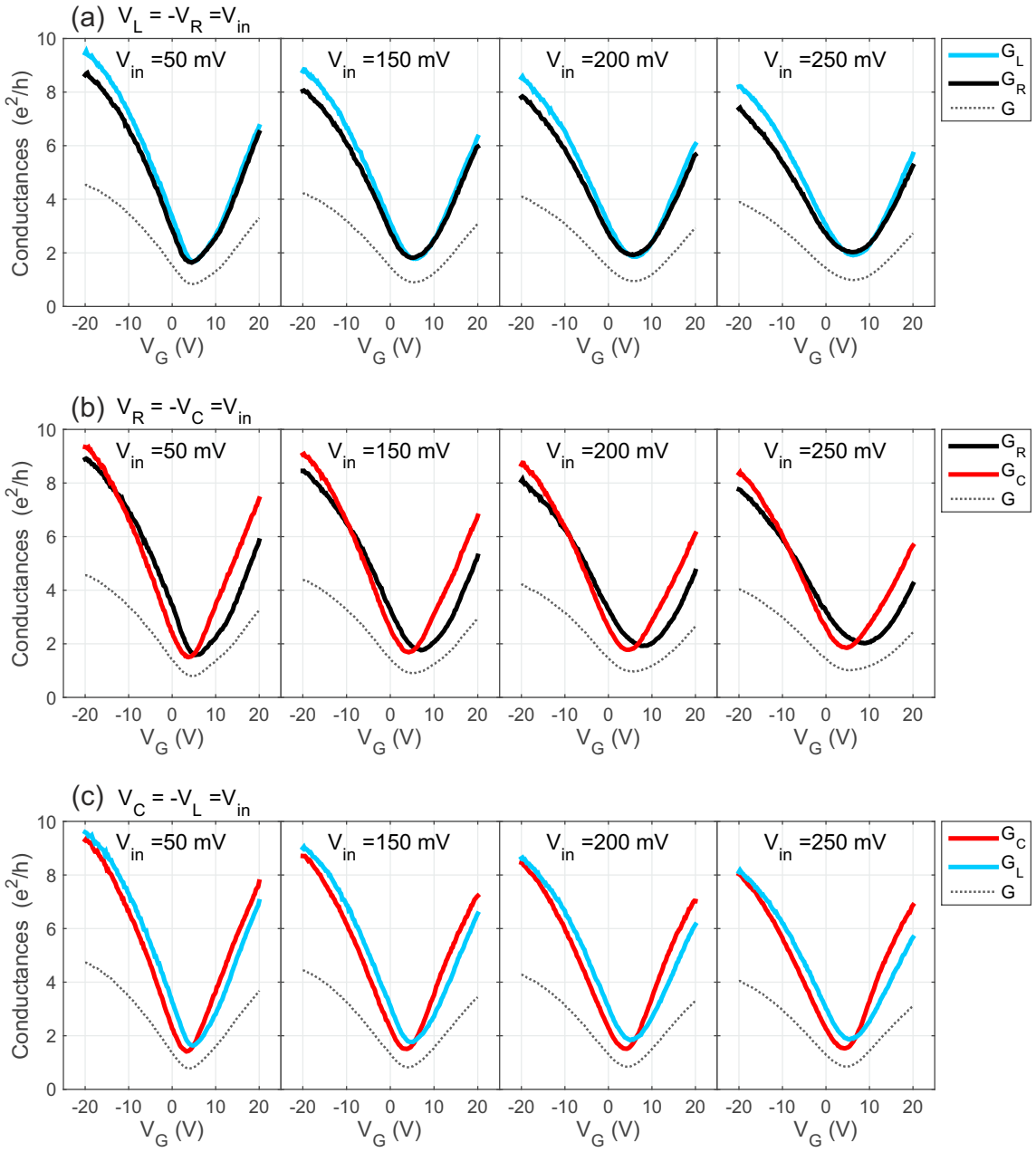

Figure 5.15: Terminal conductances G_L, G_R, and G_C of 100-nm device (F48E4) for measurement configurations where biases were applied to (a) terminals L and R, (b) terminals R and C, (c) terminals C and L.

Chapter 6

Conclusions and outlook

Although much effort has been invested in studies on graphene three-terminal nanojunctions, engineering and clear understanding of the rectification effect in those devices is still in its beginnings. This work was aimed to improve understanding of this effect with theoretical and experimental investigations. Main conclusions are summarized here, followed by an outlook.

In our simulations of diffusive GTTJ devices, the rectification effect is described as electrostatic effect. A conductivity gradient inside the graphene channel, caused by applied biases (input voltages) and the field effect, creates an asymmetric voltage drop inside the channel, resulting in rectified output voltage. A figure of merit is the rectification efficiency, defined as output voltage divided by input voltage. The simulations fit well to a substantial number of reported experimental results. Moreover, they provide engineering guidelines for efficiency enhancement, such as good graphene material quality and high capacitive gate coupling. Increasing temperature decreases efficiency. Potential disorder poses limitations on efficiency. Geometry dependence of efficiency enters via gate coupling and electric fringing fields. Changing parameter values over ranges realistically achievable in experiments can lead to strong efficiency enhancement (by factor ~ 20), but the overall efficiency stays below 50%. The simulations yield an intrinsic efficiency limitation of roughly 60% at temperatures relevant for application purposes. The reason why the saturation value remains conspicuously below 100% is the relatively high residual conductivity at the Dirac point. It limits the ability to modulate conductivity in graphene, which consequently limits rectification efficiency. For the very same reason, graphene is not suitable for digital FET applications.

In experiments, robust rectification behavior was demonstrated in GTTJs of different constriction sizes (100 to 400 nm) at 296 K and 87 K. Efficiencies at room temperature were typically between 10 to 20% at 100 mV input voltage, while corresponding values at 87 K were below 10%. Highest rectification efficiency from our experiments was $\sim 40\%$ at 400 mV input voltage, observed at room temperature. This value is higher than most efficiencies reported in the literature. Such high rectification efficiency might move GTTJs closer to applications. Moreover, asymmetry of TTJ junctions was seen to affect rectification efficiency.

While from our field-effect simulations efficiency enhancement was expected when cooling down the devices, it turned out to be opposite in experiments. This result suggests that mechanisms other than the field effect contribute to the measured rectification ef-

fect. At 87 K rectification efficiency can be partially explained by the field effect, but at room temperature a large discrepancy between field-effect simulations and experimental data was observed. Thus, at room temperature other mechanisms seem to contribute to the rectification. Joule-heating induced thermal voltages were identified here as a possible contributing mechanism. Such thermal mechanisms must be relevant, especially in high-bias regimes where high power dissipation densities ($\sim$ mW/µm^2) are reached. Joule heating offers a possible explanation for high efficiency at room temperature and comparatively low efficiency at LN_2 temperature. Temperature-rise estimates (several hundered K) are in agreement with values reported in the literature, and corresponding thermal-voltage estimates can partially explain the output voltages at room and LN_2 temperatures. The graphene Seebeck coefficient can explain gate-voltage and temperature dependences of the output voltages. Relatively weak geometry-dependence of efficiencies in our devices is consistent within this Joule-heating mechanism.

Below, directions for further research are proposed. The next logical step is to prove that Joule heating induces rectification. By proper geometric device design, resulting in large differences in power density, it is possible to separate electrical and thermal operation regimes. Measuring at several temperatures will further elucidate temperature-dependence of rectification mechanisms. A study combining electrical measurements with Raman spectroscopy, such that output voltage and lattice temperature are measured simultaneously, would be certainly revealing to this end.

The p-type-to-n-type tuning ability of graphene allows GTTJs to be used as adaptive logic gates [91]. The two types of rectification functionality (positive and negative) allow GTTJs to work as both AND gate (electron transport) and OR gate (hole transport). Furthermore, investigating high-frequency response of GTTJs is a promising route for device application. Ultra-high carrier mobility in combination with small device size might enable rectification functionality at THz frequencies.

Obviously, improving graphene quality in GTTJ rectifiers is a promising direction to go. This can be done by fabrication of GTTJs encapsulated between hBN, leading to clean graphene with enhanced electronic properties [76]. Due to lower potential disorder and higher carrier mobilities in such devices compared to graphene-on-SiO_2 devices, rectification efficiency is expected to be higher. Ballistic transport in those devices could lead to ultra-high operation speed.

Studies of voltage rectification should definitely be extended to other 2D materials [14–17]. Making use of semiconducting properties of transition-metal dichalcogenides (TMDs), high (and possibly perfect) rectification efficiencies can be envisioned for TMD-based TTJs. In FETs made from TMDs such as MoS_2 [135] and WSe_2 [136], conductivity pinch-off was demonstrated, and WSe_2-based FETs additionally showed both p-type and n-type conduction. On the other hand, those materials are not suited for high-frequency applications due to low mobilities of the order of 100 cm^2/Vs. However, a highly promising 2D material for both analogue and digital electronics is phosphorene (monolayer of black phosphorus). In encapsulated few-layer phosphorene, high room-temperature carrier mobility exceeding 1000 cm^2/Vs was demonstrated, as well as conductivity pinch-off and tunability from n-type to p-type [137]. GHz cutoff frequencies were reported for phosphorene FETs [138] — even on flexible substrate [139]. Based on those properties, 2D materials therefore show big potential as channel material for future TTJ rectifiers.

Appendix A

Rectification measurements on GTTJs

In this appendix chapter, all experimental raw data from rectification measurements made on GTTJ devices of different sizes are presented. All device were made from exfoliated graphene on Si/SiO_2 chips (285 nm thickness of dielectric layer) and were fabricated and measured as described in the chapter 4. For each sample figures showing conductance G and output voltage V_{out} as function of gate voltage and bias (input voltage) are presented. Either one or three measurement configurations are presented, depending on availability. Two devices were measured at LN_2 temperature. Data is discussed in chapter 5.

A.1 Data from 100-nm sample (F32)

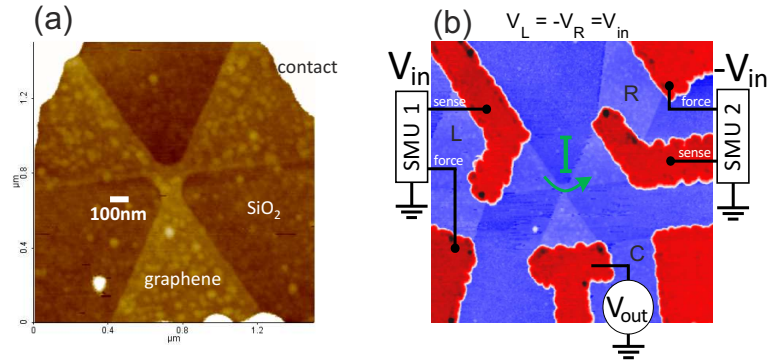

Figure A.1: Sample F32 with constriction sizes 100 nm. (a) 1.5x1.5 µm^2 AFM scan of the GTTJ. (b) Measurement configuration (4x4 µm^2 AFM scan). Terminals L, R, and C in pale blue and electrical contacts in red. Graphene connects each inner contact to an adjacent outer one. Push-pull bias $\pm V_{in}$ was applied to two terminals, generating a current I. SMU *sense* outputs were connected to inner contacts. V_{out} was probed with a multimeter at the remaining inner contact. The remaining outer contact was left open. A back-gate voltage was applied to the silicon substrate.

Thermal cycle 1

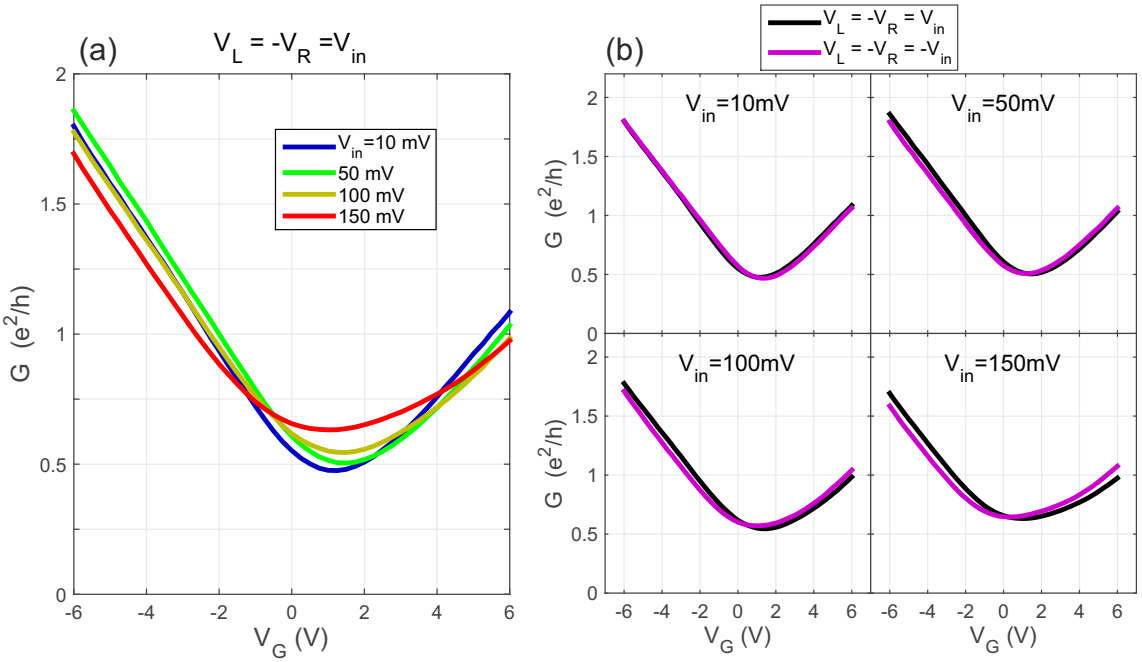

Figure A.2: Room-temperature conductance data from sample F32 (measurement configuration shown in figure A.1). (a) Conductance as function of back-gate voltage V_G for different input voltages V_{in}. (b) Conductance curves from (a) compared to curves from measurement at same V_{in} of opposite sign.

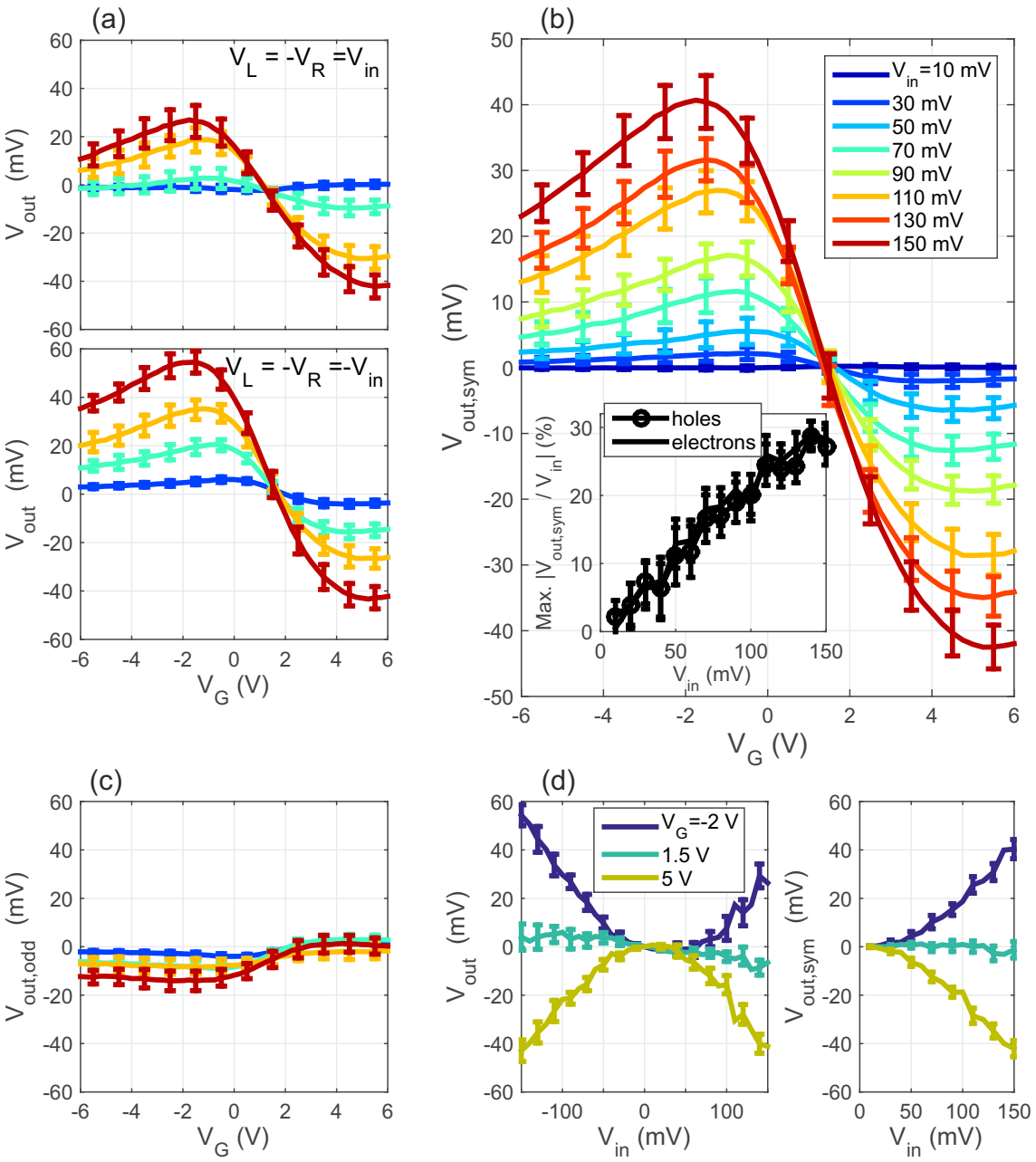

Figure A.3: Room-temperature output-voltage data from sample F32 (measurement configuration shown in figure A.1). (a) V_{out} as function of back-gate voltage V_G for different input voltages V_{in} and both bias configurations [Same color code as in (b)]. (b) Symmetric part calculated from the raw data in (a). The inset shows the maximum efficiency as function of V_{in}. (c) Odd part calculated from the raw data in (a) [Same color code as in (b)]. (d) Replotting of data sets in (a) and (b) in order to show the dependence of V_{out} and $V_{out,sym}$ on V_{in} at certain V_G-values.

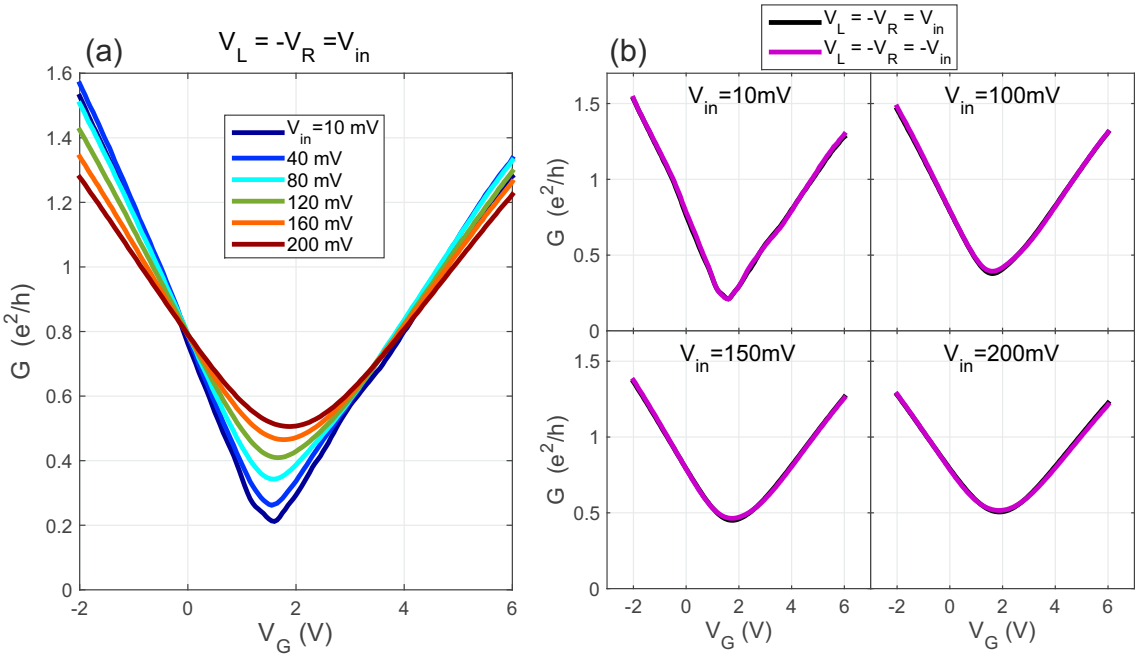

Figure A.4: LN_2-temperature conductance data from sample F32 (measurement configuration shown in figure A.1). (a) Conductance as function of back-gate voltage V_G for different input voltages V_{in}. (b) Conductance curves from (a) compared to curves from measurement at same V_{in} of opposite sign.

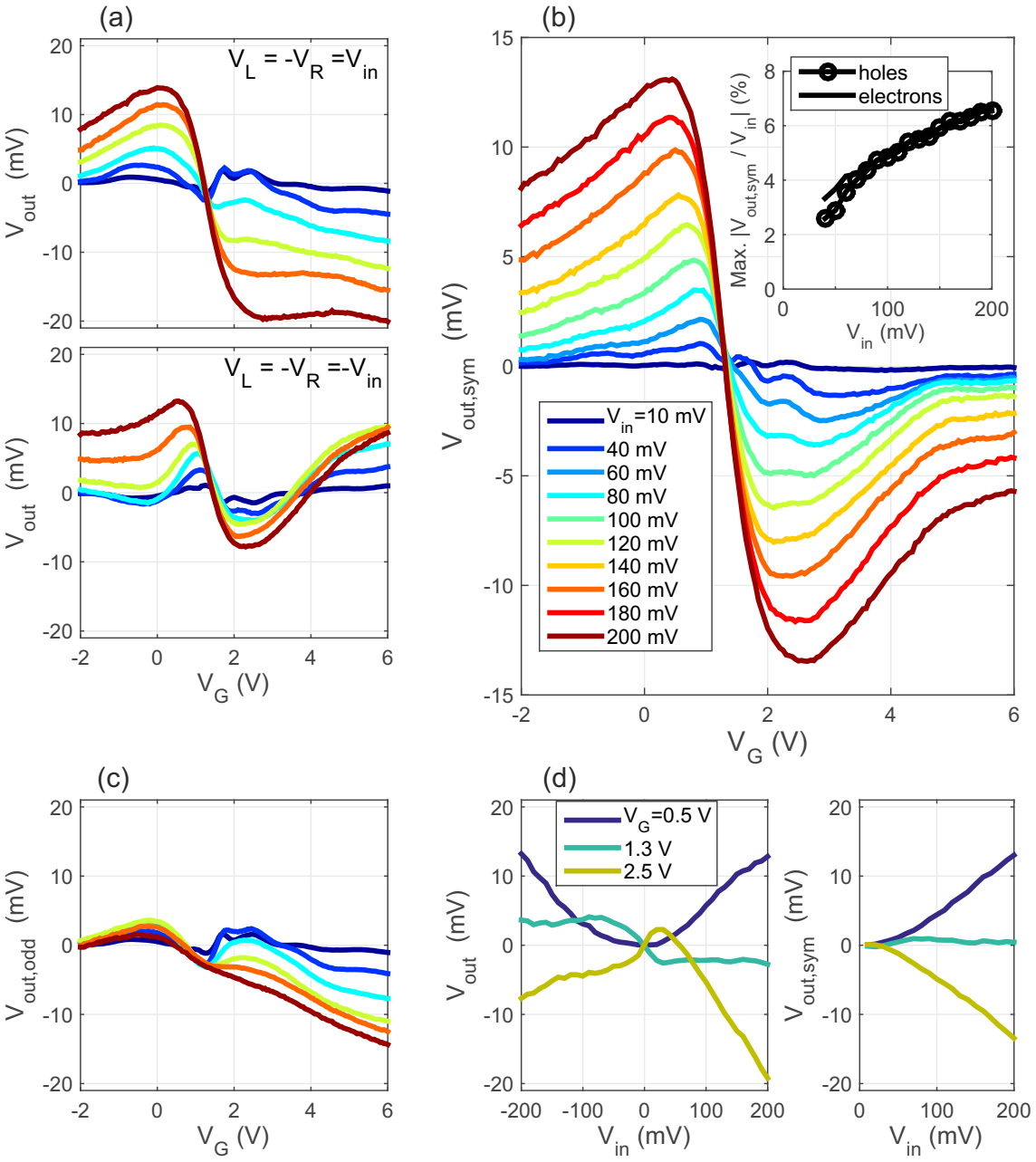

Figure A.5: LN_2-temperature output-voltage data from sample F32 (measurement configuration shown in figure A.1). (a) V_{out} as function of back-gate voltage V_G for different input voltages V_{in} and both bias configurations [Same color code as in (b)]. (b) Symmetric part calculated from the raw data in (a). The inset shows the maximum efficiency as function of V_{in}. (c) Odd part calculated from the raw data in (a) [Same color code as in (b)]. (d) Replotting of data sets in (a) and (b) in order to show the dependence of V_{out} and $V_{out,sym}$ on V_{in} at certain V_G-values.

Thermal cycle 2

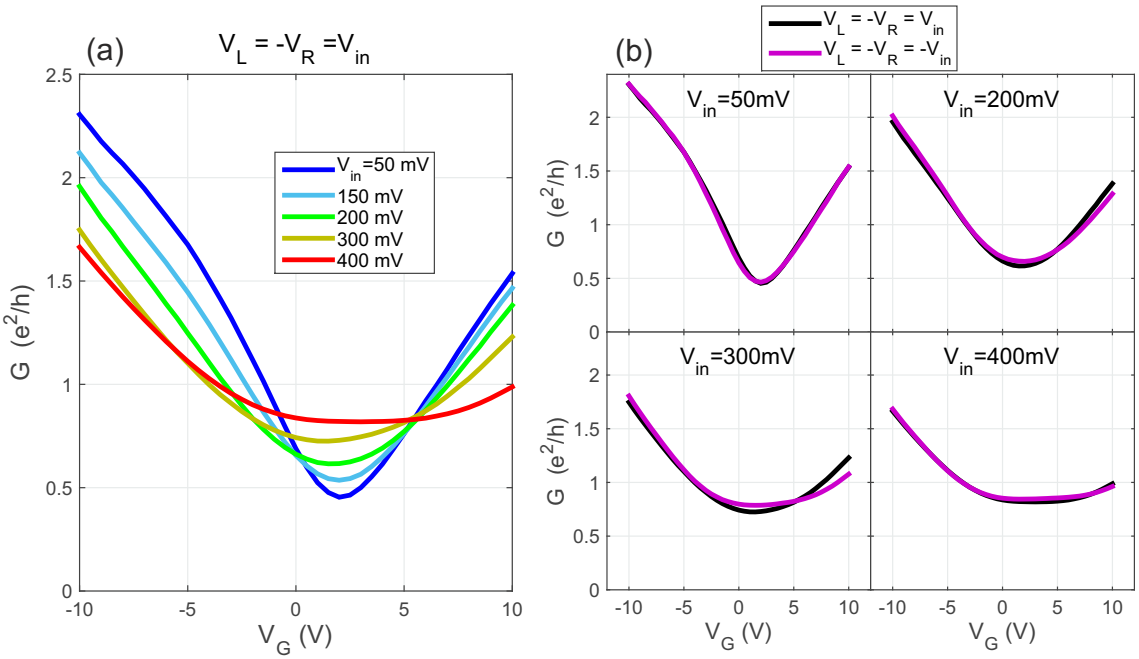

Figure A.6: Room-temperature conductance data from sample F32 (measurement configuration shown in figure A.1). (a) Conductance as function of back-gate voltage V_G for different input voltages V_{in}. (b) Conductance curves from (a) compared to curves from measurement at same V_{in} of opposite sign.

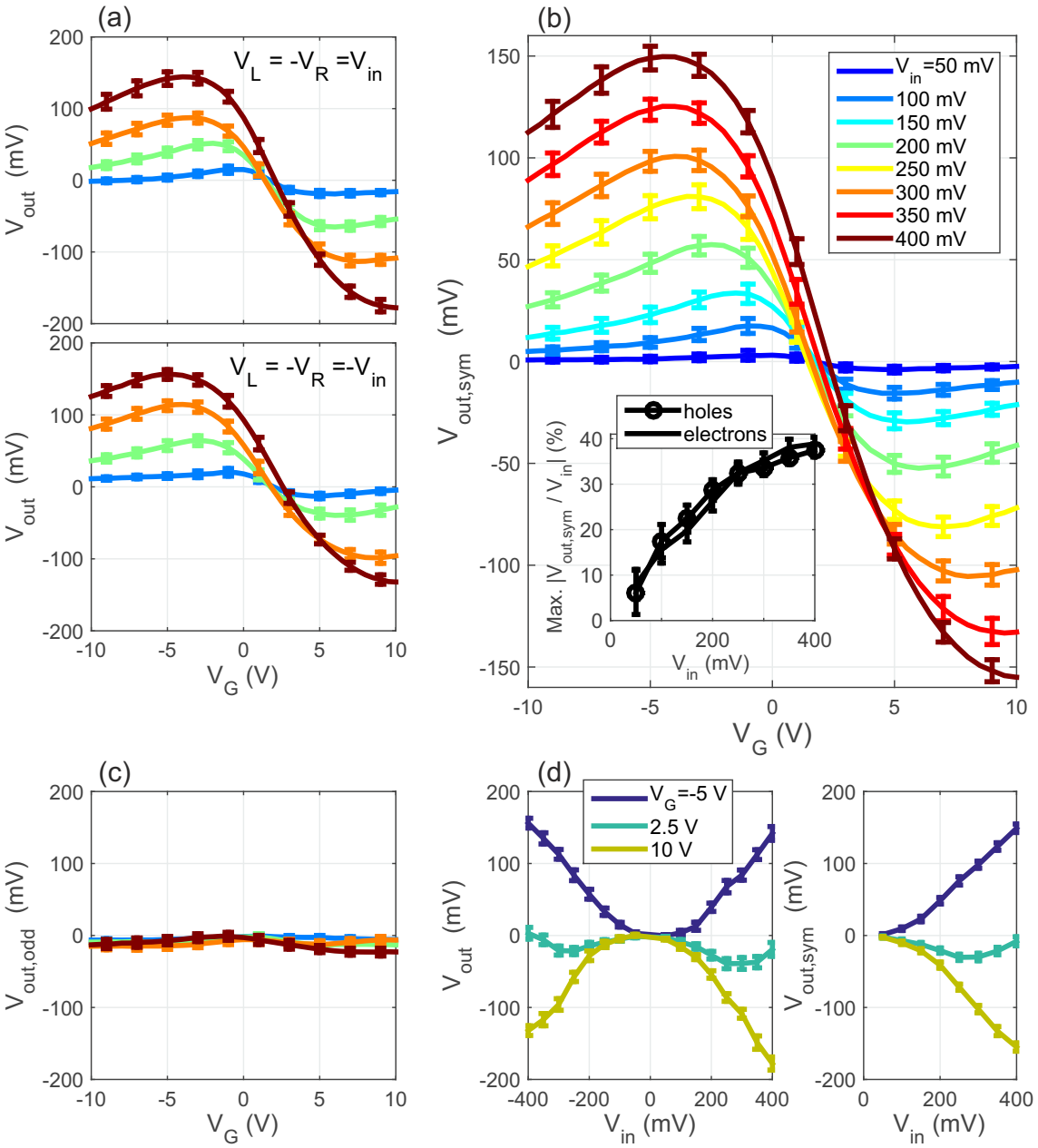

Figure A.7: Room-temperature output-voltage data from sample F32 (measurement configuration shown in figure A.1). (a) V_{out} as function of back-gate voltage V_G for different input voltages V_{in} and both bias configurations [Same color code as in (b)]. (b) Symmetric part calculated from the raw data in (a). The inset shows the maximum efficiency as function of V_{in}. (c) Odd part calculated from the raw data in (a) [Same color code as in (b)]. (d) Replotting of data sets in (a) and (b) in order to show the dependence of V_{out} and $V_{out,sym}$ on V_{in} at certain V_G-values.

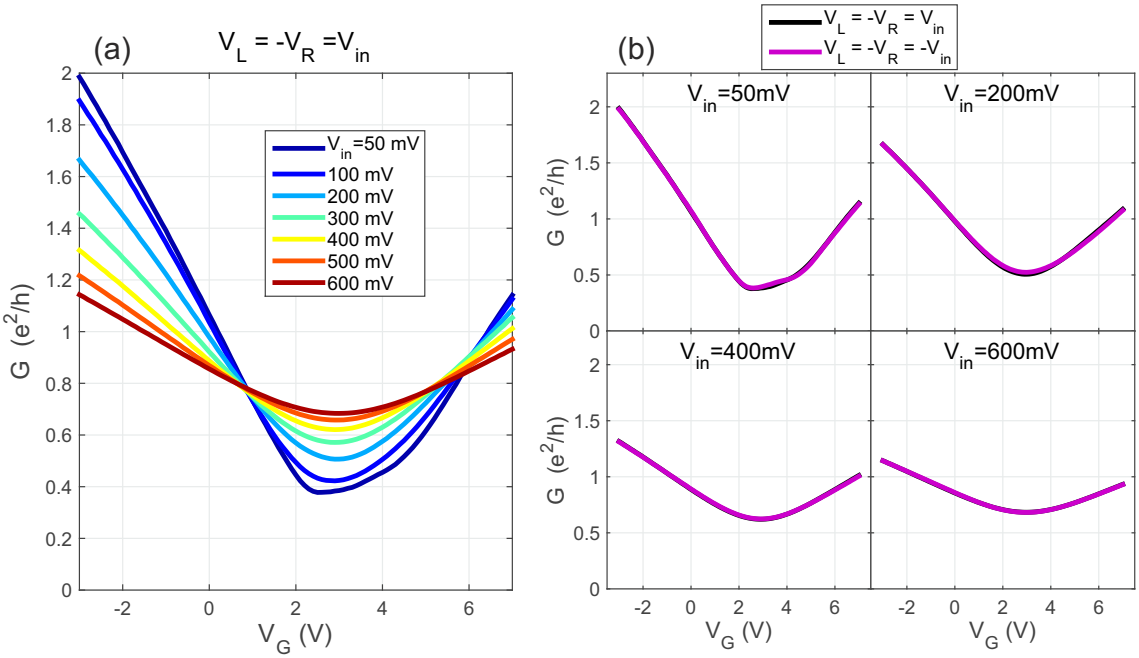

Figure A.8: LN_2-temperature conductance data from sample F32 (measurement configuration shown in figure A.1). (a) Conductance as function of back-gate voltage V_G for different input voltages V_{in}. (b) Conductance curves from (a) compared to curves from measurement at same V_{in} of opposite sign.

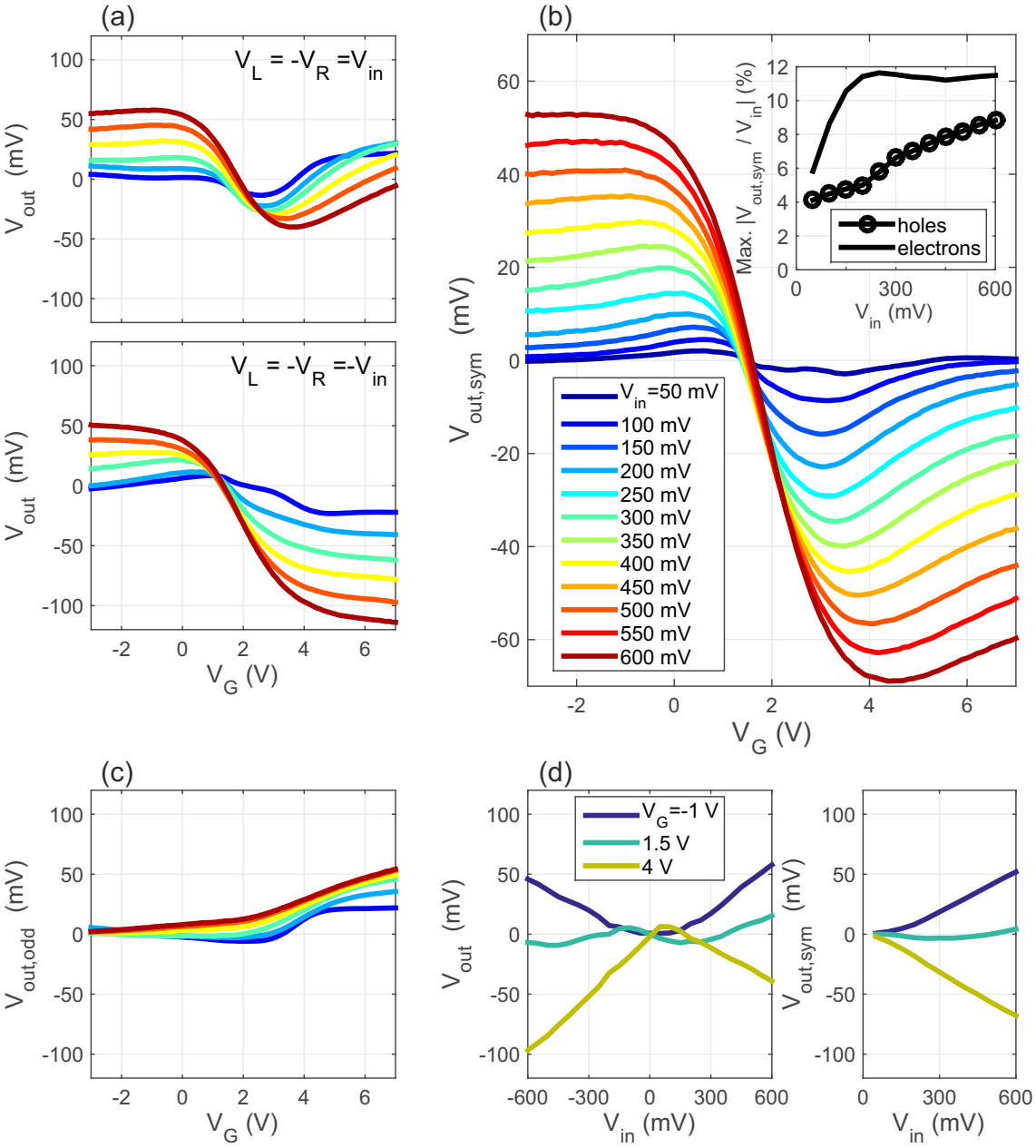

Figure A.9: LN_2-temperature output-voltage data from sample F32 (measurement configuration shown in figure A.1). (a) V_{out} as function of back-gate voltage V_G for different input voltages V_{in} and both bias configurations [Same color code as in (b)]. (b) Symmetric part calculated from the raw data in (a). The inset shows the maximum efficiency as function of V_{in}. (c) Odd part calculated from the raw data in (a) [Same color code as in (b)]. (d) Replotting of data sets in (a) and (b) in order to show the dependence of V_{out} and $V_{out,sym}$ on V_{in} at certain V_G-values.

A.2 Data from 100-nm sample (F48E4)

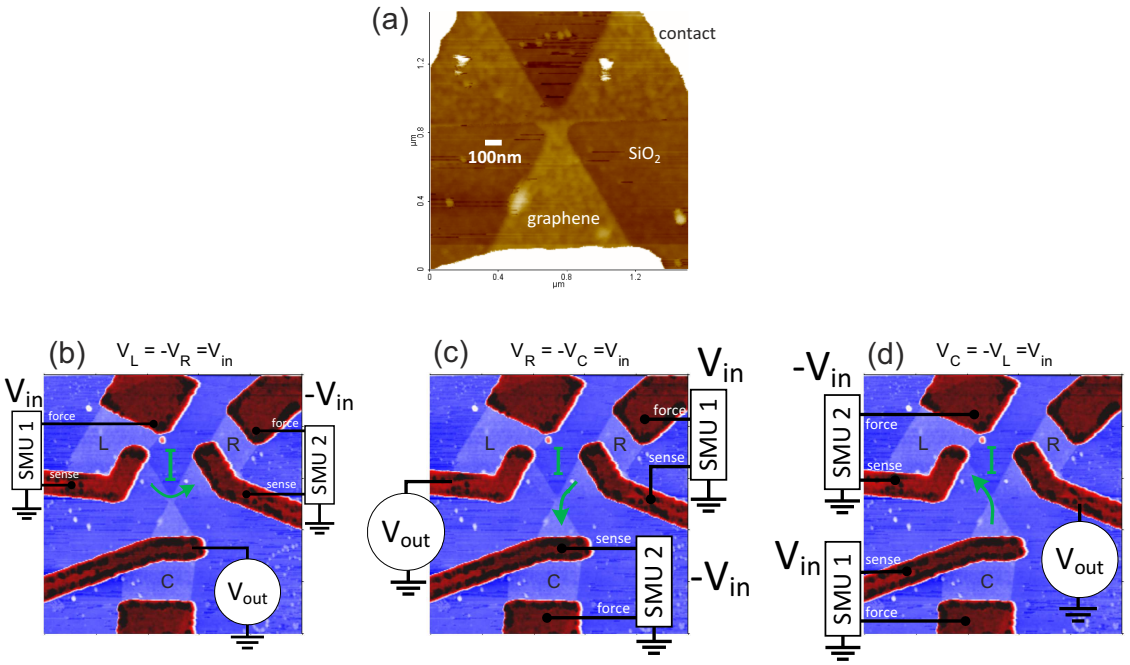

Figure A.10: Sample F48E4 with constriction sizes 100 nm. (a) 1.5x1.5 µm^2 AFM scan of the GTTJ. (b-d) Measurement configurations (5x5 µm^2 AFM scans). Terminals L, R, and C in pale blue and electrical contacts in red. Graphene connects each inner contact to an adjacent outer one. Push-pull bias $\pm V_{in}$ was applied to two terminals, generating a current I. SMU *sense* outputs were connected to inner contacts. V_{out} was probed with a multimeter at the remaining inner contact. The remaining outer contact was left open. A back-gate voltage was applied to the silicon substrate.

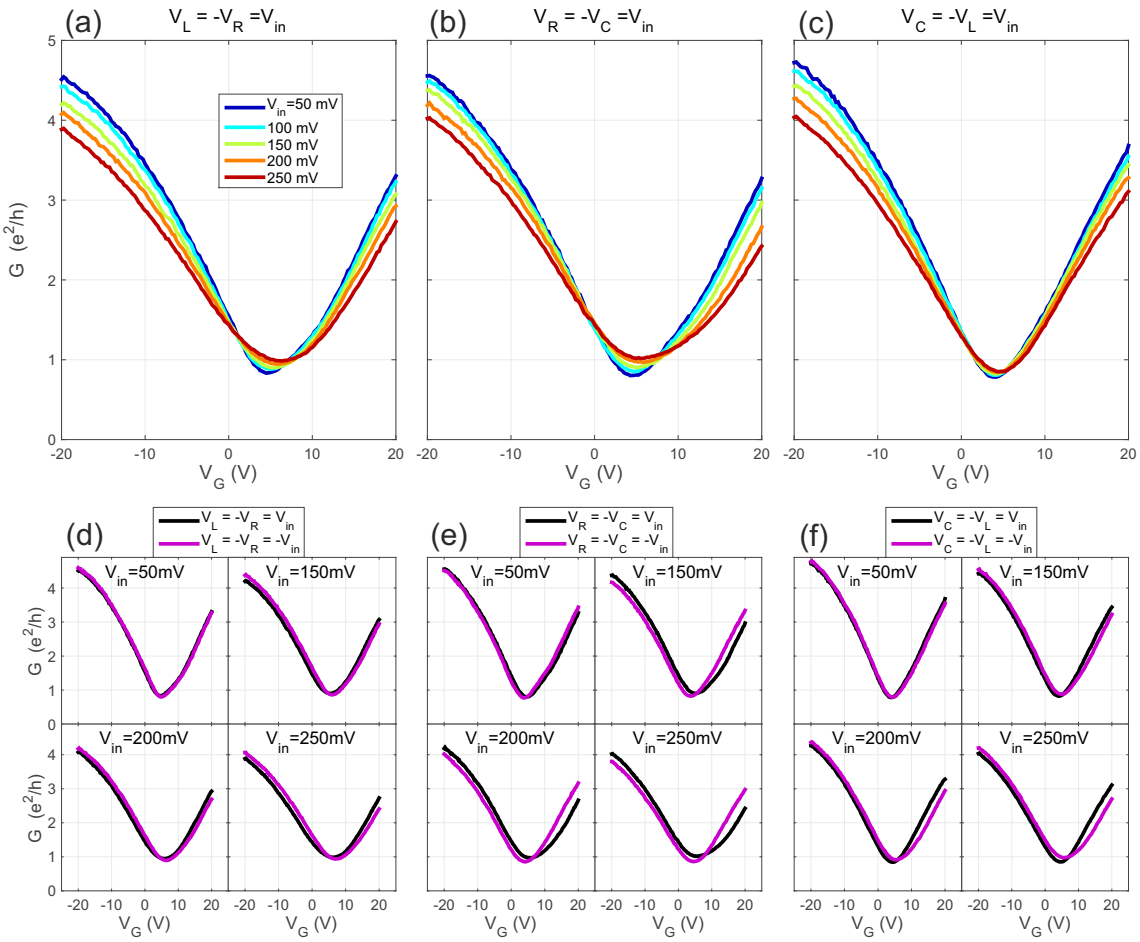

Figure A.11: Room-temperature conductance data from sample F48E4 (measurement configurations shown in figure A.10). (a-c) Conductance as function of back-gate voltage V_G for different input voltages V_{in}, respectively for each measurement configuration. (d-f) Conductance curves from (a-c) compared to curves from measurement at same V_{in} of opposite sign, respectively for each measurement configuration.

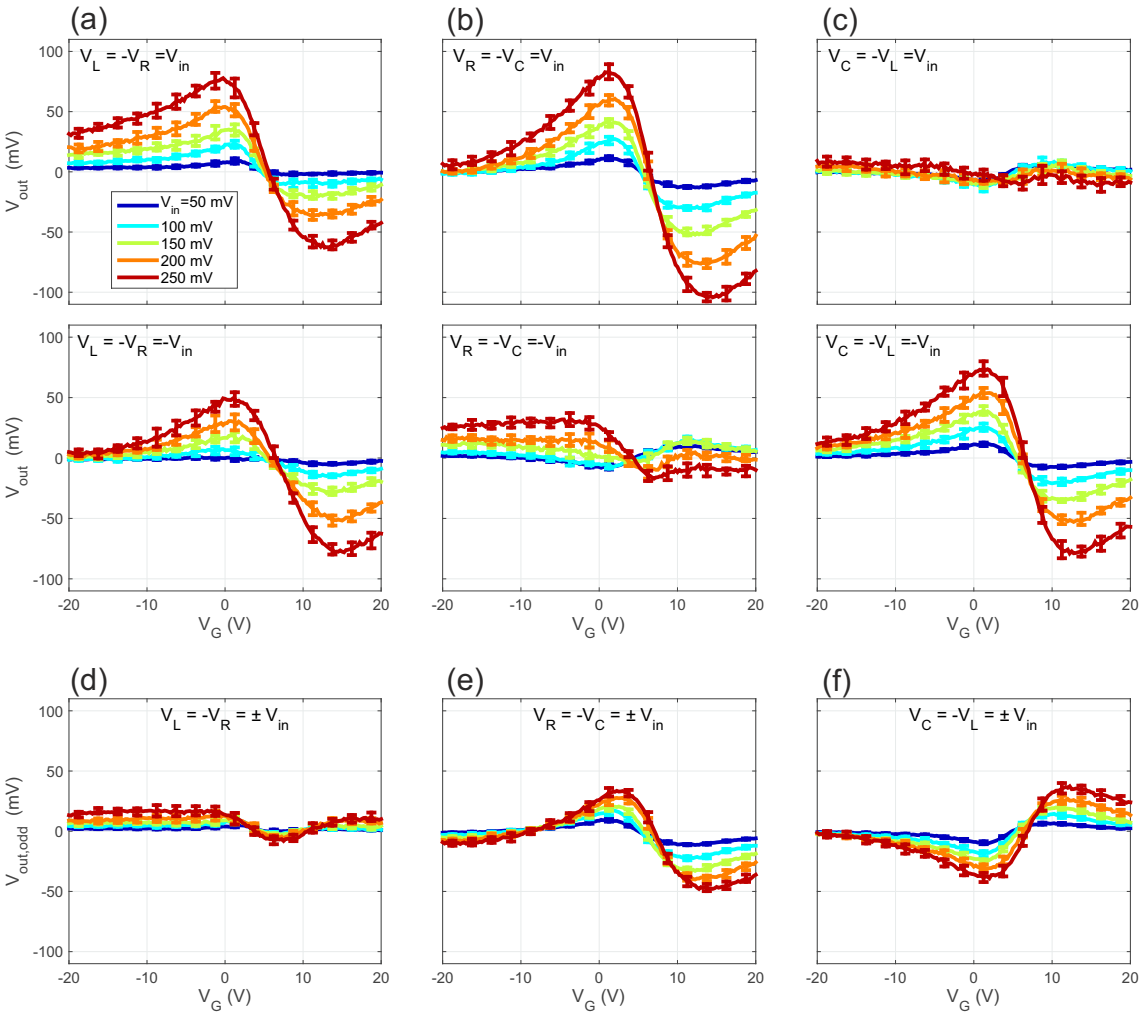

Figure A.12: Room-temperature output-voltage data from sample F48E4 (measurement configurations shown in figure A.10). (a-c) V_{out} as function of back-gate voltage V_G for different input voltages V_{in} and both bias configurations, respectively for each measurement configuration. (d-f) Odd part calculated from the raw data in (a-c), respectively for each measurement configuration. Same color code for all plots.

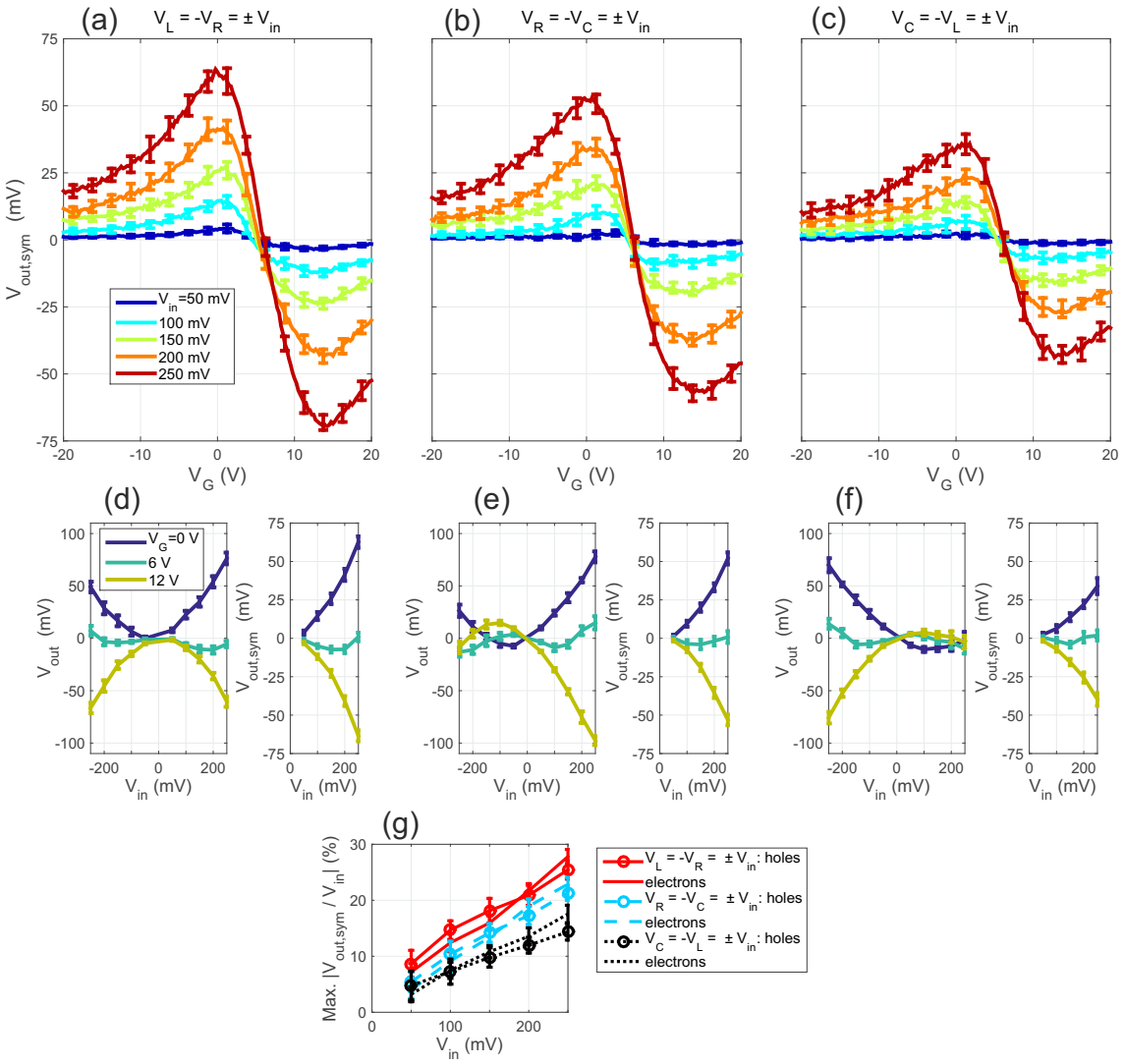

Figure A.13: Room-temperature output-voltage data (symmetric part) from sample F48E4 (measurement configurations shown in figure A.10). (a-c) Symmetric part calculated from the raw data in figure A.12(a-c), respectively for each measurement configuration (same color code). (d-f) Replotting of data sets in (a-c) and figure A.12(a-c) in order to show the dependence of V_{out} and $V_{out,sym}$ on V_{in} at certain V_G-values (same color code). (g) Maximum efficiency as function of V_{in}.

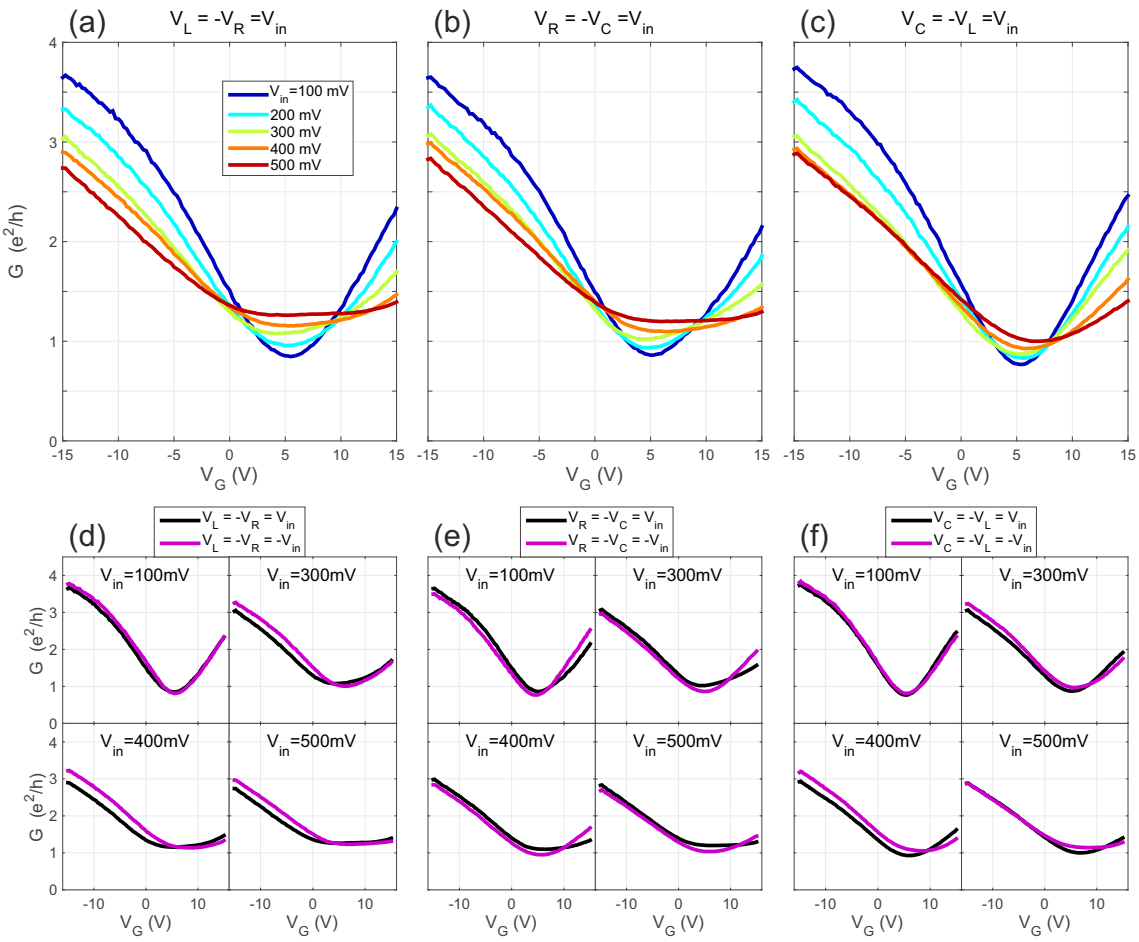

Figure A.14: Room-temperature conductance data from sample F48E4 (measurement configurations shown in figure A.10). (a-c) Conductance as function of back-gate voltage V_G for different input voltages V_{in}, respectively for each measurement configuration. (d-f) Conductance curves from (a-c) compared to curves from measurement at same V_{in} of opposite sign, respectively for each measurement configuration.

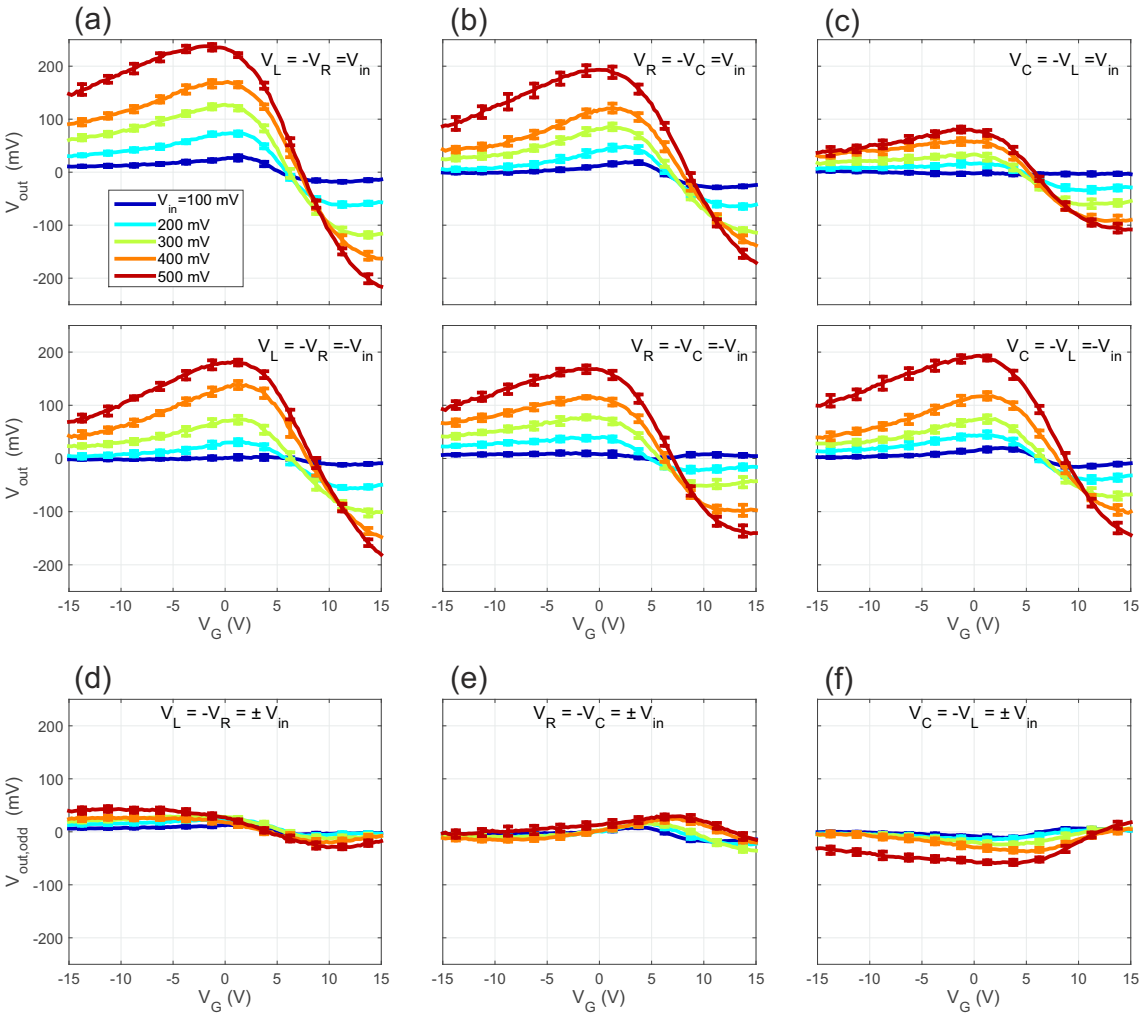

Figure A.15: Room-temperature output-voltage data from sample F48E4 (measurement configurations shown in figure A.10). (a-c) V_{out} as function of back-gate voltage V_G for different input voltages V_{in} and both bias configurations, respectively for each measurement configuration. (d-f) Odd part calculated from the raw data in (a-c), respectively for each measurement configuration. Same color code for all plots.

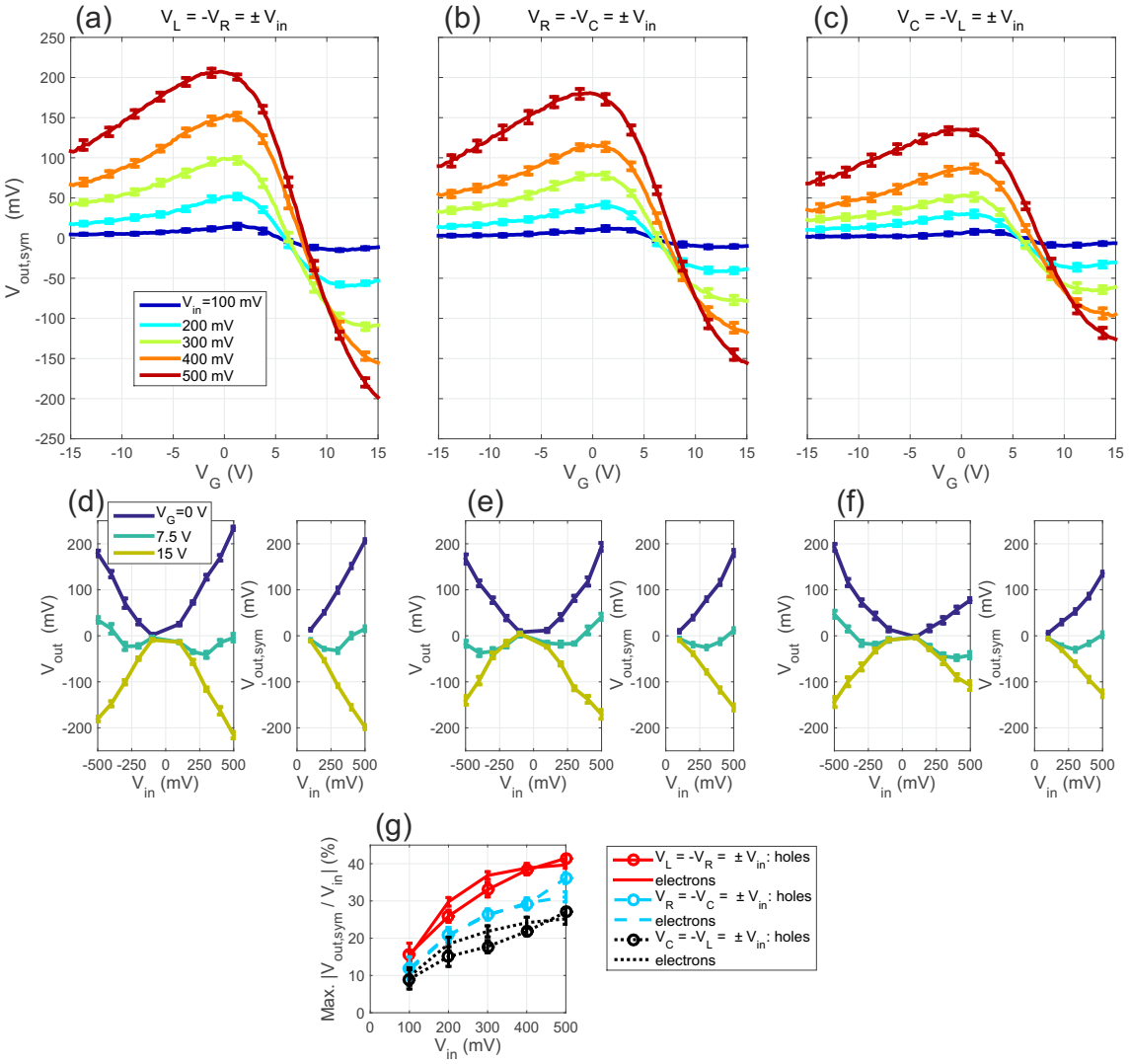

Figure A.16: Room-temperature output-voltage data (symmetric part) from sample F48E4 (measurement configurations shown in figure A.10). (a-c) Symmetric part calculated from the raw data in figure A.15(a-c), respectively for each measurement configuration (same color code). (d-f) Replotting of data sets in (a-c) and figure A.15(a-c) in order to show the dependence of V_{out} and $V_{out,sym}$ on V_{in} at certain V_G-values (same color code). (g) Maximum efficiency as function of V_{in}.

A.3 Data from 150-nm sample (F33E2)

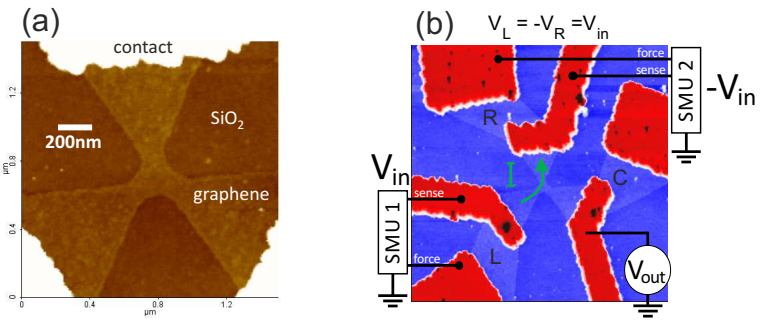

Figure A.17: Sample F33E2 with constriction sizes 150 nm. (a) 1.5x1.5 µm^2 AFM scan of the GTTJ. (b) Measurement configuration (5x5 µm^2 AFM scan). Terminals L, R, and C in pale blue and electrical contacts in red. Graphene connects each inner contact to an adjacent outer one. Push-pull bias $\pm V_{in}$ was applied to two terminals, generating a current I. SMU *sense* outputs were connected to inner contacts. V_{out} was probed with a multimeter at the remaining inner contact. The remaining outer contact was left open. A back-gate voltage was applied to the silicon substrate.

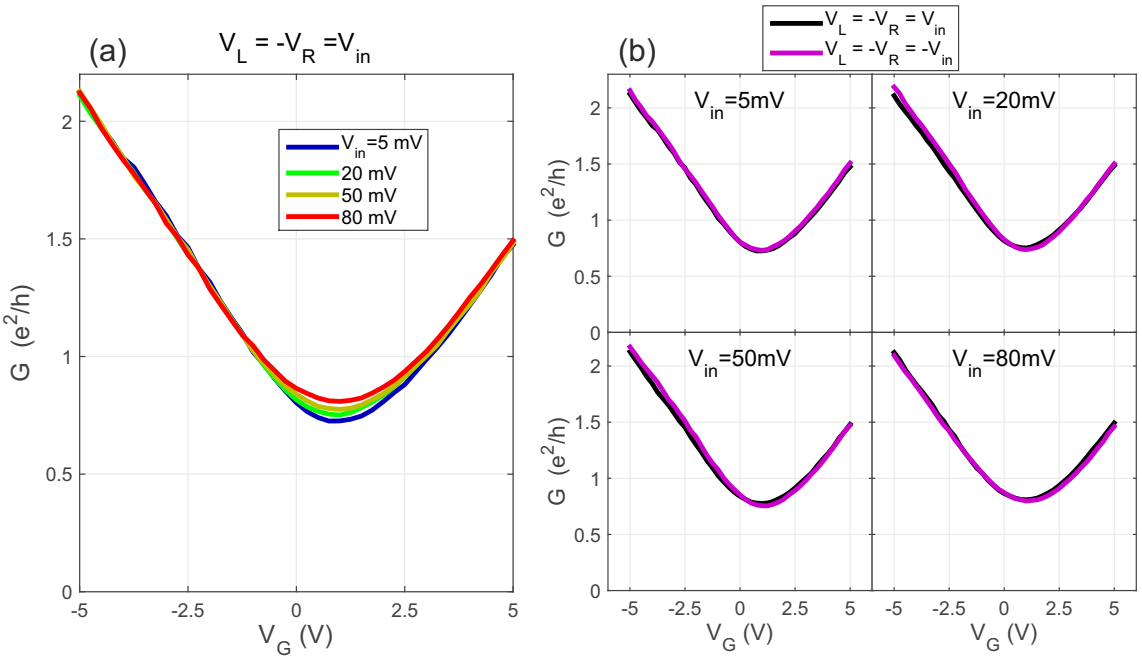

Figure A.18: Room-temperature conductance data from sample F33E2 (measurement configuration shown in figure A.17). (a) Conductance as function of back-gate voltage V_G for different input voltages V_{in}. (b) Conductance curves from (a) compared to curves from measurement at same V_{in} of opposite sign.

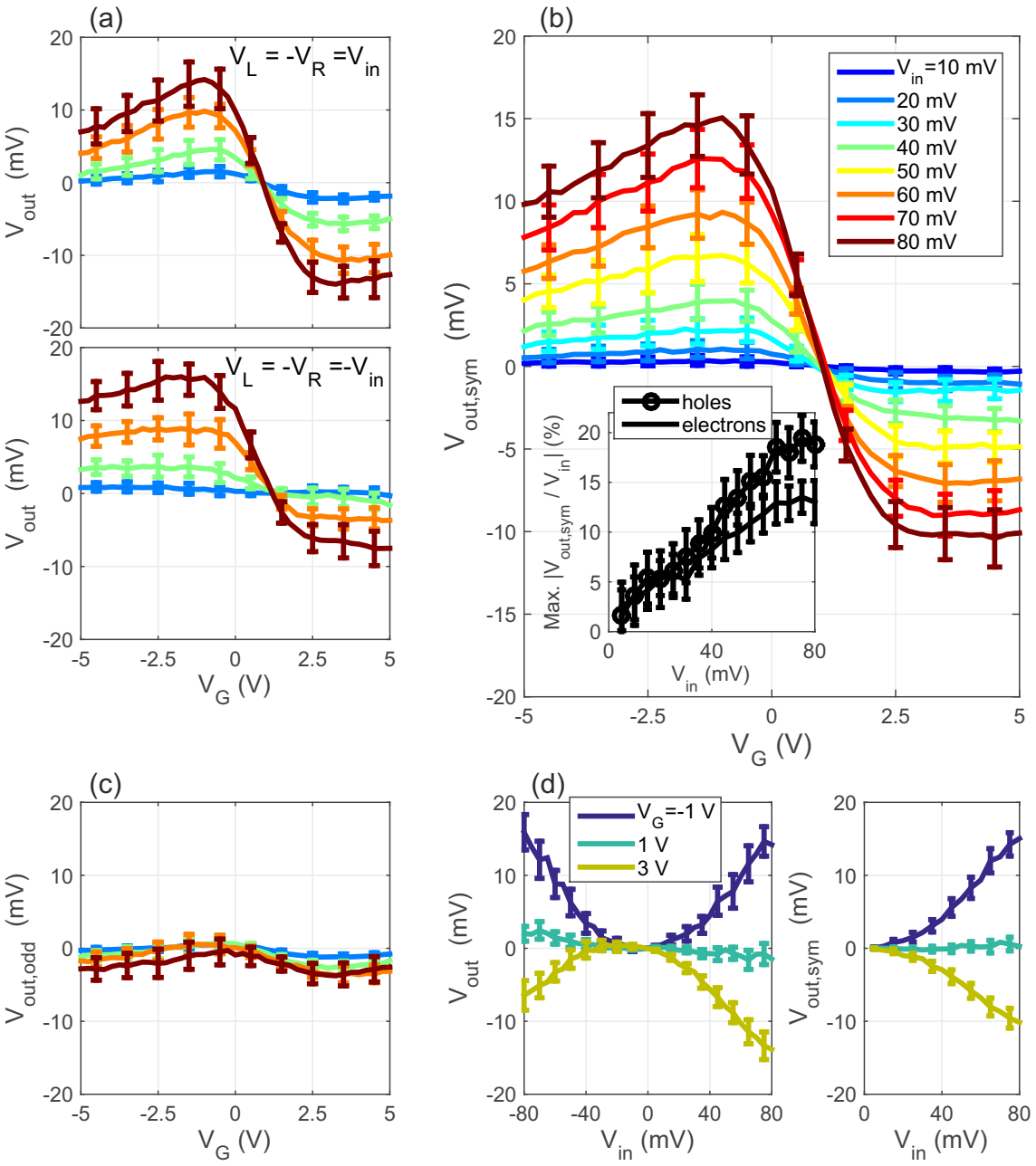

Figure A.19: Room-temperature output-voltage data from sample F33E2 (measurement configuration shown in figure A.17). (a) V_{out} as function of back-gate voltage V_G for different input voltages V_{in} and both bias configurations [Same color code as in (b)]. (b) Symmetric part calculated from the raw data in (a). The inset shows the maximum efficiency as function of V_{in}. (c) Odd part calculated from the raw data in (a) [Same color code as in (b)]. (d) Replotting of data sets in (a) and (b) in order to show the dependence of V_{out} and $V_{out,sym}$ on V_{in} at certain V_G-values.

A.4 Data from 200-nm sample (F48E3)

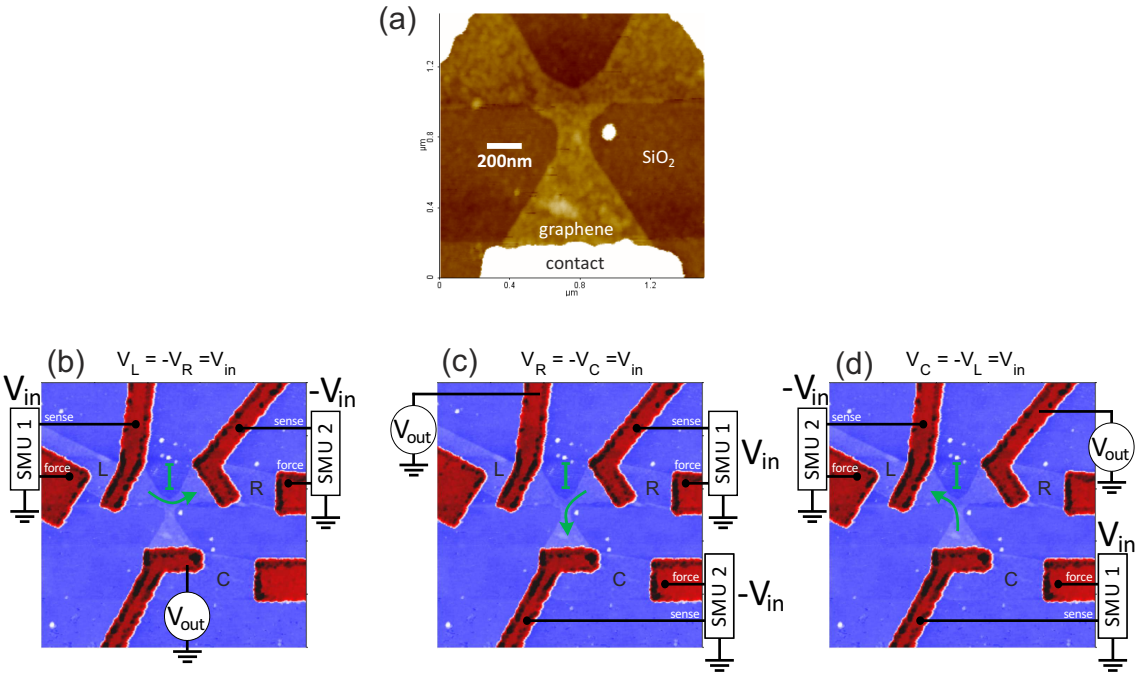

Figure A.20: Sample F48E3 with constriction sizes 200 nm. (a) 1.5x1.5 µm^2 AFM scan of the GTTJ. (b-d) Measurement configurations (5x5 µm^2 AFM scans). Terminals L, R, and C in pale blue and electrical contacts in red. Graphene connects each inner contact to an adjacent outer one. Push-pull bias $\pm V_{in}$ was applied to two terminals, generating a current I. SMU *sense* outputs were connected to inner contacts. V_{out} was probed with a multimeter at the remaining inner contact. The remaining outer contact was left open. A back-gate voltage was applied to the silicon substrate.

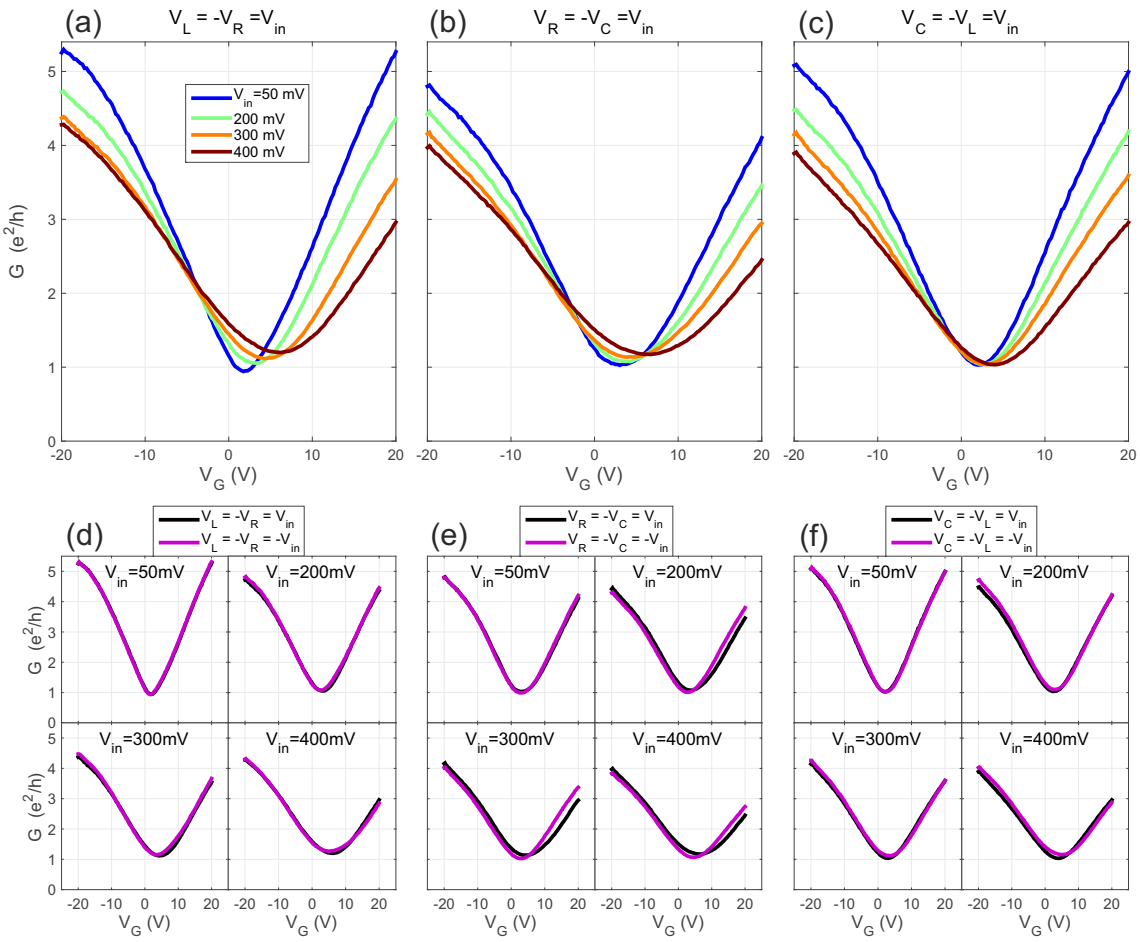

Figure A.21: Room-temperature conductance data from sample F48E3 (measurement configurations shown in figure A.20). (a-c) Conductance as function of back-gate voltage V_G for different input voltages V_{in}, respectively for each measurement configuration. (d-f) Conductance curves from (a-c) compared to curves from measurement at same V_{in} of opposite sign, respectively for each measurement configuration.

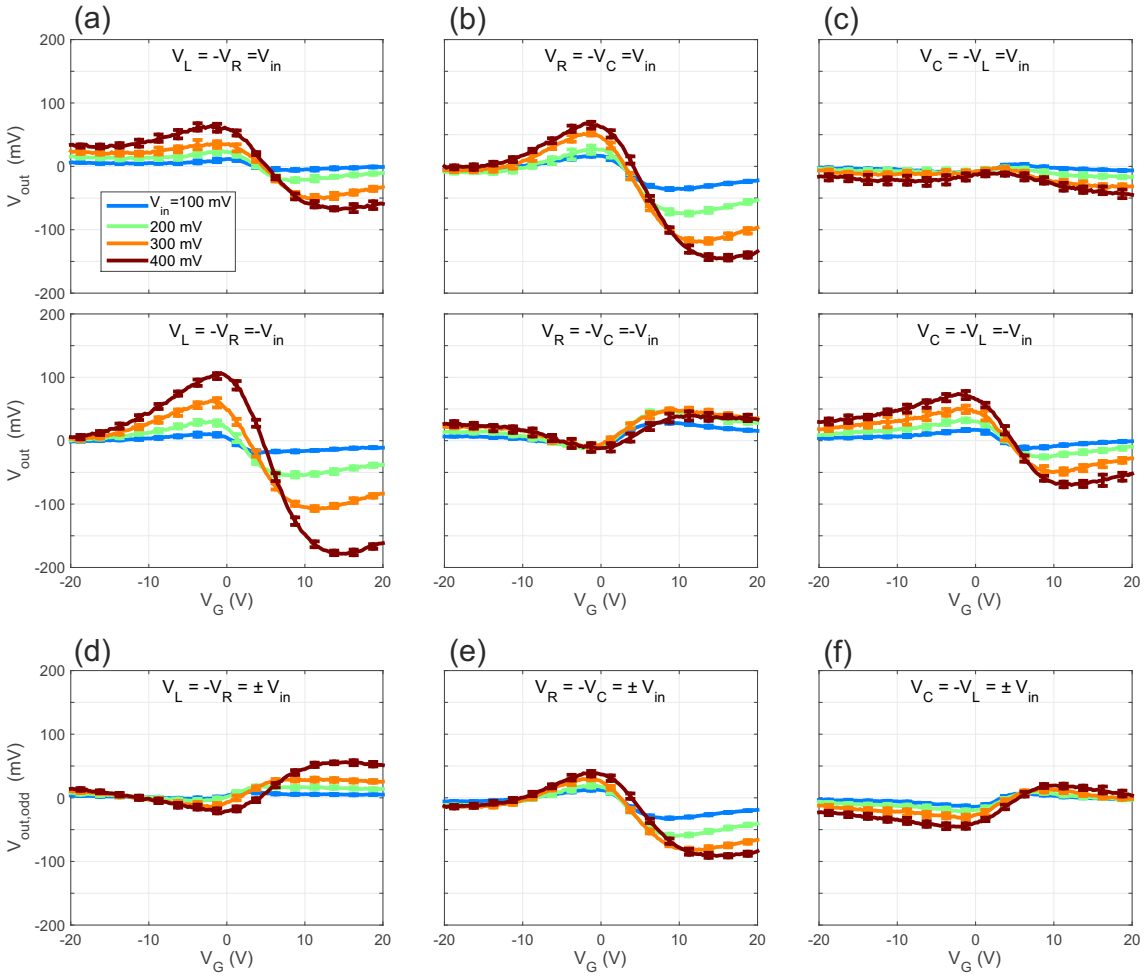

Figure A.22: Room-temperature output-voltage data from sample F48E3 (measurement configurations shown in figure A.20). (a-c) V_{out} as function of back-gate voltage V_G for different input voltages V_{in} and both bias configurations, respectively for each measurement configuration. (d-f) Odd part calculated from the raw data in (a-c), respectively for each measurement configuration. Same color code for all plots.

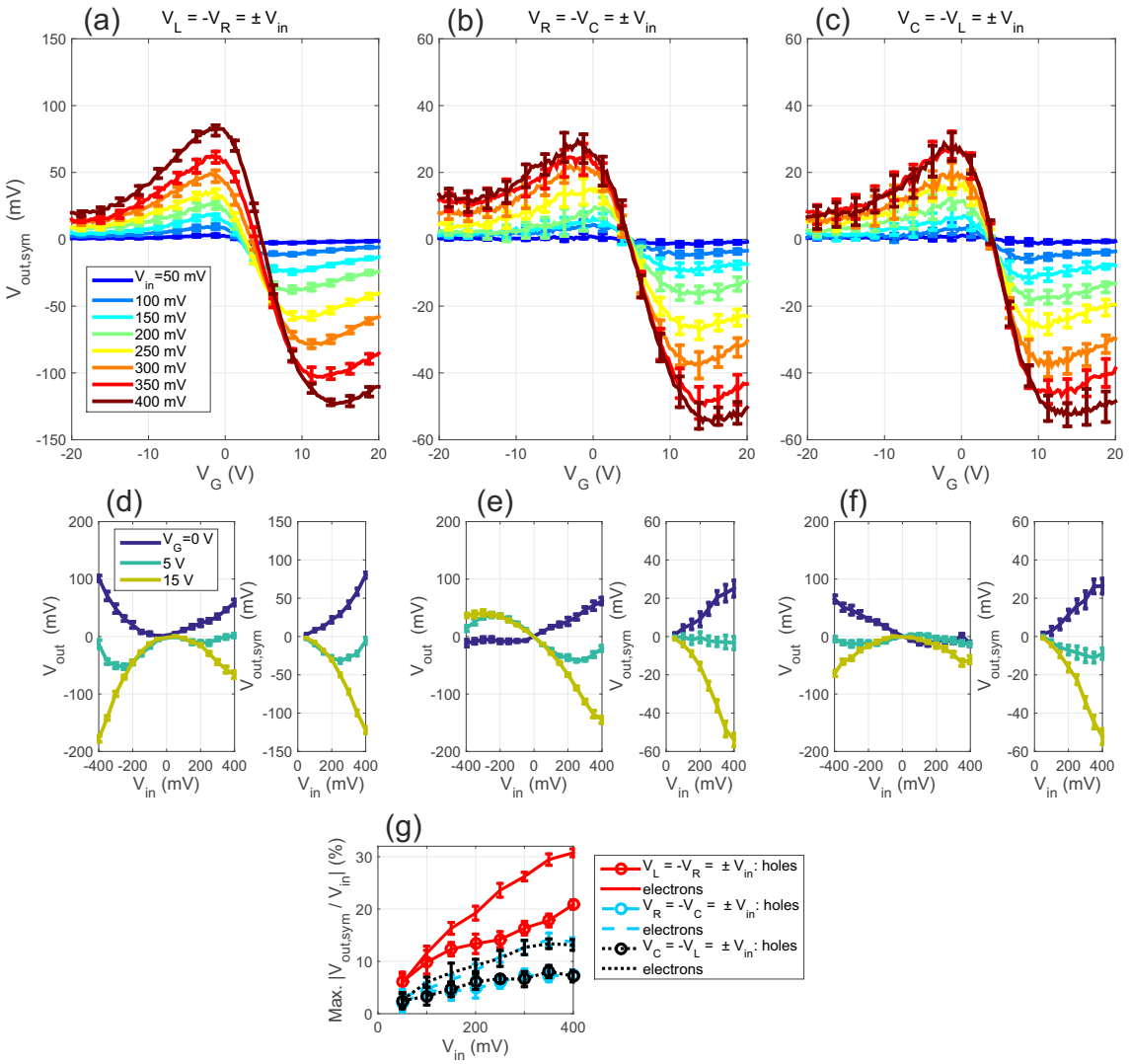

Figure A.23: Room-temperature output-voltage data (symmetric part) from sample F48E3 (measurement configurations shown in figure A.20). (a-c) Symmetric part calculated from the raw data in figure A.22(a-c), respectively for each measurement configuration (same color code). (d-f) Replotting of data sets in (a-c) and figure A.22(a-c) in order to show the dependence of V_{out} and $V_{out,sym}$ on V_{in} at certain V_G-values (same color code). (g) Maximum efficiency as function of V_{in}.

A.5 Data from 400-nm sample (F33C1)

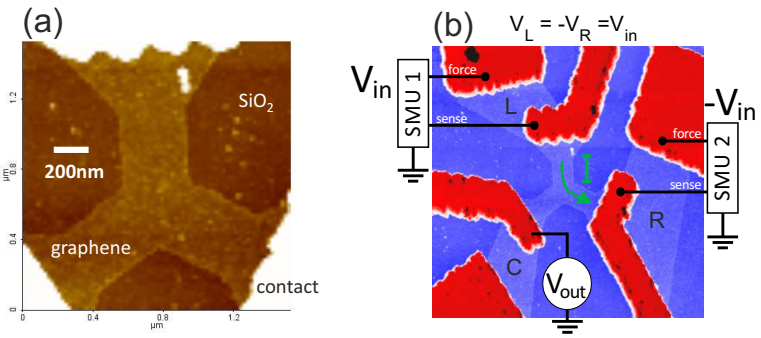

Figure A.24: Sample F33C1 with constriction sizes 400 nm. (a) 1.5x1.5 µm^2 AFM scan of the GTTJ. (b) Measurement configuration (5x5 µm^2 AFM scan). Terminals L, R, and C in pale blue and electrical contacts in red. Graphene connects each inner contact to an adjacent outer one. Push-pull bias $\pm V_{in}$ was applied to two terminals, generating a current I. SMU *sense* outputs were connected to inner contacts. V_{out} was probed with a multimeter at the remaining inner contact. The remaining outer contact was left open. A back-gate voltage was applied to the silicon substrate.

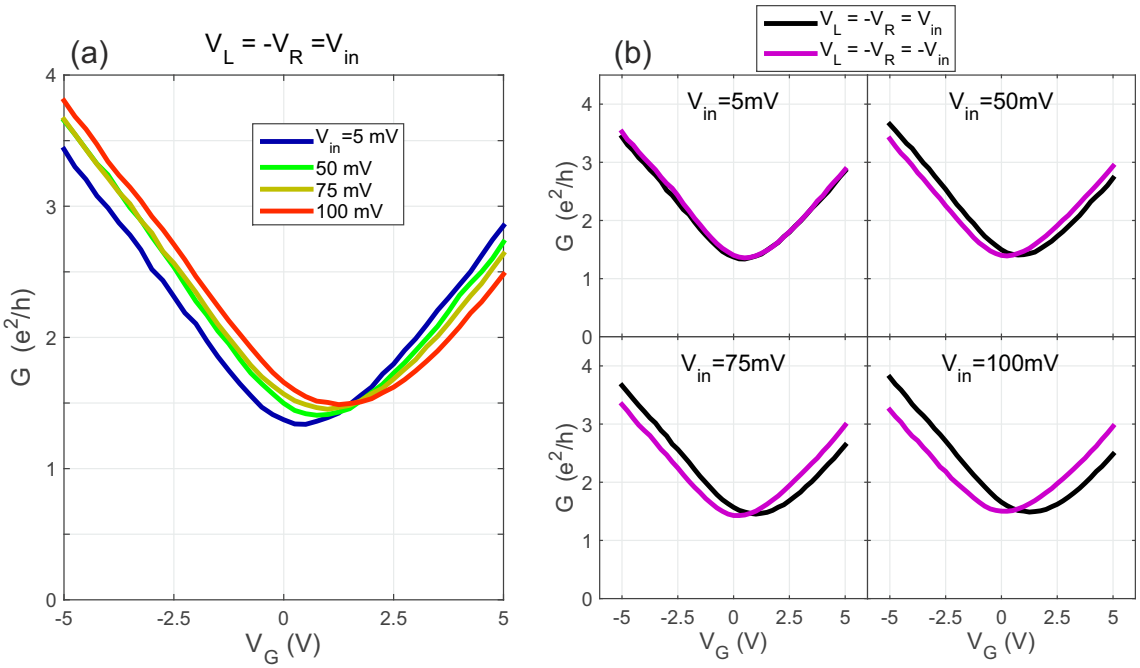

Figure A.25: Room-temperature conductance data from sample F33C1 (measurement configuration shown in figure A.24). (a) Conductance as function of back-gate voltage V_G for different input voltages V_{in}. (b) Conductance curves from (a) compared to curves from measurement at same V_{in} of opposite sign.

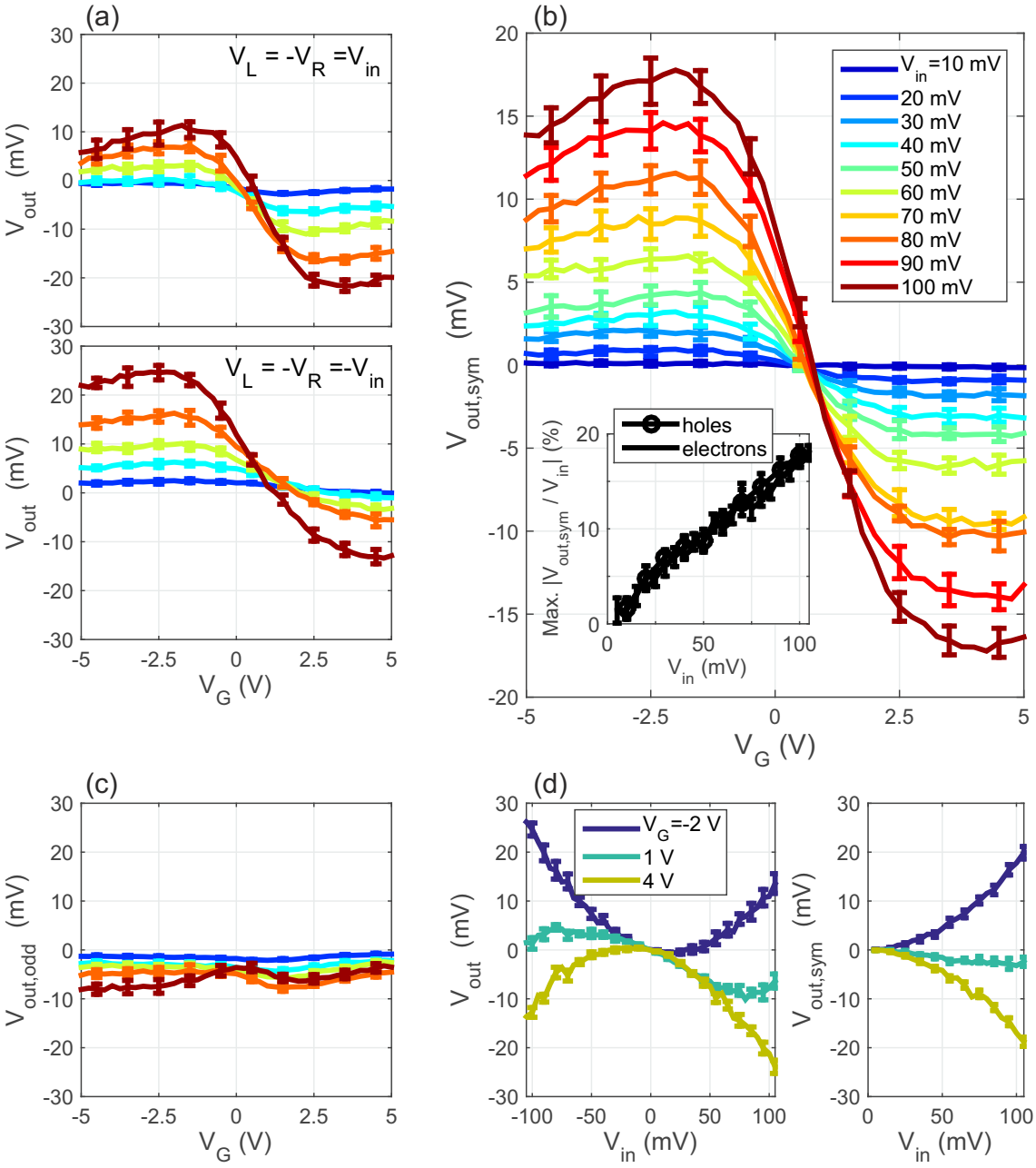

Figure A.26: Room-temperature output-voltage data from sample F33C1 (measurement configuration shown in figure A.24). (a) V_{out} as function of back-gate voltage V_G for different input voltages V_{in} and both bias configurations [Same color code as in (b)]. (b) Symmetric part calculated from the raw data in (a). The inset shows the maximum efficiency as function of V_{in}. (c) Odd part calculated from the raw data in (a) [Same color code as in (b)]. (d) Replotting of data sets in (a) and (b) in order to show the dependence of V_{out} and $V_{out,sym}$ on V_{in} at certain V_G-values.

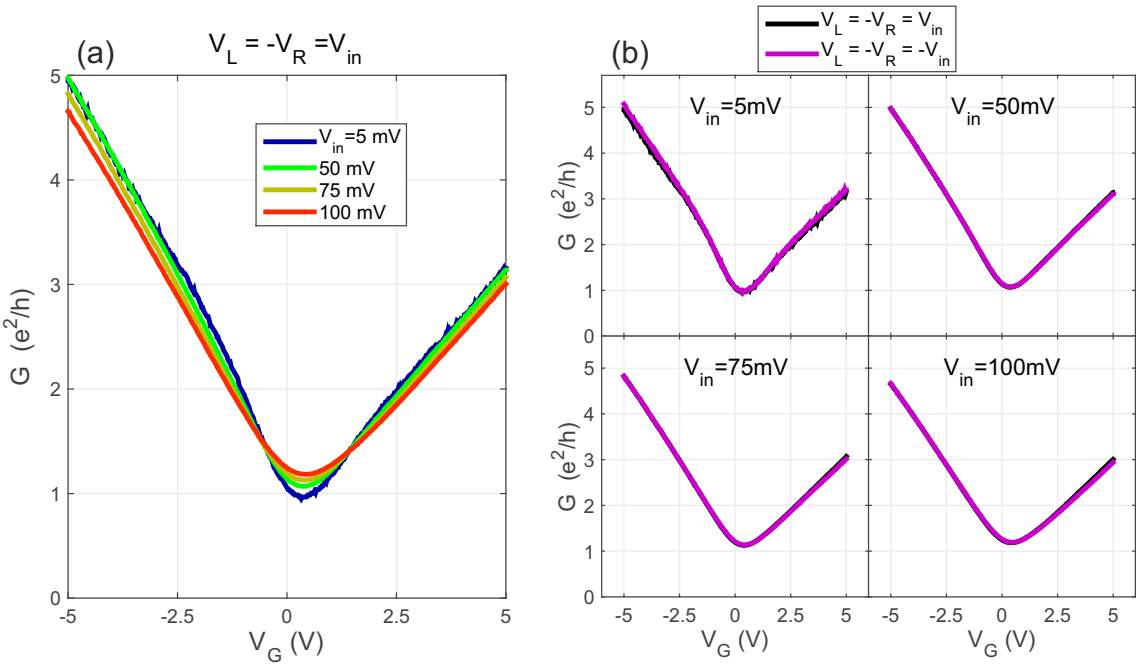

Figure A.27: LN_2 temperature conductance data from sample F33C1, measurement configuration shown in figure A.24. (a) Conductance as function of back-gate voltage V_G for different input voltages V_{in}. (b) Conductance curves from (a) compared to curves from measurement at same V_{in} of opposite sign.

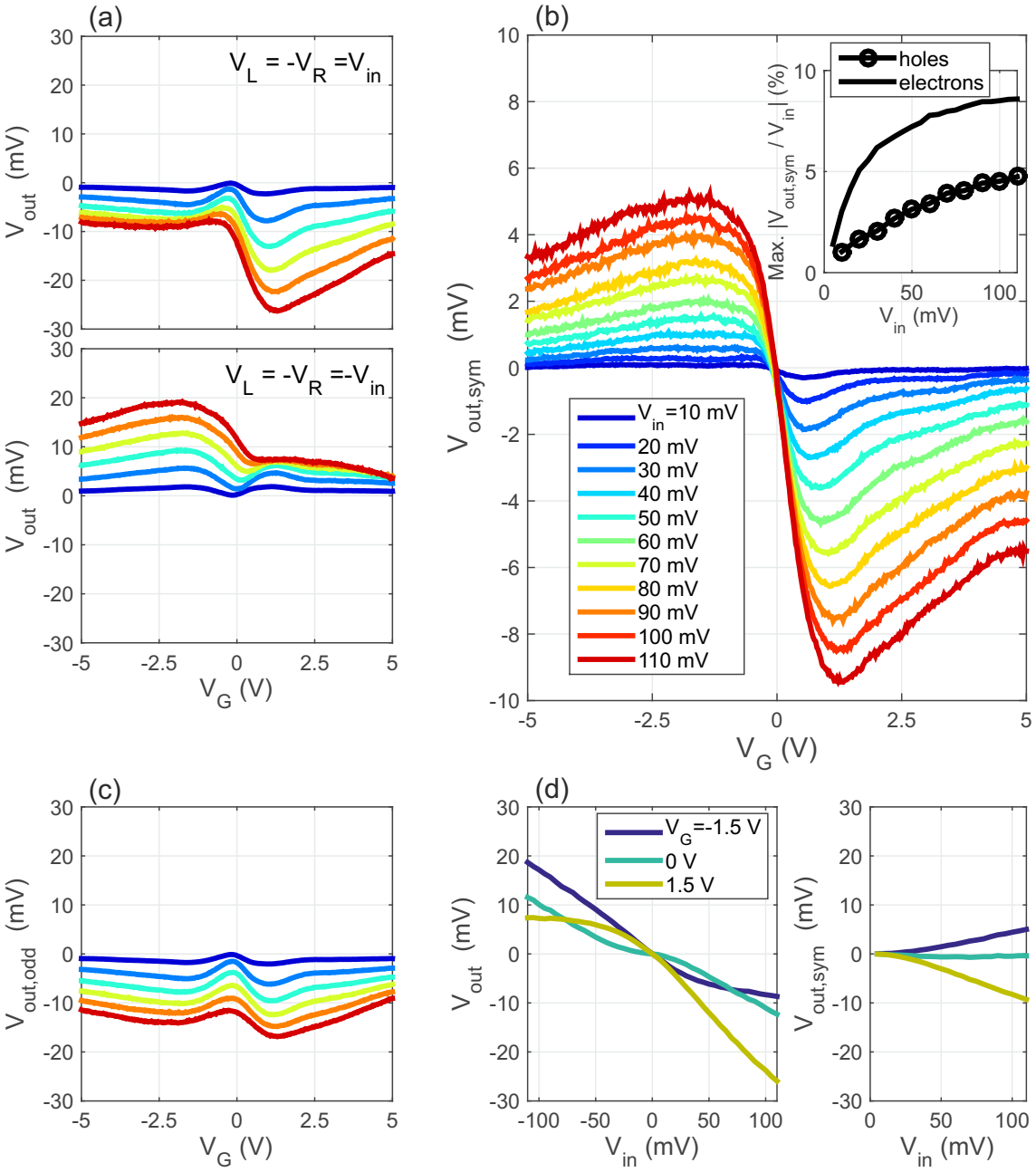

Figure A.28: LN_2-temperature output-voltage data from sample F33C1 (measurement configuration shown in figure A.24). (a) V_{out} as function of back-gate voltage V_G for different input voltages V_{in} and both bias configurations [Same color code as in (b)]. (b) Symmetric part calculated from the raw data in (a). The inset shows the maximum efficiency as function of V_{in}. (c) Odd part calculated from the raw data in (a) [Same color code as in (b)]. (d) Replotting of data sets in (a) and (b) in order to show the dependence of V_{out} and $V_{out,sym}$ on V_{in} at certain V_G-values.

Appendix B

Processes

Process	Description
Fabrication of chips with pads and markers (photo-lithography)	
Wafer: 4" oxidized silicon wafer (thermally grown SiO_2, 285±5 nm, from *NOVA Electronic Materials*)	
HMDS spinning (adhesion promoter)	6 drops, 3000 rpm for 40s (3s ramp-time), closed holes of cover
Resist spinning: *ma-N 1405*	Cover whole wafer surface, 3000 rpm for 40s (3s ramp-time), closed holes of cover ; bake wafer on hotplate at 100°C for 1 min; remove resist at wafer edges with acetone (cotton stick)
Mask alignment and exposure	Use mask *Ensslin - ETH First graphene* (date 3-17-08) ; dose 170 mJ/cm^2 (365-nm light source, constant power, hard contact)
Development	Put in *ma-D 533-S* for 2 min, gently moving wafer ; put in flowing deionized water for 1 min ; blow dry with N_2 gun
Plasma ashing (removing resist residues)	O_2 plasma ashing at 200 W, 1 mbar, for 30s
Metal deposition	Physical vapor deposition: 5 nm titanium + 45 nm gold
Lift-off	Leave wafer in 50°C acetone for 5 min; peel off metal at edges with cotton stick ; leave in acetone for several hours, upside down on three metal pillars ; blow sample with pipette until metal detaches from sample (or use ultra-sound bursts or cotton stick scratching if pipette blowing does not work) ; put in IPA and check under microscope if lift-off was successful ; blow dry with N_2 gun
Dicing	Spin protective resist layer (e.g. *ma-N 1405*) ; dice wafer into 7.1 x 7.1 mm^2 chips
Chip cleaning before graphene deposition	Put in 50°C acetone for 4 min (ultra-sonic bath) ; repeat 2x with fresh acetone ; put in 50°C IPA for 2 min (ultra-sonic bath) ; blow dry with N_2 gun ; O_2 plasma ashing at 200 W, 1 mbar, for 10 min

Process	Description
Nanostructure fabrication: contacts	
Resist spinning: PMMA 50K, pure in chlorobenzene	Cover whole chip surface (1 drop), 5000 rpm for 45s (5s ramp-time), closed holes of cover ; bake chip on hotplate at 180°C for 5 min.
Resist spinning: PMMA 950K, 1:1 in chlorobenzene	Cover whole chip surface (1 drop), 5000 rpm for 45s (5s ramp-time), closed holes of cover ; bake chip on hotplate at 180°C for 5 min.
Electron-beam lithography	30 kV acceleration voltage, aperture 30 µm (current $\sim$ 300 pA), dose 550 µC/cm^2 (for markers dose x1.5), step 20 nm (dwell time $\sim$ 6 µs)
Development	1 min in MIBK 3:1 in IPA, 30s in IPA, blow dry with N_2 gun
Metal deposition	Physical vapor deposition: 1 nm chrome + 50 nm gold
Lift-off	Leave sample in 50°C acetone for 5 min; peel off metal at edges with cotton stick ; leave in 50°C acetone for at least 20 min; blow sample with pipette until metal detaches from sample ; put in IPA and check under microscope if lift-off was successful ; blow dry with N_2 gun
Nanostructure fabrication: TTJ geometry	
Resist spinning: PMMA 950K, 1:1 in chlorobenzene	Cover whole chip surface (1 drop), 5000 rpm for 45s (5s ramp-time), closed holes of cover ; bake chip on hotplate at 180°C for 5 min.
Electron-beam lithography	30 kV acceleration voltage, aperture 10 µm (current $\sim$ 30 pA), dose 350 µC/cm^2, step 4 nm (dwell time $\sim$ 3 µs)
Development	1 min in MIBK 3:1 in IPA, 30s in IPA, blow dry with N_2 gun
Reactive ion etching	40 sccm Ar and 5 sccm O_2, 35 mTorr, 315 V bias, 60 W RF power, 10s effective etching duration (counting start at plasma generation)
Resist removal	Put sample upside down in 50°C acetone, shaking it with tweezers for 7 min; put upside down in fresh 50°C acetone for 1 hour ; blow sample with pipette ; put in IPA ; blow dry with N_2 gun

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Publications

Finite element simulations of graphene based three-terminal nanojunction rectifiers
P. Butti, I. Shorubalko, U. Sennhauser, and K. Ensslin
Journal of Applied Physics, vol. 114, p. 033710, 2013.

Field effect in the quantum Hall regime of a high mobility graphene wire
C. Barraud, T. Choi, P. Butti, I. Shorubalko, T. Taniguchi, K. Watanabe, T. Ihn, and K. Ensslin
Journal of Applied Physics, vol. 116, p. 073705, 2014.

Thermal voltages in graphene three-terminal nanojunctions
P. Butti, I. Shorubalko, and K. Ensslin
(in preparation).

Acknowledgments

I would like to express my gratitude to Klaus Ensslin for great guidance and constant support. His optimism has been especially encouraging in times when I was stuck. Further thanks to Urs Sennhauser and Michel Calame for giving me the opportunity to work at Empa and for valuable advice. Special thanks to Alex Dommann for his interest in the project and for additional support. Moreover, I want to thank Jérôme Faist for participating in the examination.

Great thanks are due to my mentor Ivan Shorubalko, who taught me everything there is to know about cleanroom processing and electrical measurement techniques. He has always been eager to share his knowledge of the small things that make experiments work. His enthusiasm for experimental results is really contagious and has been a big motivation for me.

I am very grateful to the nano-physics group at ETH Zurich for important knowledge exchange on graphene device fabrication: thank-you to Dominik Bischoff, Pauline Simonet, Anastasia Varlet, Clément Barraud, Marius Eich, Hiske Overweg, Theo Choi, and Arnhild Jacobsen. A big thank to everybody in the group for an always warm welcome.
Device fabrication was carried out at the FIRST cleanroom (Center for Micro- and Nano-Science, ETH Hönggerberg), and I would like to thank its staff for creating an excellent working environment. A special thank goes to Hansjakob Rusterholz for wafer-dicing. For access to AFM and Raman equipments at ETH Zurich and Empa, I am grateful to Christofer Hierold, Ulrich Müller, and Andreas Borgschulte.

For further helpful input, thanks to Olivier Scholder, Eugen Zgraggen, Cuno Künzler, Gregory Auton, Eduardo Cuervo Reyes, Clemens Nyffeler, and André Kupferschmid.

The project was made possible by the Swiss National Science Foundation (SNF), whose funding is gratefully acknowledged.

Many thanks go to all friends and colleagues from Empa for the great times. Jürgen, Eduardo, Ivan, and Matthias have been really pleasant office-mates. I'll surely remember the first-generation Durak sessions with Roman, Olivier, Eugen, Ivan, Sammy, and Konstantins. Breaks with Simi, Brian, Willi, Jeff, and Erkan were always good fun. It was exciting to be part of the Empa PhD Symposium organization team with Maike, Mateusz, Marie, and Gagik; many thanks to Anne Satir for general assistance.

Finally, I am deeply grateful to all friends outside from Empa for their encouragements, and to my parents for always believing in me. My biggest thank of all goes to Marina for her constant love and support.